

600 mA/1.25 MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER

FEATURES

- Up to 95% Conversion Efficiency
- Typical Quiescent Current: 18 μ A
- Load Current: 600 mA
- Operating Input Voltage Range: 2.5 V to 6.0 V
- Switching Frequency: 1.25 MHz
- Adjustable and Fixed Output Voltage
- Power Save Mode Operation at Light load Currents
- Active-Low $\overline{\text{MODE}}$ pin on TPS62021
- 100% Duty Cycle for Lowest Dropout
- Internal Softstart
- Dynamic Output Voltage Positioning
- Thermal Shutdown
- Short-Circuit Protection
- 10 Pin MSOP PowerPad™ Package
- 10 Pin QFN 3 X 3 mm Package

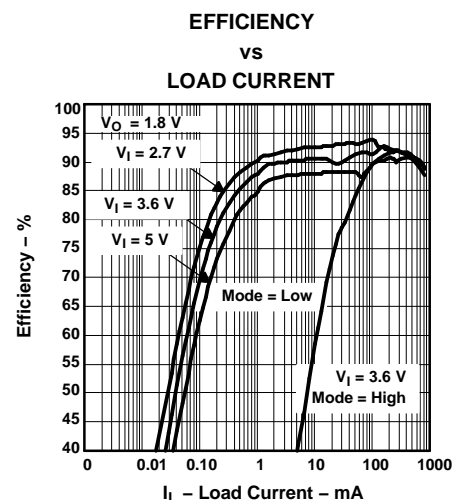
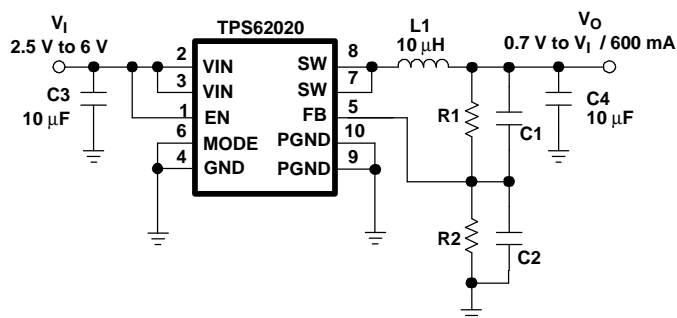
APPLICATIONS

- PDA, Pocket PC and Smart Phones
- USB Powered Modems
- CPUs and DSPs
- PC Cards and Notebooks
- xDSL Applications
- Standard 5-V to 3.3-V Conversion

DESCRIPTION

The TPS62020 is a high efficiency synchronous step-down dc-dc converter optimized for battery powered portable applications. This device is ideal for portable applications powered by a single Li-Ion battery cell or by 3-cell NiMH/NiCd batteries. With an output voltage range from 6.0 V down to 0.7 V, the device supports low voltage DSPs and processors in PDAs, pocket PCs, as well as notebooks and subnotebook computers. The TPS62020 operates at a fixed switching frequency of 1.25 MHz and enters the power save mode operation at light load currents to maintain high efficiency over the entire load current range. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the $\overline{\text{MODE}}$ pin high. The difference between the TPS62020 and the TPS62021 is the logic level of the $\overline{\text{MODE}}$ pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin. The TPS62020 supports up to 600-mA load current.

Typical Application Circuit (600-mA Output Current)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	MODE PIN LOGIC LEVEL	PACKAGE		PACKAGE MARKING	
		MSOP ⁽¹⁾	QFN ⁽²⁾	MSOP	QFN
-40°C to 85°C	MODE	TPS62020DGQ	TPS62020DRC	BBK	BBJ
	MODE	TPS62021DGQ	TPS62021DRC	ASH	ASJ

(1) The DGQ package is available in tape and reel. Add R suffix (DGQR) to order quantities of 2500 parts per reel.

(2) The DRC package is available in tape and reel. Add R suffix (DRCR) to order quantities of 3000 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

	UNITS
Supply voltage V _{IN} ⁽²⁾	-0.3 V to 7 V
Voltages on EN, MODE, FB, SW ⁽²⁾	-0.3 V to V _{CC} +0.3 V
Continuous power dissipation	See Dissipation Rating Table
Operating junction temperature range	-40°C to 150°C
Storage temperature range	-65°C to 150°C
Lead temperature (soldering, 10 sec)	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	R _{θJA} ⁽¹⁾	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
MSOP	60°C/W	1.67 W	917 mW	667 mW
QFN	48.7°C/W	2.05 W	1.13 W	821 mW

(1) The thermal resistance, R_{θJA} is based on a soldered PowerPAD using thermal vias.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
V _I Supply voltage	2.5		6.0	V
V _O Output voltage range for adjustable output voltage version	0.7		V _I	V
I _O Output current			600	mA
L Inductor ⁽¹⁾	3.3	10		μH
C _I Input capacitor ⁽¹⁾		10		μF
C _O Output capacitor ⁽¹⁾		10		μF
T _A Operating ambient temperature	-40		85	°C
T _J Operating junction temperature	-40		125	°C

(1) Refer to application section for further information

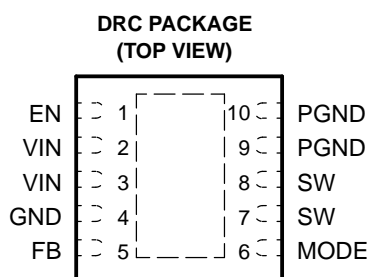
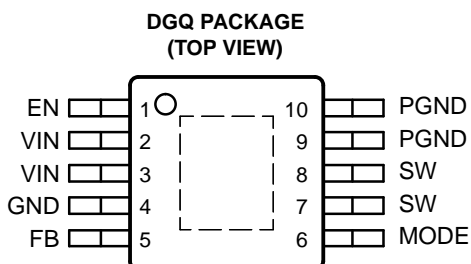
ELECTRICAL CHARACTERISTICS

$V_I = 3.6\text{ V}$, $V_O = 1.8\text{ V}$, $I_O = 600\text{ mA}$, $EN = VIN$, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT					
V_I Input voltage range		2.5		6.0	V
$I_{(Q)}$ Operating quiescent current	$I_O = 0\text{ mA}$, device is not switching		18	35	μA
I_{SD} Shutdown supply current	$EN = GND$		0.1	1	μA
V_{UVLO} Under-voltage lockout threshold		1.5		2.3	V
ENABLE AND MODE					
V_{EN} EN high level input voltage		1.4			V
V_{EN} EN low level input voltage				0.4	V
I_{EN} EN input bias current	$EN = GND$ or VIN		0.01	1.0	μA
$V_{(MODE)}$ MODE high level input voltage		1.4			V
$V_{(MODE)}$ MODE low level input voltage				0.4	V
$I_{(MODE)}$ MODE input bias current	$MODE = GND$ or VIN		0.01	1.0	μA
POWER SWITCH					
$r_{DS(ON)}$	P-channel MOSFET on-resistance	$V_I = V_{GS} = 3.6\text{ V}$	115	210	$\text{m}\Omega$
	P-channel MOSFET on-resistance	$V_I = V_{GS} = 2.5\text{ V}$	145	270	$\text{m}\Omega$
$I_{(kg(P))}$	P-channel leakage current	$V_{DS} = 6.0\text{ V}$		1	μA
$r_{DS(ON)}$	N-channel MOSFET on-resistance	$V_I = V_{GS} = 3.6\text{ V}$	85	200	$\text{m}\Omega$
	N-channel MOSFET on-resistance	$V_I = V_{GS} = 2.5\text{ V}$	115	280	$\text{m}\Omega$
$I_{(kg(N))}$	N-channel leakage current	$V_{DS} = 6.0\text{ V}$		1	μA
I_L	P-channel current limit	$2.5\text{ V} < V_I < 6.0\text{ V}$	0.9	1.1	A
	Thermal shutdown		150		$^\circ\text{C}$
OSCILLATOR					
f_S Oscillator frequency	$V_{FB} = 0.5\text{ V}$	1	1.25	1.5	MHz
	$V_{FB} = 0\text{ V}$		625		kHz
OUTPUT					
V_O Adjustable output voltage range		0.7		V_{IN}	V
V_{ref} Reference voltage			0.5		V
V_{FB} Feedback voltage	$V_I = 2.5\text{ V}$ to 6.0 V ; $I_O = 0\text{ mA}$	0%		3%	V
	$V_I = 2.5\text{ V}$ to 6.0 V ; $0\text{ mA} \leq I_O \leq 600\text{ mA}$	-3%		3%	V
Line regulation ⁽¹⁾	$V_I = V_O + 0.5\text{ V}$ (min 2.5 V) to 6.0 V , $I_O = 10\text{ mA}$		0		%/V
Load regulation ⁽¹⁾	$I_O = 10\text{ mA}$ to 1200 mA		0		%/mA
$I_{(kg(SW))}$	Leakage current into SW pin	$V_I > V_O$, $0\text{ V} \leq V_{SW} \leq V_I$		0.1	μA
	Reverse leakage current into pin SW	$V_I = \text{open}$; $EN = GND$; $V_{SW} = 6.0\text{ V}$		0.1	μA
f Short circuit switching frequency	$V_{FB} = 0\text{ V}$		625		kHz

(1) The line and load regulations are digitally controlled to assure an output voltage accuracy of $\pm 3\%$.

PIN ASSIGNMENTS



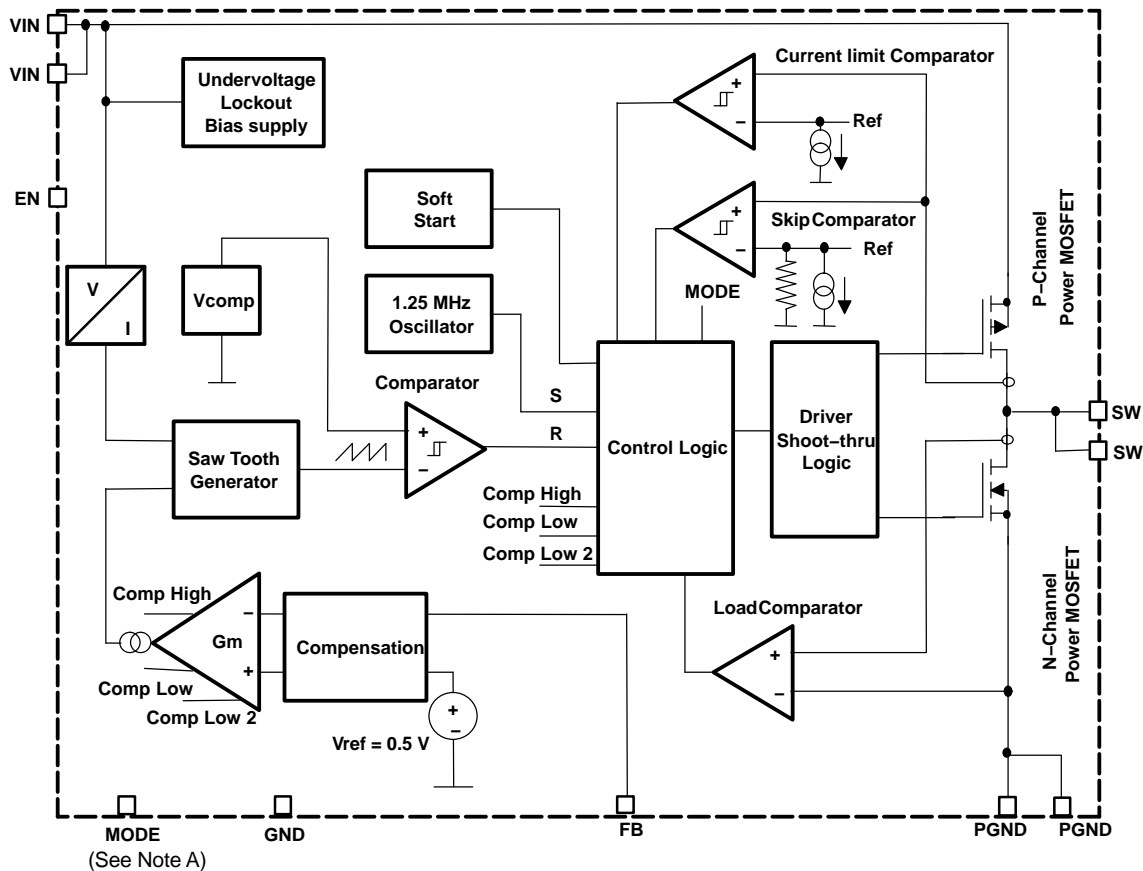
NOTE: The PowerPAD must be connected to GND.

PIN ASSIGNMENTS (continued)

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	1	I	Enable. Pulling EN to ground forces the device into shutdown mode. Pulling EN to V_I enables the device. EN should not be left floating and must be terminated.
VIN	2, 3	I	Supply voltage input
GND	4		Analog ground
FB	5	I	Feedback. Connect an external resistor divider to this pin.
MODE MODE	6	I	The difference between TPS62020 and TPS62021 is the logic level of the MODE pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin. The TPS62020 is forced into fixed-frequency PWM mode by pulling the MODE pin high. Pulling the MODE pin low enables the Power Save Mode, operating in PFM mode (Pulse frequency modulation) at light load current, and in fixed frequency PWM at medium to heavy load currents. In contrast, the TPS62021 is forced into PWM mode by pulling the $\overline{\text{MODE}}$ pin low.
SW	7, 8	I/O	This is the switch pin of the converter and connected to the drain of the internal power MOSFETs
PGND	9, 10		Power ground

FUNCTIONAL BLOCK DIAGRAM



NOTE A: The TPS62020 has an active-high MODE pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	1, 2, 3
η	Efficiency	vs Input voltage	4
I_Q	No load quiescent current	vs Input voltage	5, 6
f_s	Switching frequency	vs Input voltage	7
$r_{DS(on)}$	P-Channel switch $r_{DS(on)}$	vs Input voltage	8
$r_{DS(on)}$	N-Channel rectifier switch $r_{DS(on)}$	vs Input voltage	9
	Load transient response		10
	PWM operation		11
	Power save mode operation		12
	Start-up		13

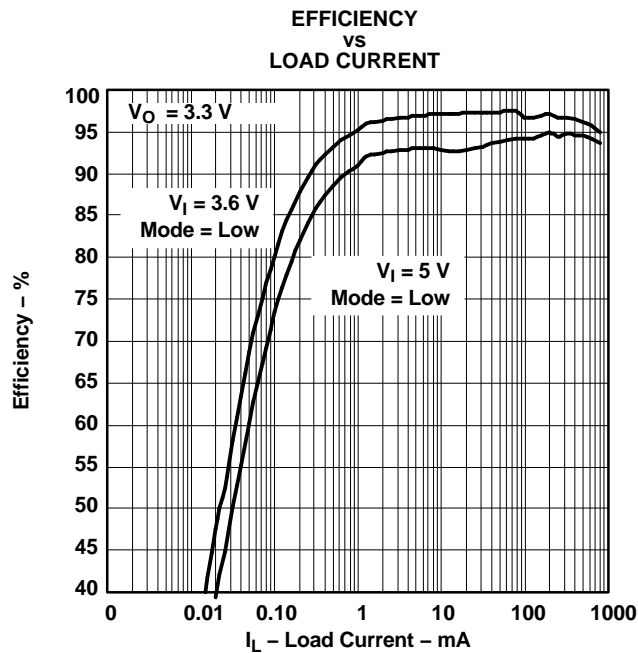


Figure 1.

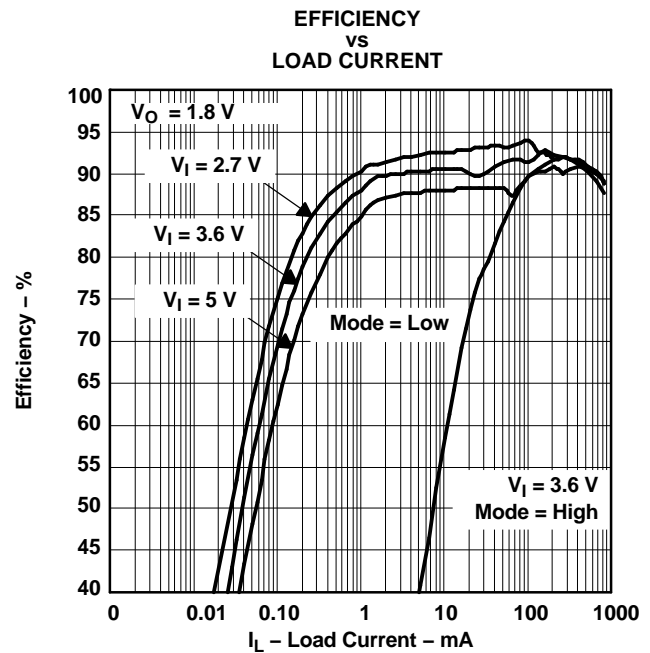
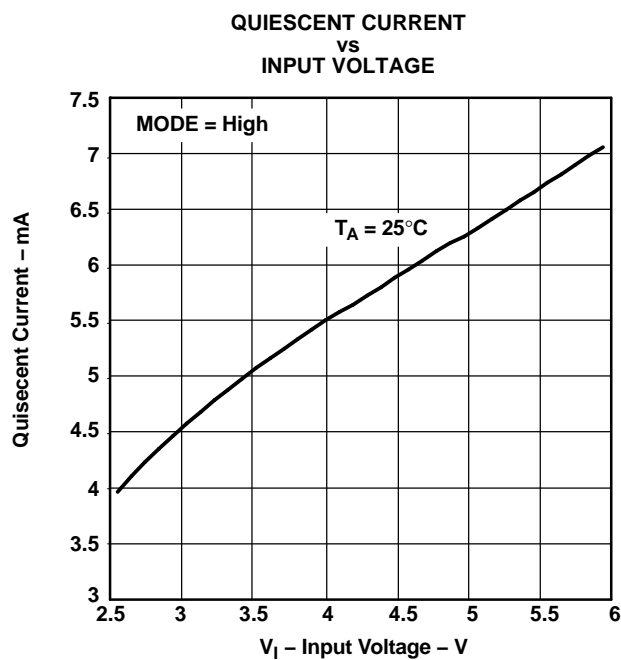
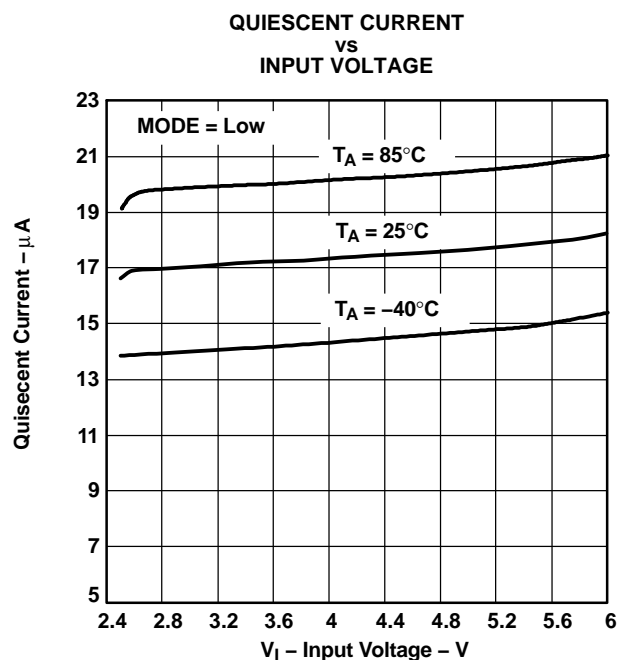
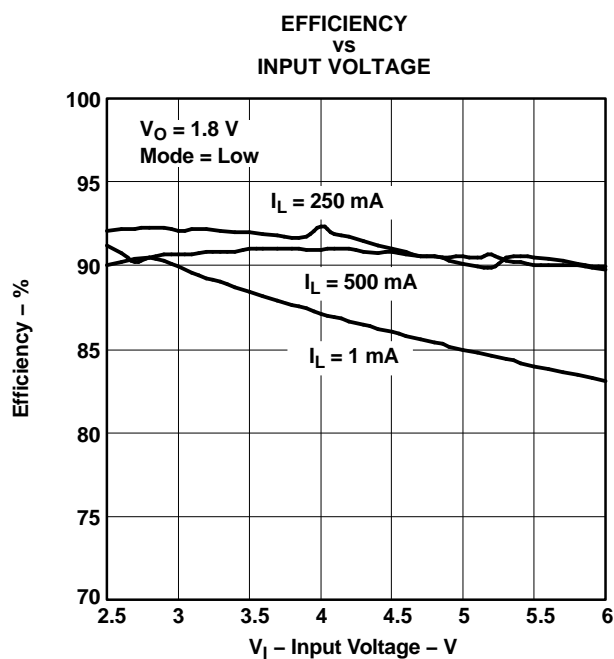
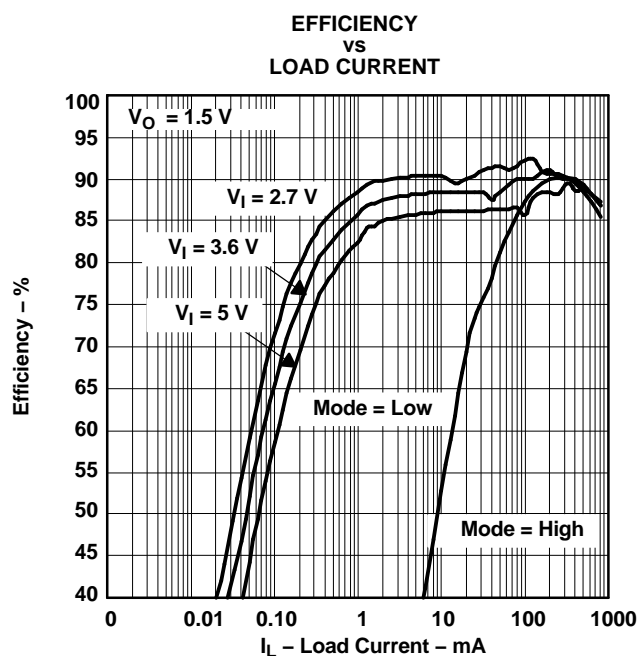


Figure 2.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

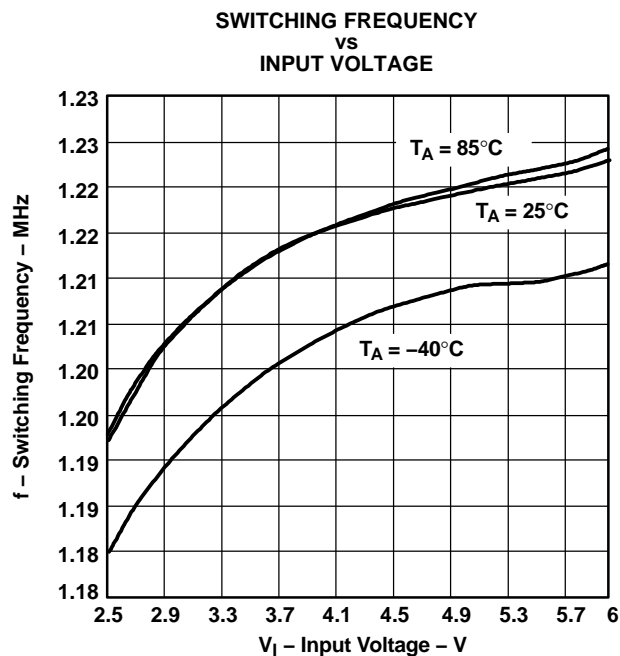


Figure 7.

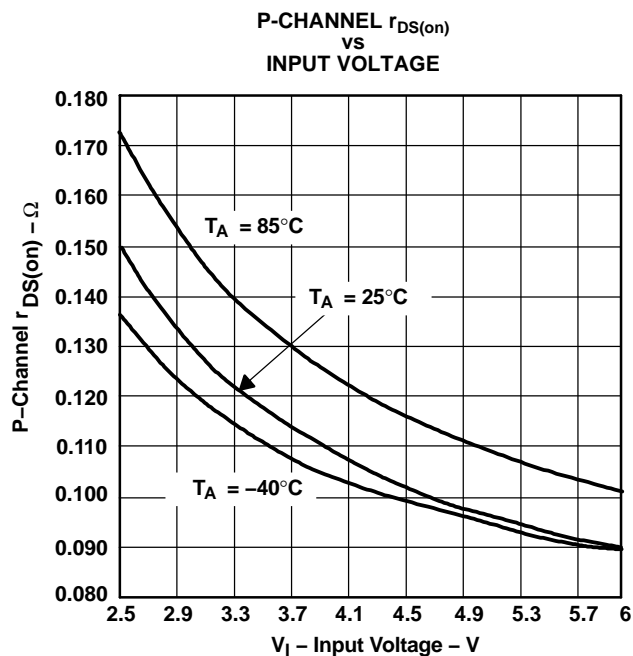


Figure 8.

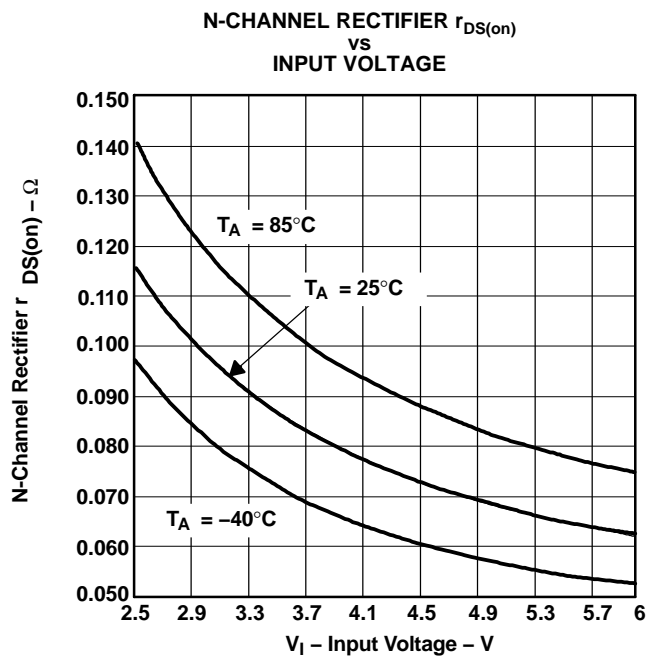


Figure 9.

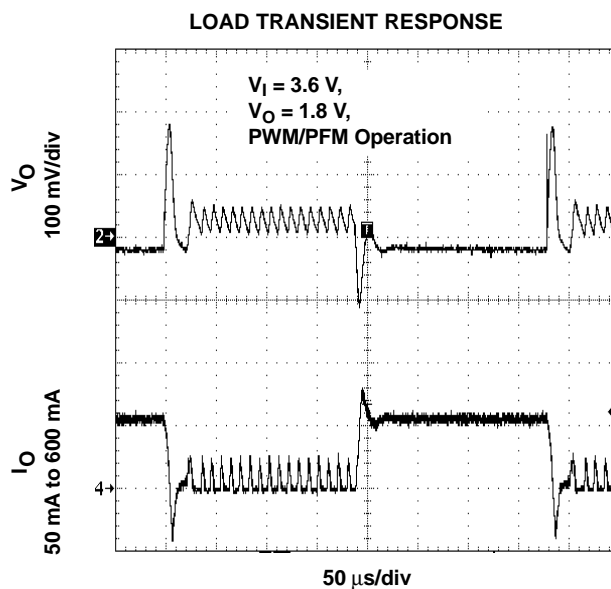


Figure 10.

TYPICAL CHARACTERISTICS (continued)

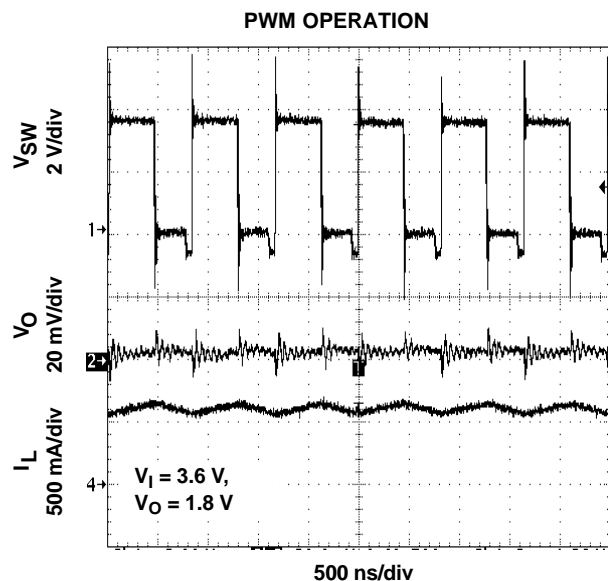


Figure 11.

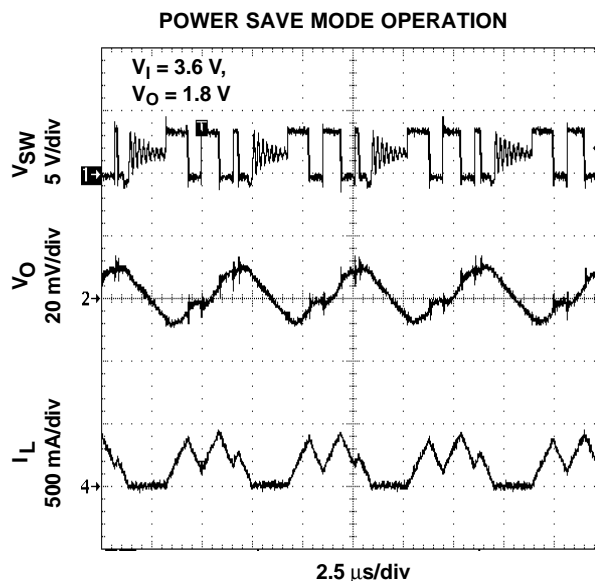


Figure 12.

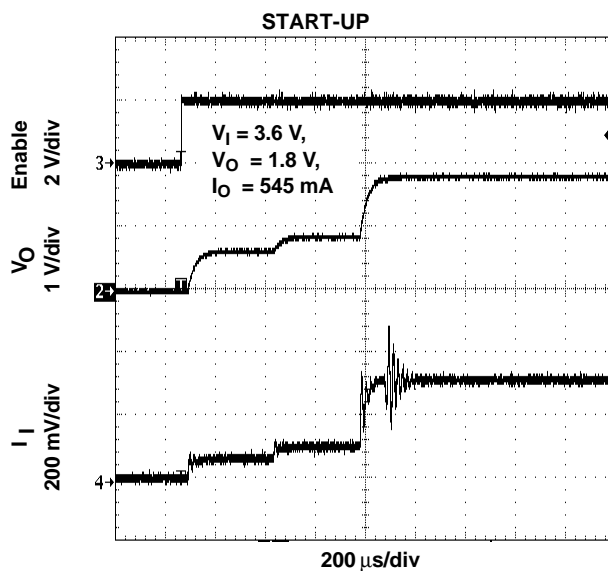


Figure 13.

DETAILED DESCRIPTION

OPERATION

The TPS62020 is a synchronous step-down converter operating with typically 1.25-MHz fixed frequency. At moderate to heavy load currents the device operates in pulse width modulation (PWM), and at light load currents the device enters power save mode operation using pulse frequency modulation (PFM). When operating in PWM mode, the typical switching frequency is 1.25 MHz with a minimum switching frequency of 1 MHz. This makes the device suitable for xDSL applications minimizing RF (radio frequency) interference.

During PWM operation the converter uses a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S) the P-channel MOSFET switch turns on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The Gm amplifier as well as the input voltage determines the rise time of the saw tooth generator, and therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter, giving a very good line and load transient regulation.

POWER SAVE MODE OPERATION

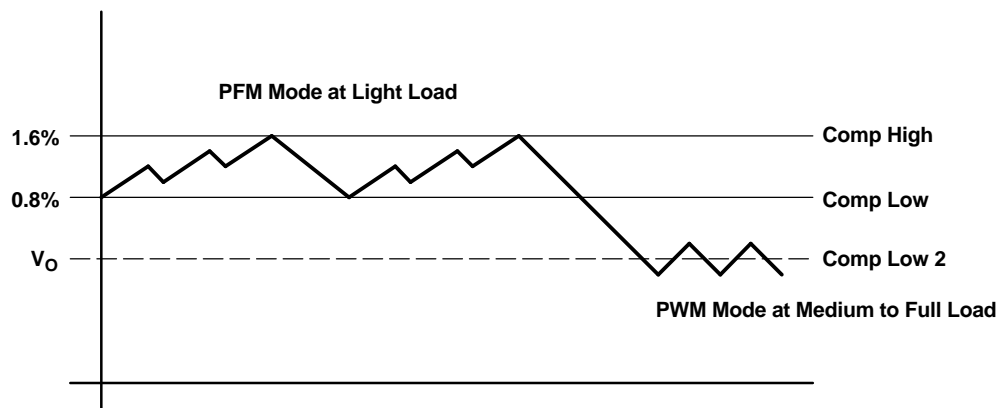
As the load current decreases, the converter enters power save mode operation. During power save mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current maintaining high efficiency.

The converter monitors the average inductor current and the device enters power save mode when the average inductor current is below the threshold. The transition point between PWM and power save mode is given by the transition current with the following equation:

$$I_{\text{transition}} = \frac{V_I}{18.66 \, \Omega} \quad (1)$$

During power save mode the output voltage is monitored with the comparator by the threshold's comp low and comp high. As the output voltage falls below the comp low threshold set to typically 0.8% above the nominal output voltage, the P-channel switch turns on. The P-channel switch remains on until the transition current Equation 1 is reached. Then the N-channel switch turns on completing the first cycle. The converter continues to switch with its normal duty cycle determined by the input and output voltage but with half the nominal switching frequency of 625-kHz typ. Thus the output voltage rises and, as soon as the output voltage reaches the comp high threshold of 1.6%, the converter stops switching. Depending on the load current, the converter switches for a longer or shorter period of time in order to deliver the energy to the output. If the load current increases and the output voltage can not be maintained with the transition current Equation 1, the converter enters PWM again. See Figure 11 and Figure 12 under the typical graphs section and Figure 14 for power save mode operation. Among other techniques this advanced power save mode method allows high efficiency over the entire load current range and a small output ripple of typically 1% of the nominal output voltage.

Setting the power save mode thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic voltage positioning achieving lower absolute voltage drops during heavy load transient changes. This allows the converter to operate with small output capacitors like 10 µF or 22 µF and still having a low absolute voltage drop during heavy load transient. Refer to Figure 14 as well for detailed operation of the power save mode.

DETAILED DESCRIPTION (continued)**Figure 14. Power Save Mode Thresholds and Dynamic Voltage Positioning**

The converter enters the fixed frequency PWM mode as soon as the output voltage falls below the comp low 2 threshold.

DYNAMIC VOLTAGE POSITIONING

As described in the power save mode operation sections before and as detailed in Figure 14 the output voltage is typically 0.8% (i.e., 1% on average) above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. In the other direction during a load transient from full load to light load the voltage overshoot is also minimized by turning on the N-Channel rectifier switch to pull the output voltage actively down.

MODE (AUTOMATIC PWM/PFM OPERATION AND FORCED PWM OPERATION)

Connecting the MODE pin of the TPS62020 to GND enables the automatic PWM and power save mode operation. The converter operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the TPS62020 MODE pin high forces the converter to operate constantly in the PWM mode even at light load currents. The advantage is the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads (see Figure 1 to Figure 3). For additional flexibility it is possible to switch from power save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the TPS6204x to the specific system requirements.

The difference between the TPS62020 and the TPS62021 is the logic level of the MODE pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin. Pulling the TPS62021 $\overline{\text{MODE}}$ pin high enables the automatic PWM and Power Save Mode.

100% DUTY CYCLE LOW DROPOUT OPERATION

The TPS62020 offers a low input to output voltage difference while still maintaining regulation with the use of the 100% duty cycle mode. In this mode, the P-Channel switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. i.e. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as:

$$V_{I \min} = V_{O \max} + I_{O \max} \times (r_{DS(on) \max} + R_L) \quad (2)$$

with:

- $I_{O(max)}$ = maximum output current plus inductor ripple current
- $r_{DS(on) \max}$ = maximum P-channel switch $r_{DS(on)}$.

DETAILED DESCRIPTION (continued)

- R_L = DC resistance of the inductor
- V_{Omax} = nominal output voltage plus maximum output voltage tolerance

SOFTSTART

The TPS62020 series has an internal softstart circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage in case a battery or a high impedance power source is connected to the input of the TPS62020.

The softstart is implemented with a digital circuit increasing the switch current in steps of typically $I_{LIM}/8$, $I_{LIM}/4$, $I_{LIM}/2$ and then the typical switch current limit of 1.1 A as specified in the electrical parameter table. The start-up time mainly depends on the output capacitor and load current, see Figure 13.

SHORT-CIRCUIT PROTECTION

As soon as the output voltage falls below 50% of the nominal output voltage, the converter switching frequency as well as the current limit is reduced to 50% of the nominal value. Since the short-circuit protection is enabled during start up the device does not deliver more than half of its nominal current limit until the output voltage exceeds 50% of the nominal output voltage. This needs to be considered in case a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature of typically 150°C is exceeded the device goes into thermal shutdown. In this mode, the P-Channel switch and N-Channel rectifier are turned off. The device continues its operation when the junction temperature falls below typically 150°C again.

ENABLE

Pulling the EN low forces the part into shutdown mode, with a shutdown current of typically 0.1 μ A. In this mode, the P-Channel switch and N-Channel rectifier are turned off and the whole device is in shut down. If an output voltage is present during shut down, which could be an external voltage source or super cap, the reverse leakage current is specified under electrical parameter table. For proper operation the enable (EN) pin must be terminated and should not be left floating.

Pulling EN high starts up the device with the softstart as described under the section Softstart.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents device misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET with undefined conditions.

APPLICATION INFORMATION

ADJUSTABLE OUTPUT VOLTAGE VERSION

When the adjustable output voltage version TPS62020 is used, the output voltage is set by the external resistor divider. See Figure 15.

The output voltage is calculated as:

$$V_O = 0.5 \text{ V} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

with $R_1 + R_2 \leq 1 \text{ M}\Omega$ and internal reference voltage V_{ref} typical = 0.5 V

$R_1 + R_2$ should not be greater than 1 M Ω because of stability reasons. To keep the operating quiescent current to a minimum, the feedback resistor divider should have high impedance with $R_1 + R_2 \leq 1 \text{ M}\Omega$. Due to this and the low reference voltage of $V_{\text{ref}} = 0.5 \text{ V}$, the noise on the feedback pin (FB) needs to be minimized. Using a capacitive divider C1 and C2 across the feedback resistors minimizes the noise at the feedback, without degrading the line or load transient performance.

C1 and C2 should be selected as:

$$C_1 = \frac{1}{2 \times \pi \times 10 \text{ kHz} \times R_1} \quad (4)$$

with:

- R_1 = upper resistor of voltage divider
- C_1 = upper capacitor of voltage divider

For C1 a value should be chosen that comes closest to the calculated result.

$$C_2 = \frac{R_1}{R_2} \times C_1 \quad (5)$$

with:

- R_2 = lower resistor of voltage divider
- C_2 = lower capacitor of voltage divider

For C2, the selected capacitor value should always be selected larger than the calculated result. For example, in Figure 15 for C2 100 pF are selected for a calculated result of $C_2 = 88.42 \text{ pF}$.

If quiescent current is not a key design parameter C1 and C2 can be omitted, and a low impedance feedback divider has to be used with $R_1 + R_2 < 100 \text{ k}\Omega$. This reduces the noise available on the feedback pin (FB) as well but increases the overall quiescent current during operation. The higher the programmed output voltage the lower the feedback impedance has to be for best operation when not using C1 and C2.

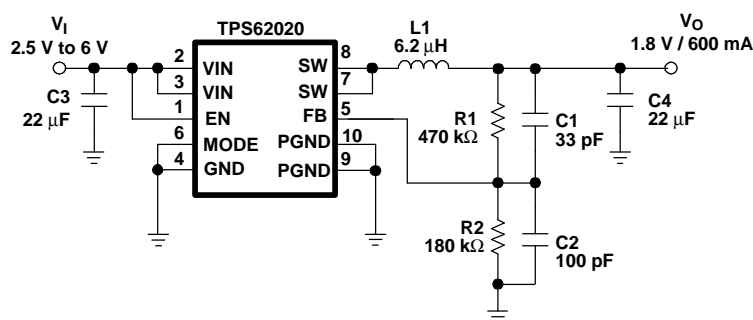


Figure 15. Adjustable Output Voltage Version

APPLICATION INFORMATION (continued)

Inductor Selection

The TPS62020 uses typically a 10-μH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. When changing inductor values, the product of the inductor value times output-capacitor value (L×C) should stay constant. For example, when reducing the inductor value, increase the output capacitor accordingly. See the application circuits in Figure 17, Figure 18, and Figure 19. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converter. Therefore an inductor with the lowest dc resistance should be selected for highest efficiency. Formula Equation 7 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with formula Equation 7. This is needed because during heavy load transient the inductor current rises above the value calculated under Equation 7.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \quad (6)$$

$$I_{L \max} = I_{O \max} + \frac{\Delta I_L}{2} \quad (7)$$

with:

- f = Switching frequency (1.25 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_{L \max}$ = Maximum inductor current

The highest inductor current occurs at maximum V_I .

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor. A more conservative approach is to select the inductor current rating just for the maximum switch current of 1.3 A for the TPS62020. Keep in mind that the core material from inductor to inductor differs and has an impact on the efficiency, especially at high switching frequencies. Refer to Table 1 and the typical applications and inductors selection.

Table 1. Inductor Selection

INDUCTOR VALUE	DIMENSIONS	COMPONENT SUPPLIER
10 μH	6,6 mm × 4,75 mm × 2,92 mm	Coilcraft DO1608C-103
10 μH	5,0 mm × 5,0 mm × 3,0 mm	Sumida CDRH4D28-100
3.3 μH	5,0 mm × 5,0 mm × 2,4 mm	Sumida CDRH4D22 3R3
6.8 μH	5,8 mm × 7,4 mm × 1,5 mm	Sumida CMD5D13 6R8

Output Capacitor Selection

The advanced fast response voltage mode control scheme of the TPS62020 allows the use of small ceramic capacitors with a typical value of 10 μF and 22 μF without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. Refer to Table 2 for component selection. If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{\text{RMS Cout}} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

At nominal load current the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + \text{ESR} \right) \quad (9)$$

Where the highest output voltage ripple occurs at the highest input voltage, V_I .

At light load currents, the device operates in power save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The input capacitor should have a minimum value of 10 μF for the TPS62020. The input capacitor can be increased without any limit for better input voltage filtering.

Table 2. Input and Output Capacitor Selection

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
10 μF	0805	Taiyo Yuden JMK212BJ106MG TDK C12012X5ROJ106K	Ceramic Ceramic
10 μF	1206	Taiyo Yuden JMK316BJ106KL TDK C3216X5ROJ106M	Ceramic
22 μF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 μF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

Layout Considerations

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths as indicated in bold in Figure 16. These traces should be routed first. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. The feedback resistor network should be routed away from the inductor and switch node to minimize noise and magnetic interference. To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces should be used for shielding. A common ground plane or a star ground as shown below should be used. This becomes very important especially at high switching frequencies of 1.25 MHz.

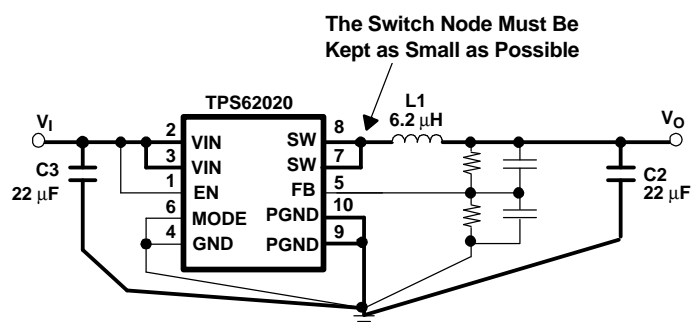


Figure 16. Layout Diagram

THERMAL INFORMATION

One of the most influential components on the thermal performance of a package is board design. In order to take full advantage of the heat dissipating abilities of the PowerPAD™ packages, a board should be used that acts similar to a heat sink and allows for the use of the exposed (and solderable), deep downset pad. For further information please refer to Texas Instruments application note (SLMA002) *PowerPAD Thermally Enhanced Package*.

The PowerPAD™ of the 10-pin MSOP package has an area of 1,52 mm × 1,79 mm (±0,05 mm) and must be soldered to the PCB to lower the thermal resistance. Thermal vias to the next layer further reduce the thermal resistance.

TYPICAL APPLICATIONS

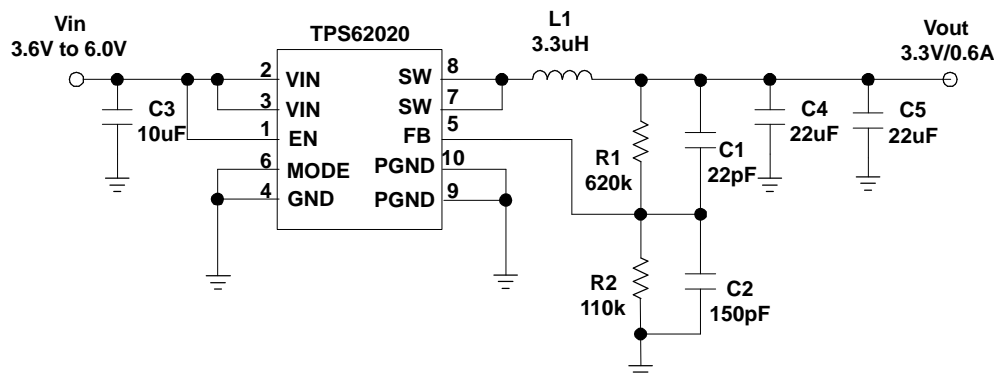


Figure 17. Li-Ion to 3.3 V With Improved Load Transient Response

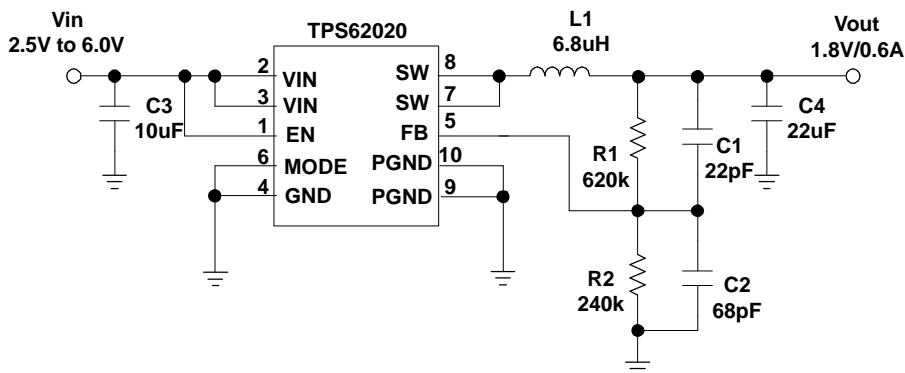


Figure 18. 1.8 V Output Using 6.8 μ H Inductor

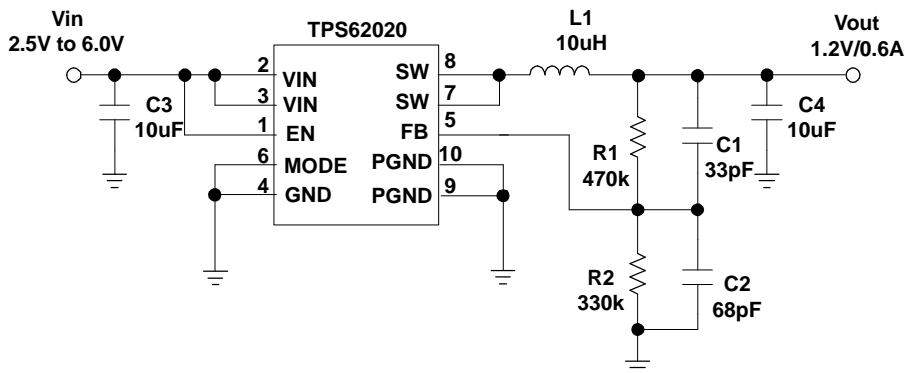
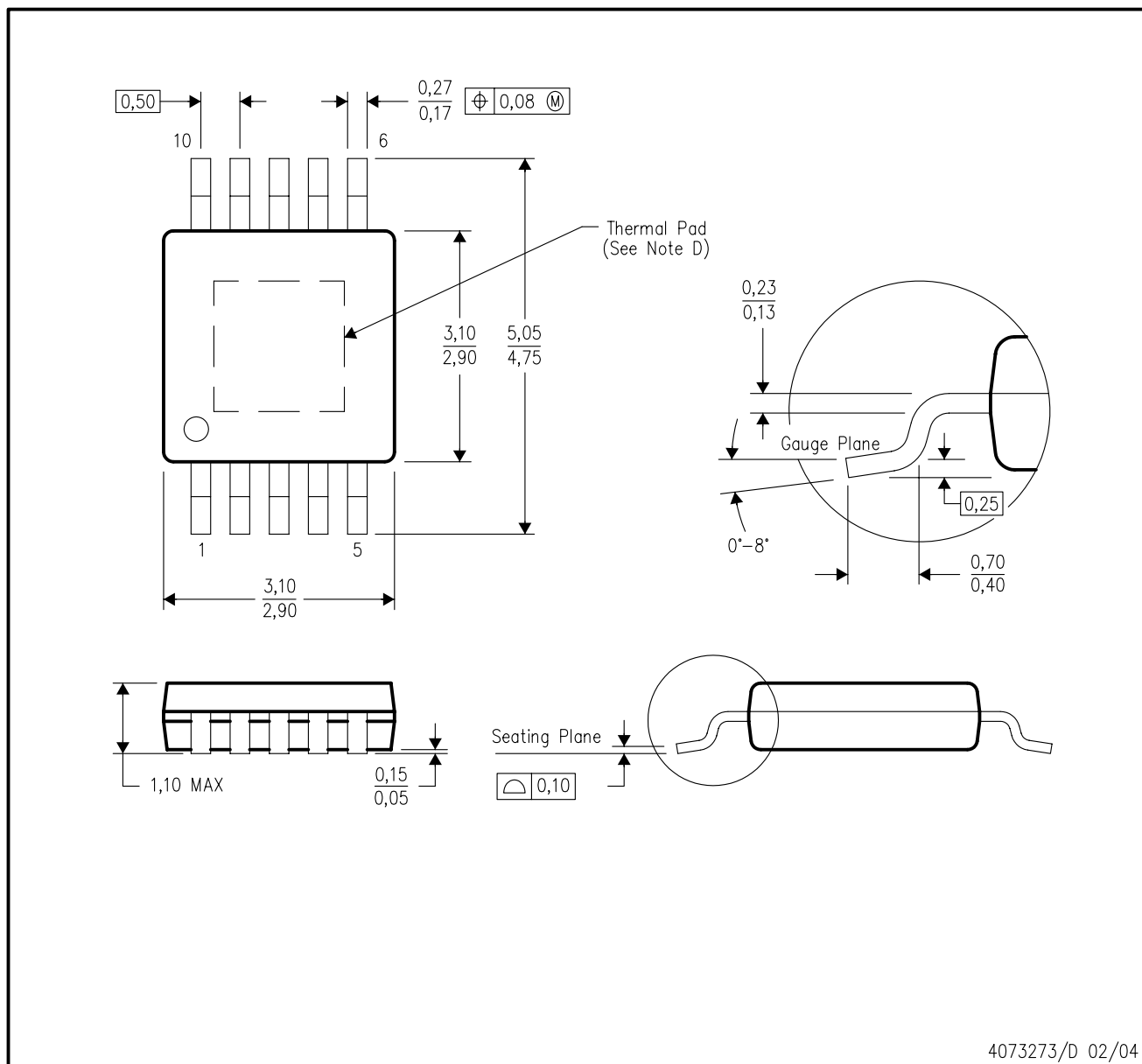


Figure 19. 1.2 V Output Using 10 μ H Inductor

DGQ (S-PDSO-G10)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



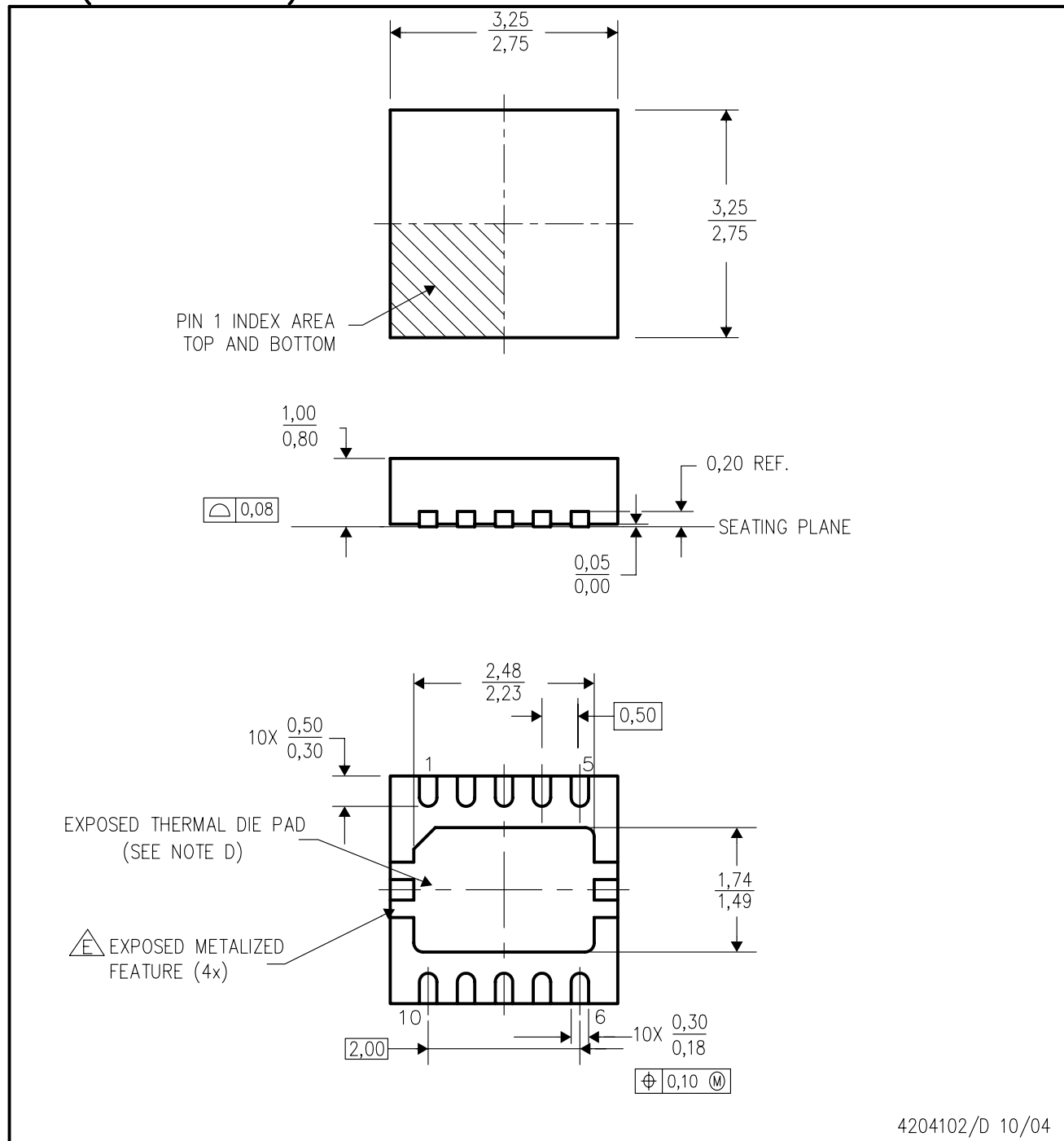
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-187 variation BA-T.

PowerPAD is a trademark of Texas Instruments.

DRC (S-PDSO-N10)

CUSTOM DEVICE

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
- E. Metalized features are supplier options and may not be on the package.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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