



## GENERAL DESCRIPTION

The SM5221-001/002 is an infrared remote control encoder LSI utilizing CMOS technology. The transmission code consists of "leader pulse", "16 bit customer code", and "16 bit data code". Using Micro-processors for decoder, various applications can be realized.

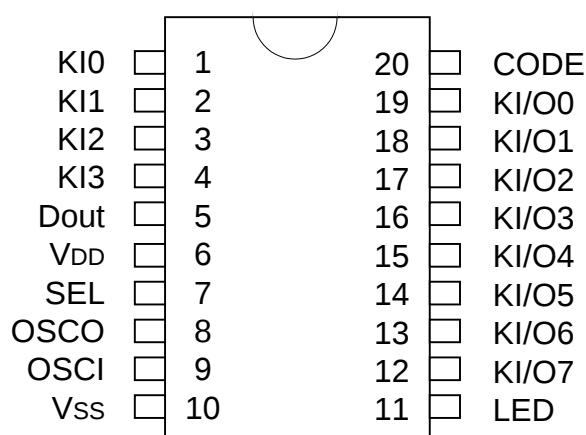
## FEATURES

- \* Low voltage operation ..... VDD=2.0 to 3.3V
- \* Low power consumption ..... IDD < 1 $\mu$ A at standby mode
- \* 32 function keys and 3 double action keys
- \* 64 + 6 function codes are available.  
(Using SEL terminal)
- \* 65536 customer codes can be selected.  
(Using external R, Diode-SM5024A or internal MASK ROM-SM5024B)
- \* 20pin SOP or DIP

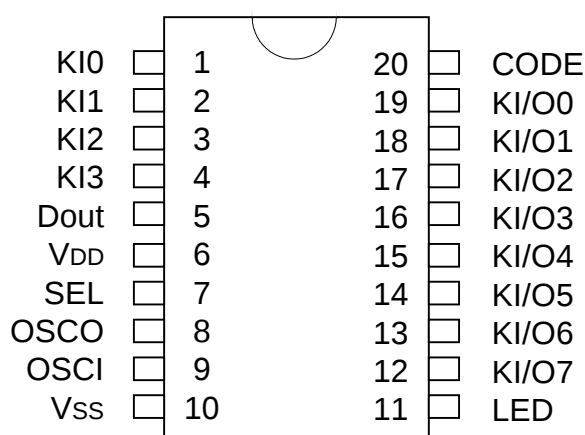
## APPLICATIONS

- \* Audio Remote Control
- \* Video Remote Control
- \* Consumer Product Remote Control

## PIN ASSIGNMENTS (TOP VIEW)



20 PIN DIP IN 300MIL



20 PIN SOP IN 300MIL



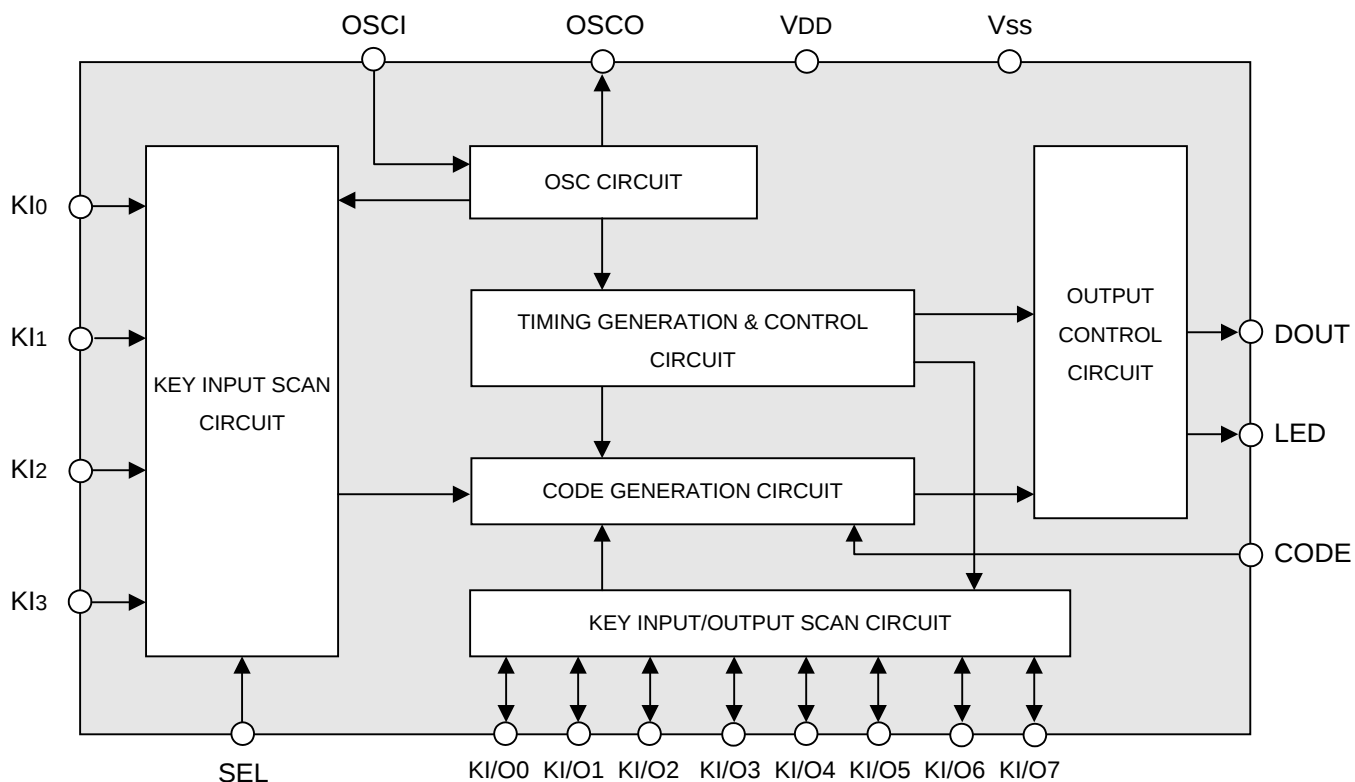
## PIN DESCRIPTION

| No. | Pin Name | I / O | Function                             |
|-----|----------|-------|--------------------------------------|
| 1   | KI0      | I     | Scan Key Input 0<br>With Pull Low    |
| 2   | KI1      | I     | Scan Key Input 1<br>With Pull Low    |
| 3   | KI2      | I     | Scan Key Input 2<br>With Pull Low    |
| 4   | KI3      | I     | Scan Key Input 3<br>With Pull Low    |
| 5   | DOUT     | O     | Remote Output                        |
| 6   | VDD      | POWER | Postive Power<br>Supply              |
| 7   | SEL      | I     | Data Select                          |
| 8   | OSCO     | O     | Oscillator Output                    |
| 9   | OSCI     | I     | Oscillator Input                     |
| 10  | VSS      | POWER | Negative Power<br>Supply (substrate) |
| 11  | LED      | O     | Indicator For<br>Transmission        |
| 12  | KI/O7    | I / O | Key Scan 7                           |
| 13  | KI/O6    | I / O | Key Scan 6                           |
| 14  | KI/O5    | I / O | Key Scan 5                           |
| 15  | KI/O4    | I / O | Key Scan 4                           |
| 16  | KI/O3    | I / O | Key Scan 3                           |
| 17  | KI/O2    | I / O | Key Scan 2                           |
| 18  | KI/O1    | I / O | Key Scan 1                           |
| 19  | KI/O0    | I / O | Key Scan 0                           |
| 20  | CODE     | I / O | Customer Code<br>Select Input        |

| Pin Name | No. | I / O | Function                             |
|----------|-----|-------|--------------------------------------|
| KI0      | 1   | I     | Scan Key Input 0<br>With Pull Low    |
| KI1      | 2   | I     | Scan Key Input 1<br>With Pull Low    |
| KI2      | 3   | I     | Scan Key Input 2<br>With Pull Low    |
| KI3      | 4   | I     | Scan Key Input 3<br>With Pull Low    |
| KI/O0    | 19  | I / O | Key Scan 0                           |
| KI/O1    | 18  | I / O | Key Scan 1                           |
| KI/O2    | 17  | I / O | Key Scan 2                           |
| KI/O3    | 16  | I / O | Key Scan 3                           |
| KI/O4    | 15  | I / O | Key Scan 4                           |
| KI/O5    | 14  | I / O | Key Scan 5                           |
| KI/O6    | 13  | I / O | Key Scan 6                           |
| KI/O7    | 12  | I / O | Key Scan 7                           |
| DOUT     | 5   | O     | Remote Output                        |
| SEL      | 7   | I     | Data Select                          |
| LED      | 11  | O     | Indicator For<br>Transmission        |
| CODE     | 20  | I / O | Customer Code<br>Select Input        |
| OSCO     | 8   | O     | Oscillator Output                    |
| OSCI     | 9   | I     | Oscillator Input                     |
| VDD      | 6   | POWER | Postive Power<br>Supply              |
| VSS      | 10  | POWER | Negative Power<br>Supply (substrate) |



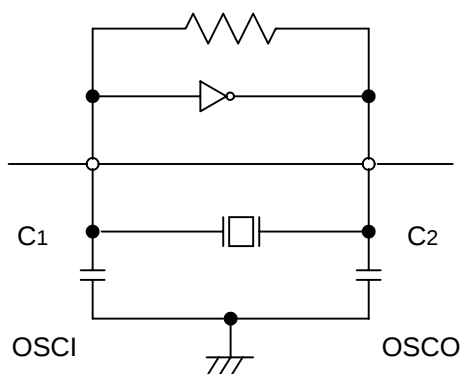
## BLOCK DIAGRAM



## FUNCTION DESCRIPTION

### (1) Oscillation

The SM5221-001/002 oscillation circuit is designed for use of a 400 kHz or 500 kHz ceramic resonator, but there may be mutual influence between variations in the IC and ceramic resonator resulting in abnormal oscillation. The oscillation circuit starts to operate when a key is depressed.



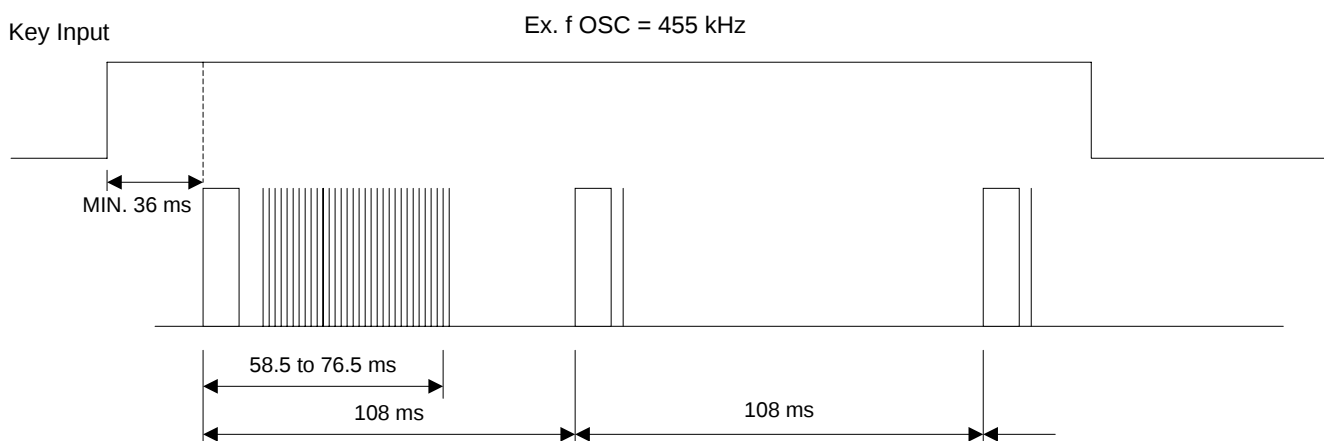


## (2) Key Scan

A pull-down resistor is inserted

keys are depressed simultaneously, transmission is disabled by the multi-depression prevention circuit.

When a key is depressed, reading of the custom code and key data code is started, and DOUT output begins 36 ms later, so that if the key is being depressed during this 36 ms interval one transmission is performed. If a key is held down for 108 ms or longer, consecutive transmissions of the leader code only are performed while the key is depressed.



## (3) Data Code D7 Control

Data code D7 can be controlled by this pin, allowing 64 kinds of data to be transmitted.

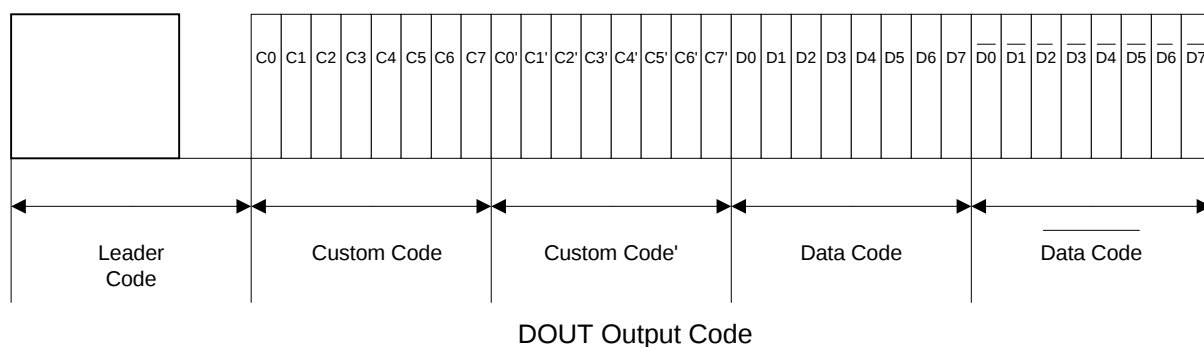
D7 is set to "0" by connecting the SEL pin to VDD, and to "1" by connecting the SEL pin to VSS. As the input of this pin is high-impedance, it must be connected to either VDD or VSS.



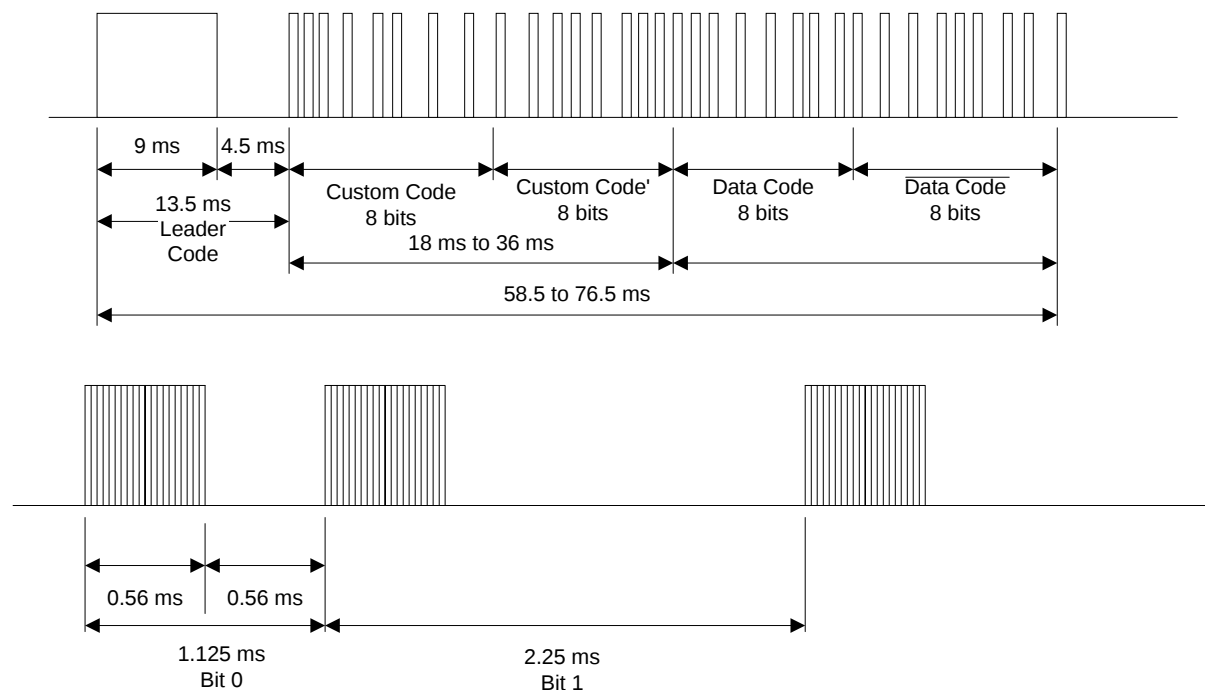
## TRANSMISSION CODE

### (1) DOUT Output

The transmission code consists of a leader code, 16-bit custom code, and 8-bit data code. The inverse code of the data code is also sent simultaneously, giving a total configuration of 32 bits per transmission.

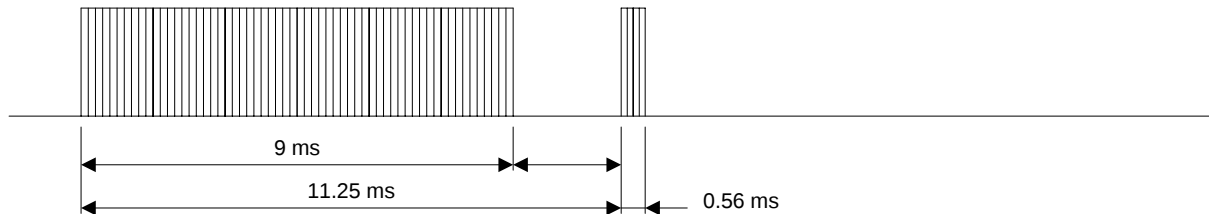


The leader code consists of a 9 ms carrier waveform plus a 4.5 ms OFF waveform, and is used as the leader for the following code. The code uses the PPM (Pulse Position Modulation) method, with "1" and "0" differentiated by the time between pulses reference following diagram. Each code consists of 8 bits, and simultaneous transmission of the inverse code.

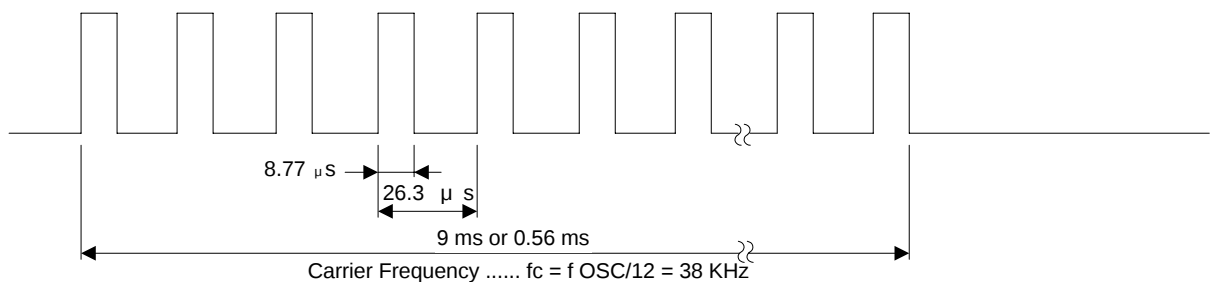




## Continuous Code



## Carrier

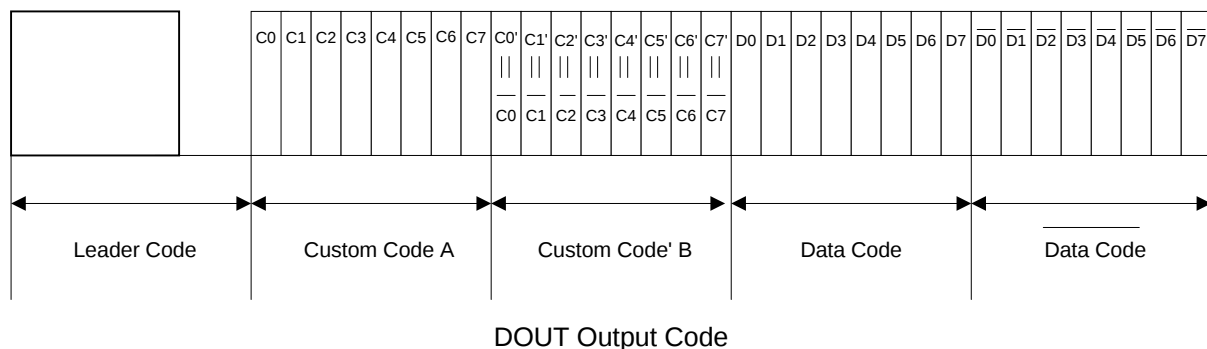


## (2) Custom Code Extension

The custom code can be set by the diodes connected to the CODE pin and the KI/O pins. Connecting the CODE pin and KI/O pins via diodes gives a corresponding custom code of "1", while no connection gives "0".

The above output codes can be obtained

further extend the number of custom codes, 200 k $\Omega$  pull up resistors are added to pins KI/O0 through KI/O7, and the bit corresponding to a pin from among the custom code' outputs is output without being inverted.



\*: Pull-up resistor added to pins KI/O0 and KI/O2.  
C0 and C2 output without inversion (non-inverted bits).



### (3) Custom Code

The DOUT output custom code can be set in any of 65536 ways by means of the diodes attached to the CODE (Custom Code Select) pin and the KI/O pins and the pull-up resistors attached to the KI/O pins. When a code other than code 00000000 (no diode connection) is used.

### (4) Custom Code Mask ROM Specification

The custom code can also be set by mask ROM. When the mask ROM specification is used the custom code can be set without the connection of external diodes and resistors, and by combining external diodes and resistors with mask ROM it is possible to output a code with different contents from those set by the mask ROM. When mask ROM specification is used, (Ver. I) or (Ver. II) can be selected.

|         | Custom Code High-Order<br>8 Bits                                                                                                                                                             | Custom Code' Low-Order<br>8 Bits                                                                      |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| Ver. I  | Determined by logical OR of internal ROM1 and external diode positions.                                                                                                                      | Determined by logical OR of internal ROM2 and external pull-up resistor positions                     |
| Ver. II | C0, C1, C2:<br>Determined by wiring one of pins KI/O0 thru KI/O7 to CCS pin.<br>C3 thru C7:<br>Determined by internal ROM3 and absence/presence of KI/O6 & KI/O7 external pull-up resistors. | Determined by logical OR of internal ROM2 and external pull-up resistor (KI/O0 thru KI/O5) positions. |

\* Standard product SM5221-001/002 uses the Ver. I specification

Internal ROM is set as follows:

| ROM 1<br>Custom code high-order 8 bits |    |    |    |    |    |    |    | ROM 2<br>Custom code' low-order 8 bits |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|----------------------------------------|----|----|----|----|----|----|----|
| 0                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                                      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| C0                                     | C1 | C2 | C3 | C4 | C5 | C6 | C7 | C0                                     | C1 | C2 | C3 | C4 | C5 | C6 | C7 |

\* Standard product SM5221-002 uses the Ver. II specification.



Internal ROM is set as follows:

ROM 3

C7, C6, C5, C4, C3 of Custom Code High-Order 8 Bits

Pull-Up resistor

| ROM3      | C7 | C6 | C5 | C4 | C3 | KI / O6 | KI / O7 |
|-----------|----|----|----|----|----|---------|---------|
| ROM 3 - 0 | 0  | 0  | 0  | 0  | 0  | No      | No      |
| ROM 3 - 1 | 1  | 0  | 0  | 1  | 1  | No      | Yes     |
| ROM 3 - 2 | 1  | 0  | 0  | 0  | 0  | Yes     | No      |
| ROM 3 - 3 | 1  | 1  | 1  | 0  | 1  | Yes     | Yes     |

ROM2

Custom code' low-order 8 bits

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

C0' C1' C2' C3' C4' C5' C6' C7'



(Ver. I)

Internal custom code ROM1 and ROM2 (total (ROM1) corresponding to the external diodes, and 8 bits the part (ROM2) corresponding to the external pull-up resistors.

(Ver. II)

With Ver. II, the CODE pin does not have the function of reading the external diodes. Internal custom code ROM2 and ROM3 (total 28 bits) are effective, with 20 bits being the part (ROM3) for setting the 4 channels of custom code C7, C6, C5, C4 and C3 as 5 bits each, and 8 bits being the part (ROM2) corresponding to the external pull-up resistors (excluding KI/O6 and KI/O7). With Ver. II 0/1 allocation to C2, C1 and C0 of the custom code high-order bits is set as shown in the following table according to the pin connection status of KI/O0 through KI/O7.

| CCS-  | C2 | C1 | C0 |
|-------|----|----|----|
| KI/O0 | 0  | 0  | 0  |
| KI/O1 | 0  | 0  | 1  |
| KI/O2 | 0  | 1  | 0  |
| KI/O3 | 0  | 1  | 1  |
| KI/O4 | 1  | 0  | 0  |
| KI/O5 | 1  | 0  | 1  |
| KI/O6 | 1  | 1  | 0  |
| KI/O7 | 1  | 1  | 1  |

When CODE pin is open  
(C2 C1 C0) = ( 0, 0, 0)



## KEY DATA CODE

| Key | Connection |     |     |     |       | Data Code |    |    |    |    |    |    |     |
|-----|------------|-----|-----|-----|-------|-----------|----|----|----|----|----|----|-----|
|     | KI0        | KI1 | KI2 | KI3 | KI/O  | D0        | D1 | D2 | D3 | D4 | D5 | D6 | D7  |
| K 1 | *          |     |     |     | KI/O0 | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0/1 |
| K 2 |            | *   |     |     |       | 1         | 0  | 0  | 0  | 0  | 0  | 0  | 0/1 |
| K 3 |            |     | *   |     |       | 0         | 1  | 0  | 0  | 0  | 0  | 0  | 0/1 |
| K 4 |            |     |     | *   |       | 1         | 1  | 0  | 0  | 0  | 0  | 0  | 0/1 |
| K 5 | *          |     |     |     | KI/O1 | 0         | 0  | 1  | 0  | 0  | 0  | 0  | 0/1 |
| K 6 |            | *   |     |     |       | 1         | 0  | 1  | 0  | 0  | 0  | 0  | 0/1 |
| K 7 |            |     | *   |     |       | 0         | 1  | 1  | 0  | 0  | 0  | 0  | 0/1 |
| K 8 |            |     |     | *   |       | 1         | 1  | 1  | 0  | 0  | 0  | 0  | 0/1 |
| K 9 | *          |     |     |     | KI/O2 | 0         | 0  | 0  | 1  | 0  | 0  | 0  | 0/1 |
| K10 |            | *   |     |     |       | 1         | 0  | 0  | 1  | 0  | 0  | 0  | 0/1 |
| K11 |            |     | *   |     |       | 0         | 1  | 0  | 1  | 0  | 0  | 0  | 0/1 |
| K12 |            |     |     | *   |       | 1         | 1  | 0  | 1  | 0  | 0  | 0  | 0/1 |
| K13 | *          |     |     |     | KI/O3 | 0         | 0  | 1  | 1  | 0  | 0  | 0  | 0/1 |
| K14 |            | *   |     |     |       | 1         | 0  | 1  | 1  | 0  | 0  | 0  | 0/1 |
| K15 |            |     | *   |     |       | 0         | 1  | 1  | 1  | 0  | 0  | 0  | 0/1 |
| K16 |            |     |     | *   |       | 1         | 1  | 1  | 1  | 0  | 0  | 0  | 0/1 |
| K17 | *          |     |     |     | KI/O4 | 0         | 0  | 0  | 0  | 1  | 0  | 0  | 0/1 |
| K18 |            | *   |     |     |       | 1         | 0  | 0  | 0  | 1  | 0  | 0  | 0/1 |
| K19 |            |     | *   |     |       | 0         | 1  | 0  | 0  | 1  | 0  | 0  | 0/1 |
| K20 |            |     |     | *   |       | 1         | 1  | 0  | 0  | 1  | 0  | 0  | 0/1 |
| K21 | *          |     |     |     | KI/O5 | 0         | 0  | 1  | 0  | 1  | 0  | 0  | 0/1 |
| K22 |            | *   |     |     |       | 1         | 0  | 1  | 0  | 1  | 0  | 0  | 0/1 |
| K23 |            |     | *   |     |       | 0         | 0  | 1  | 0  | 1  | 0  | 0  | 0/1 |
| K24 |            |     |     | *   |       | 1         | 0  | 1  | 0  | 1  | 0  | 0  | 0/1 |
| K25 | *          |     |     |     | KI/O6 | 0         | 0  | 0  | 1  | 1  | 0  | 0  | 0/1 |
| K26 |            | *   |     |     |       | 1         | 0  | 0  | 1  | 1  | 0  | 0  | 0/1 |
| K27 |            |     | *   |     |       | 0         | 1  | 0  | 1  | 1  | 0  | 0  | 0/1 |
| K28 |            |     |     | *   |       | 1         | 1  | 0  | 1  | 1  | 0  | 0  | 0/1 |
| K29 | *          |     |     |     | KI/O7 | 0         | 0  | 1  | 1  | 1  | 0  | 0  | 0/1 |
| K30 |            | *   |     |     |       | 1         | 0  | 1  | 1  | 1  | 0  | 0  | 0/1 |
| K31 |            |     | *   |     |       | 0         | 1  | 1  | 1  | 1  | 0  | 0  | 0/1 |
| K32 |            |     |     | *   |       | 1         | 1  | 1  | 1  | 1  | 0  | 0  | 0/1 |



## DOUBLE KEY OPERATION

When more than two keys except K21 + K22, K21 + K23 and K21 + K24 are depressed at the same time, the transmission output stops.

Double key operation is useful for tape deck recording operation.

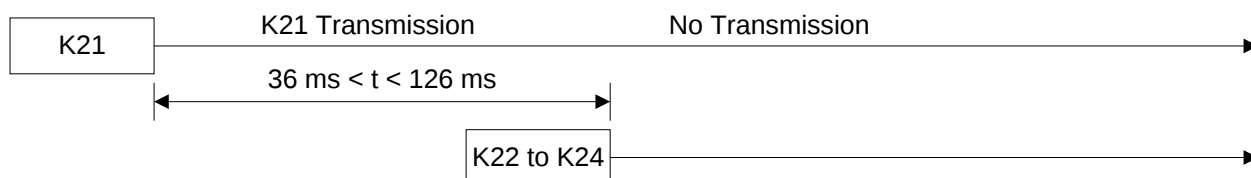
Double key operation form are following.

| KEY       | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7  |
|-----------|----|----|----|----|----|----|----|-----|
| K21 + K22 | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 0/1 |
| K21 + K23 | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 0/1 |
| K21 + K24 | 1  | 1  | 1  | 0  | 1  | 1  | 0  | 0/1 |

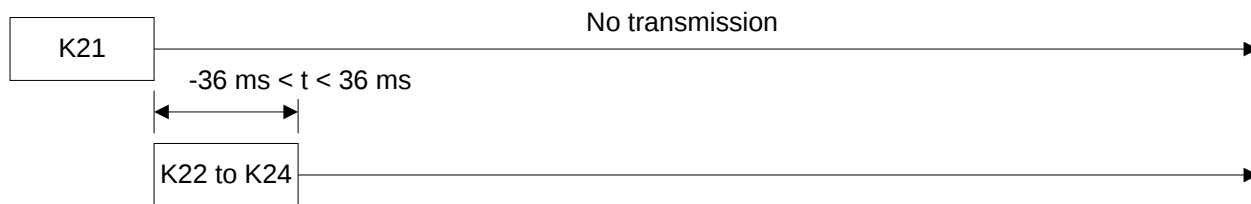
### (a) Operation



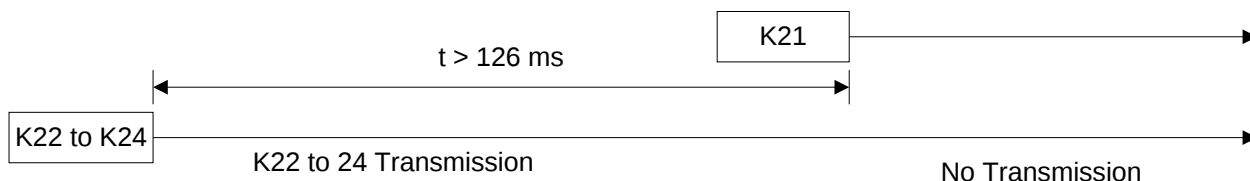
### (b) No operation



### (c) No operation



### (d) No operation





## CUSTOMER CODE ROM FORMAT

This LSI has customer code table ROM on the chip. So user can generate customer codes without external parts.

The customer code ROM format is following.

| Ver.1 or 2 SEL |   | C7  | C6  | C5  | C4  | C3  | C2  | C1  | C0  |          |        |
|----------------|---|-----|-----|-----|-----|-----|-----|-----|-----|----------|--------|
|                |   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |          |        |
| ROM 1          |   | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | ROM PULL | SEL UP |
| ROM 2          |   | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | K/IO6    | K/IO7  |
| ROM 3          | 0 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0   | 0   | 0   | NO       | NO     |
|                | 1 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0   | 0   | 0   | NO       | YES    |
|                | 2 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0   | 0   | 0   | YES      | NO     |
|                | 3 | 1/0 | 1/0 | 1/0 | 1/0 | 1/0 | 0   | 0   | 0   | YES      | YES    |

- 1) Ver. 1 or Ver. 2 selection ..... Ver. 1 = 01H, Ver. 2 = 02H
- 2) When a user selects Ver. 1, ROM1 is available for the customer code (C7 to C0) election.
- 3) ROM2 is available for the customer code' (C7' to C0') selection.
- 4) When a user selects Ver. 2, ROM3 is available for the customer code (C7 to C3) selection. And a user can select ROM3-0, ROM3-1, ROM3-2 or ROM3-3 by the KI/O6 and KI/O7 pull up resistances.



**ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)**

| Characteristic        | Symbol | Value       | Unit |
|-----------------------|--------|-------------|------|
| Supply Voltage        | VDD    | 6.0         | V    |
| Input Voltage         | VIN    | -0.3 to VDD | V    |
| Power Dissipation     | Pd     | 250         | mW   |
| Operating Temperature | Topt   | -20 to +75  |      |
| Storage Temperature   | Tstg   | -40 to +125 |      |

**RECOMMENDED OPERATING CONDITIONS**

| Characteristic                           | Symbol | Min. | Typ. | Max. | Unit |
|------------------------------------------|--------|------|------|------|------|
| Supply Voltage                           | VDD    | 2.0  | 3.0  | 3.3  | V    |
| Oscillation Frequency                    | fosc   | 400  | 455  | 500  | KHz  |
| Input Voltage                            | VIN    | 0    |      | VDD  | V    |
| Custom code select<br>Pull up Resistance | Rup    | 160  | 200  | 240  | KΩ   |



**ELECTRICAL CHARACTERISTICS (Ta = 25 , VDD = 3.0 V)**

| Characteristic                 | Symbol | Min.    | Typ. | Max.   | Unit | Conditions            |
|--------------------------------|--------|---------|------|--------|------|-----------------------|
| Supply Voltage                 | VDD    | 2.0     | 3.0  | 3.3    | V    |                       |
| Current Consumption 1          | IDD1   |         | 0.1  | 1.0    | mA   | f osc = 455 kHz       |
| Current Consumption 2          | IDD2   |         |      | 1.0    | μA   | f osc = STOP          |
| DOUT High Level Output Current | IOH1   |         | -8.0 |        | mA   | Vo = 1.5 V            |
| DOUT Low Level Output Current  | IOL1   |         | 30   |        | μA   | Vo = 0.3 V            |
| LED High Level Output Current  | IOH2   | -15     | -30  |        | μA   | Vo = 2.7 V            |
| LED Low Level Output Current   | IOL2   | 1       | 1.5  |        | mA   | Vo = 0.3 V            |
| KI High Level Input Current    | IiH1   | 5       |      | 30     | μA   | VIN = 3.0 V           |
| KI Low Level Input Current     | IiL1   |         |      | -0.2   | μA   | VIN = 0 V             |
| KI High Level Input Voltage    | ViH1   | 0.7 VDD |      | VDD    | V    |                       |
| KI Low Level Input Voltage     | ViL1   | 0       |      | 0.3VDD | V    |                       |
| KI/O High Level Input Voltage  | ViH2   | 1.3     |      | VDD    | V    |                       |
| KI/O Low Level Input Voltage   | ViL2   | 0       |      | 0.4    | V    |                       |
| KI/O High Level Input Current  | IiH2   | 2       |      | 7      | μA   | VIN = 3.0 V           |
| KI/O Low Level Input Current   | IiL2   |         |      | -0.2   | μA   | VIN = 0 V             |
| KI/O High Level Output Current | IOH3   | 1.0     |      | 2.5    | mA   | Vo = 2.5 V            |
| KI/O Low Level Output Current  | IOL3   | 35      |      | 100    | μA   | Vo = 1.7 V            |
| CODE High Level Input Voltage  | ViH3   | 1.1     |      |        | V    |                       |
| CODE High Level Input Current  | IiH3   |         |      | 0.2    | μA   | Pull up VIN = 3.0 V   |
| CODE Low Level Input Current   | IiL3   | -3      |      | -10    | μA   | Pull up VIN = 0 V     |
| CODE High Level Input Current  | IiH4   | 5       |      | 30     | μA   | Pull down VIN = 3.0 V |
| CODE Low Level Input Current   | IiL4   |         |      | -0.2   | μA   | Pull down VIN = 0 V   |



## APPLICATION CIRCUIT

