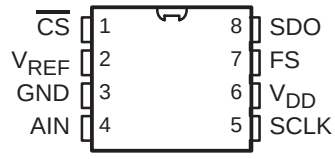
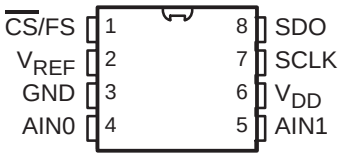
- **Maximum Throughput . . . 400 KSPS**
- **INL/DNL: ±1 LSB Max, SINAD: 72 dB, f_i = 20 kHz, SFDR: 85 dB, f_i = 20 kHz**
- **SPI/DSP-Compatible Serial Interfaces With SCLK up to 20 MHz**
- **Single 5 V Supply**
- **Rail-to-Rail Analog Input With 500 kHz BW**
- **Three Options Available:**
  - **TLC2551 – Single Channel Input**
  - **TLC2552 – Dual Channels With Autosweep**
  - **TLC2555 – Single Channel With Pseudo-Differential Input**
- **Optimized DSP Mode – Requires FS Only**
- **Low Power With Autopower Down**
  - **Operating Current : 3.5 mA**
  - **Autopower Down: 8 μA**
- **Small 8-Pin MSOP and SOIC Packages**

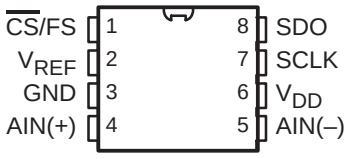
PACKAGE TOP VIEW
TLC2551



TLC2552



TLC2555



description

The TLC2551/2552/2555 are a family of high performance, 12-bit, low power, miniature 1.5 μs, CMOS analog-to-digital converters (ADC). The TLC255x family uses a 5 V supply. Devices are available with single, dual, or single pseudo-differential inputs. The TLC2551 has a 3-state output chip select ($\overline{CS}$), serial output clock (SCLK), and serial data output (SDO) that provides a direct 3-wire interface to the serial port of most popular host microprocessors (SPI interface). When interfaced with a DSP, a frame sync signal (FS) is used to indicate the start of a serial data frame. The TLV2552/55 have a shared $\overline{CS}$/FS terminal.

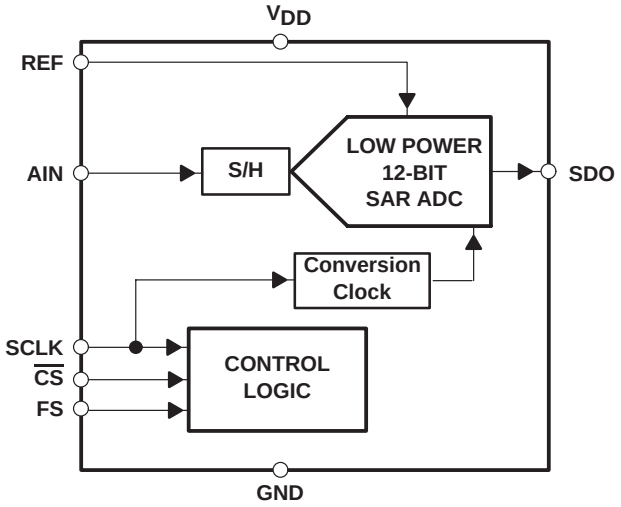
TLC2551/2/5 are designed to operate with very low power consumption. The power saving feature is further enhanced with an autopower-down mode. This product family features a high-speed serial link to modern host processors with SCLK up to 20 MHz. TLC255x family uses the SCLK as the conversion clock, thus providing synchronous operation allowing a minimum conversion time of 1.5 μs using 20 MHz SCLK.

AVAILABLE OPTIONS

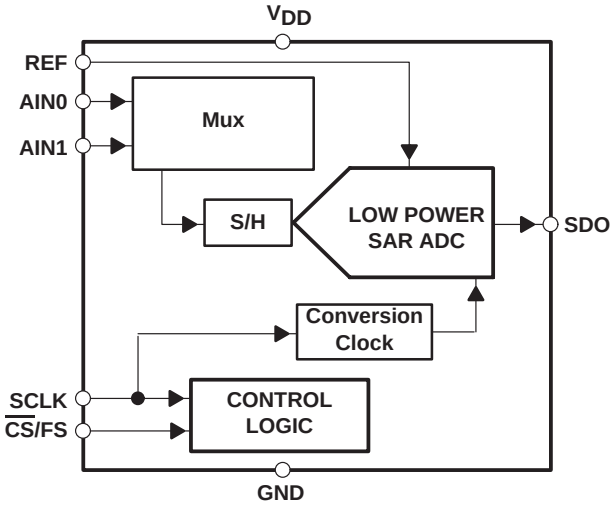
T_A	PACKAGED DEVICES	
	8-MSOP (DGK)	8-SOIC (D)
0°C to 70°C	TLC2551CDGK	
	TLC2552CDGK	
	TLC2555CDGK	
–40°C to 85°C	TLC2551IDGK	TLC2551ID
	TLC2552IDGK	TLC2552ID
	TLC2555IDGK	TLC2555ID

functional block diagram

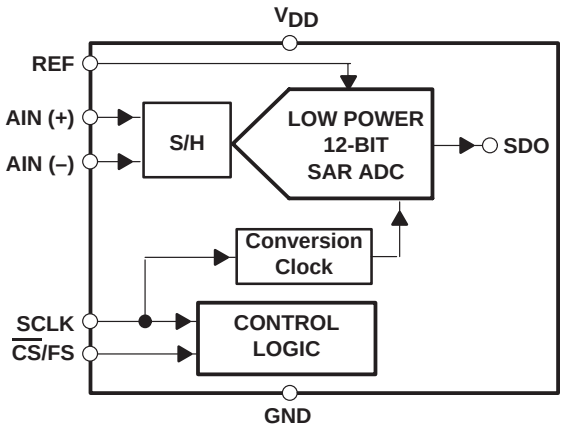
TLC2551



TLC2552



TLC2555



Terminal Functions

TLC2551

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AIN	4	I	Analog input channel
$\overline{CS}$	1	I	Chip select. A high-to-low transition on the $\overline{CS}$ input removes SDO from 3-state within a maximum setup time. $\overline{CS}$ can be used as the FS pin when a dedicated serial port is used. If TLC2551 is attached to a dedicated DSP serial port, this terminal can be grounded.
FS	7	I	DSP frame sync input. Indication of the start of a serial data frame. Tie this terminal to V_{DD} if not used.
GND	3	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
SCLK	5	I	Output serial clock. This terminal receives the serial SCLK from the host processor.
SDO	8	O	The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state until $\overline{CS}$ falling edge. The output format is MSB first. When FS is not used (FS = 1 at the falling edge of $\overline{CS}$): The MSB is presented to the SDO pin after $\overline{CS}$ falling edge and output data is valid on the falling edge of SCLK. When FS is used (FS = 0 at the falling edge of $\overline{CS}$): The MSB is presented to the SDO pin after the falling edge of FS or the falling edge of $\overline{CS}$ (whichever happens first). Output data is valid on the falling edge of SCLK. (This is typically used with an active FS from a DSP).
V_{DD}	6	I	Positive supply voltage
V_{REF}	2	I	External reference input

TLC2552/55

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AIN0 /AIN(+)	4	I	Analog input channel 0. (positive input for TLV2555)
AIN1/AIN (–)	5	I	Analog input channel 1 (inverted input for TLV2555)
$\overline{CS}$/FS	1	I	Chip select/frame sync. A high-to-low transition on the $\overline{CS}$/FS removes SDO from 3-state within a maximum delay time.
GND	3	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
SCLK	7	I	Output serial clock. This terminal receives the serial SCLK from the host processor.
SDO	8	O	The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state when $\overline{CS}$/FS is high and presents output data after the $\overline{CS}$/FS falling edge until the LSB is presented. The output format is MSB first. SDO returns to the Hi-Z state after the 16th SCLK. Output data is valid on the falling SCLK edge.
V_{DD}	6	I	Positive supply voltage
V_{REF}	2	I	External reference input

detailed description

The TLC2551/2/5 are successive approximation (SAR) ADCs utilizing a charge redistribution DAC. Figure 1 shows a simplified version of the ADC.

The sampling capacitor acquires the signal on AIN during the sampling period. When the conversion process starts, the SAR control logic and charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When the comparator is balanced, the conversion is complete and the ADC output code is generated.

detailed description (continued)

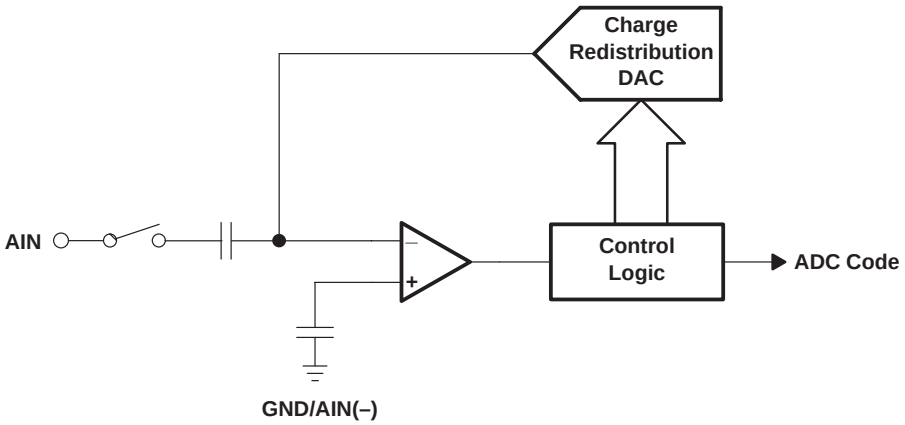


Figure 1. Simplified SAR Circuit

serial interface

OUTPUT DATA FORMAT	
MSB	**LSB**
D15–D4	D3–D0
Conversion result (OD11–OD0)	Don't care

The output data format is binary (unipolar straight binary).

binary

Zero scale code = 000h, Vcode = GND
Full scale code = FFFh, Vcode = VREFP – 1 LSB

pseudo-differential inputs

The TLC2555 operates in pseudo-differential mode. The inverted input is available on terminal 5. It can have a maximum input ripple of ±0.2 V. This is normally used for ground noise rejection.

control and timing

start of the cycle

TLC2551

- When FS is not used (FS = 1 at the falling edge of $\overline{CS}$), the falling edge of $\overline{CS}$ is the start of the cycle. Output data changes on the rising edge of SCLK. This is typically used for a microcontroller with SPI interface, although it can also be used for a DSP. The microcontroller SPI interface should be programmed for CPOL=0 (serial clock reference to ground) and CPHA=1 (data is valid on the falling edge of serial clock).
- When FS is used (FS is an active signal from a DSP), the falling edge of FS is the start of the cycle. Output data changes on the rising edge of SCLK. This is typically used for a TMS320 DSP. If the TLC2551 is attached to a dedicated DSP serial port. $\overline{CS}$ terminal can be grounded.

TLC2552/5

The $\overline{CS}$ and FS inputs are accessed via the same pin (pin 1) on the TLC2552 and TLC2555. The cycle is started by the falling edge transition provided by either a $\overline{CS}$ (interfacing with a SPI interface microcontroller) signal or FS (interfacing with a TMS320 DSP) signal. Timing for the TLC2555 is much like the TLC2551, with the exception of the $\overline{CS}$/FS line.

detailed description (continued)

TLC2552 channel MUX reset cycle

The TLC2552 uses $\overline{CS}$/FS to reset the AIN multiplexer. A short active $\overline{CS}$/FS cycle (4–7 SCLKs) resets the MUX to AIN0. If the $\overline{CS}$/FS cycle is sufficient to complete the conversion (16 SCLKs plus maximum conversion time), the MUX toggles to the next channel (see Figure 4 for timing).

sampling

The converter sample time is 12 SCLKs beginning on the 5th SCLK received after the converter has received an active $\overline{CS}$ or FS signal ($\overline{CS}$/FS for the TLC2552/5).

conversion

The TLC2551 completes conversion in the following manner. The conversion is started after the 16th SCLK edge. The conversion takes 1.4 μs using 20 MHz SCLK plus 0.1 μs overhead. Enough time (for conversion) should be allowed before a rising $\overline{CS}$/FS edge so that no conversion is terminated prematurely.

TLC2552 input channel selection is toggled on each rising $\overline{CS}$ /FS edge. The MUX channel can be reset to AIN0 via $\overline{CS}$ /FS as described in the earlier section and in Figure 5. The input is sampled for 12 SCLKs, converted, and the result is presented on SDO during the next cycle. Care should also be taken to allow enough time between samples to avoid prematurely terminating the conversion, which occurs on a rising $\overline{CS}$ /FS transition if the conversion is not complete.

timing diagrams/conversion cycles

DSP Interface

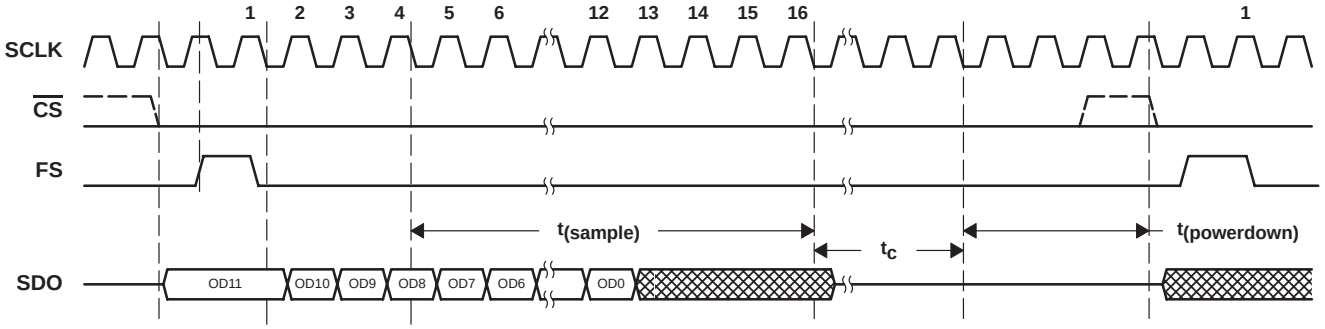


Figure 2. TLC2551 DSP Mode/FS Active

μP Interface

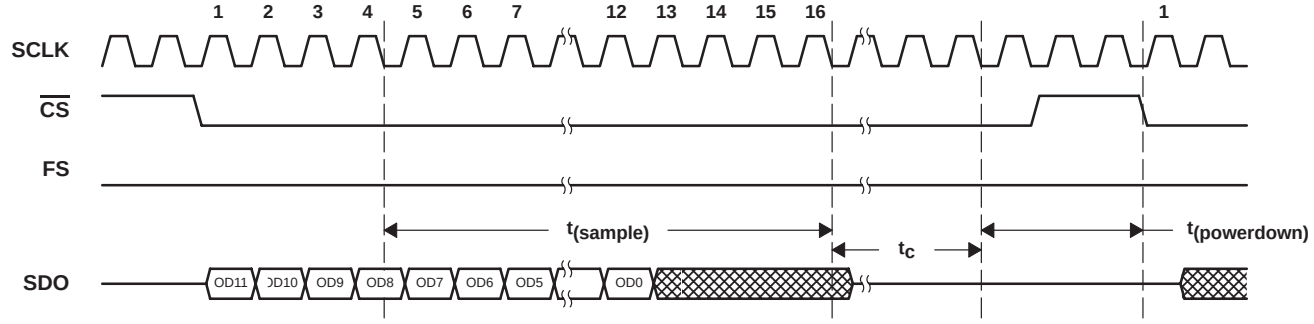


Figure 3. TLC2551 Microcontroller Mode/(SPI, CPOL = 0, CPHA = 1)

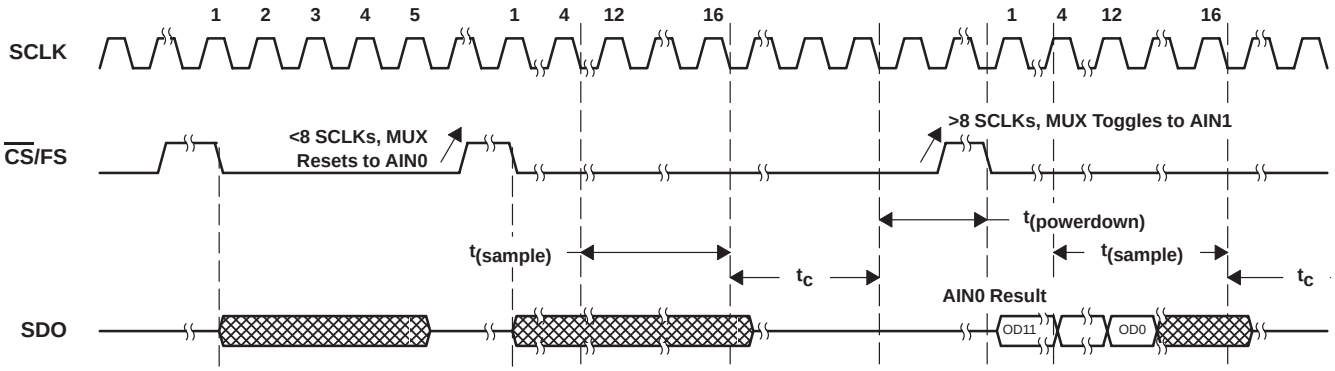


Figure 4. TLC2552 Timing

timing diagrams/conversion cycles (continued)

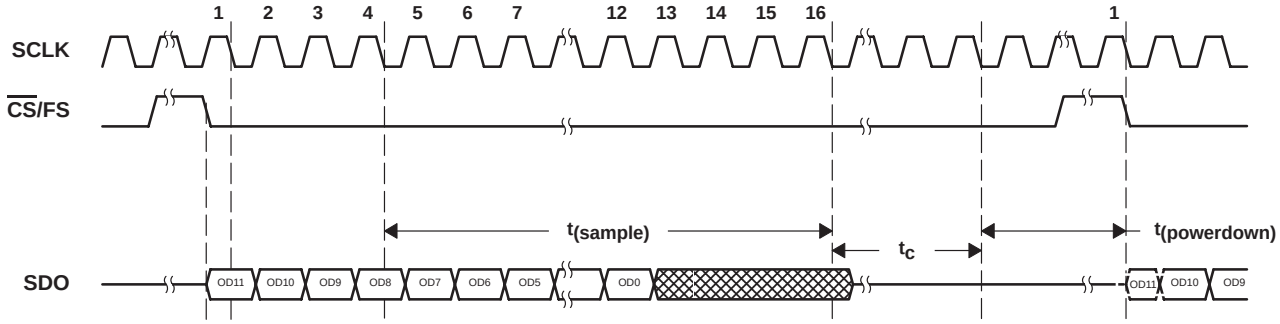


Figure 5. TLC2555 Timing

use $\overline{CS}$ as FS input

When interfacing the TLC2551 with the TMS320 DSP, the FSR signal from the DSP may be connected to the $\overline{CS}$ input if this is the only device on the serial port. This will save one output terminal from the DSP. (Output data changes on the falling edge of SCLK. Default for TLC2552 and TLC2555).

SCLK and conversion speed

It takes 14 conversion clocks to complete the conversion. The conversion clock for the TLC2551/2/5 is equal to SCLK/2. This yields a minimum conversion time of 1.4 μs plus 0.1 μs overhead. These devices can operate with an SCLK up to 20 MHz for the supply voltage range specified. The total conversion time is 14× (1/10M) +16× (1/20M)+ 0.1 μs} = 2.3 μs for a 20 MHz SCLK. This is the minimum cycle time for an active $\overline{CS}$ or $\overline{CS}$/FS signal. If violated, the conversion will terminate, invalidating the next data output cycle.

reference voltage

An external reference is applied via VREF. The voltage level applied to this pin establishes the upper limit of the analog inputs to produce a full-scale reading. The value of V_{REF} and the analog input should not exceed the positive supply or be less than GND, consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than V_{REF} and at zero when the input signal is equal to or lower than GND.

powerdown and powerup initialization

Autopower down is built in to the devices in order to reduce power consumption. The wake-up time is fast enough to provide power down between each cycle. The power-down state is initiated at the end of conversion and wakes up upon a falling edge on $\overline{CS}$ or FS.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, GND to V_{DD} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to V_{DD} + 0.3 V
Reference input voltage . . . . . V_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to V_{DD}+ 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A: C . . . . . 0°C to 70°C
I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	3.3	5.5	V
Positive external reference voltage input, V_{REFP} (see Note 1)		2		V_{DD}	V
Analog input voltage (see Note 1)		0		V_{DD}	V
High level control input voltage, V_{IH}		2.1			V
Low-level control input voltage, V_{IL}				0.6	V
Setup time, $\overline{CS}$ falling edge (for 2551) or $\overline{CS}$/FS falling edge (for 2552/55) before first SCLK falling edge, $t_{su(CSL-SCLKL)}$	V_{DD} = REF = 5.5 V	40			ns
Hold time, $\overline{CS}$ rising edge after SCLK falling edge, $t_{h(SCLKL-CSH)}$		5			ns
Delay time, delay from $\overline{CS}$ falling edge to FS rising edge ($t_{d(CSL-FSH)}$		0.5		7	SCLKs
Setup time, FS rising edge before SCLK falling edge, $t_{su(FSH-SCLKL)}$		0.35			SCLKs
Hold time, FS hold high after SCLK falling edge, $t_{h(SCLKL-FSL)}$				0.65	SCLKs
Pulse width CS high time, $t_{wH(CS)}$		100			ns
Pulse width FS high time, $t_{wH(FS)}$		0.75			SCLKs
SCLK cycle time, V_{DD} = 5.5–4.5 V, $t_{c(SCLK)}$		50		10000	ns
Pulse width low time, $t_{wL(SCLK)}$		0.4		0.6	SCLKs
Pulse width high time, $t_{wH(SCLK)}$		0.4		0.6	SCLKs
Hold time, hold from end of conversion to CS high, $t_{h(EOC-CSH)}$ (EOC is internal, indicates end of conversion time, t_c)		0.1			µs
Active CS/FS cycle time to reset internal MUX to AIN0, reset cycle	TLC2552 only	4		7	SCLKs
Operating free-air temperature, T_A	TLC2551/2/5C	0		70	°C
	TLC2551/2/5I	–40		85	

NOTES: 1. Analog input voltages greater than that applied to VREF convert as all ones (111111111111), while input voltages less than that applied to GND convert as all zeros(000000000000).
2. This is the time required for the clock input signal to fall from V_{IH} max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = V_{REF} = 4.5 V to 5.5 V, SCLK frequency = 20 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 5.5 V, I_{OH} = –0.2 mA at 30 pF load		2.4			V
V_{OL}	Low-level output voltage	V_{DD} = 5.5 V, I_{OL} = 0.8 mA at 30 pF load				0.4	V
I_{OZ}	Off-state output current (high-impedance-state)	V_O = V_{DD}	$\overline{CS}$ = V_{DD}		1	2.5	µA
		V_O = 0			–1	–2.5	
I_{IH}	High-level input current	V_I = V_{DD}			0.005	2.5	µA
I_{IL}	Low-level input current	V_I = 0 V			–0.005	2.5	µA
I_{CC}	Operating supply current	$\overline{CS}$ at 0 V,	V_{DD} = 4.5 V ~ 5.5 V		3	3.5	mA
$I_{CC(AUTOPWDN)}$	Autopower-down current (0.5 µs inactive)	For all digital inputs, 0≤ V_I ≤ 0.3 V or V_I ≥ V_{DD}– 0.3 V, SCLK = 0, V_{DD} = 4.5 V to 5.5 V, Ext ref				8	µA
	Autopower-down current (5 µs inactive)					1	
	Selected analog input channel leakage current	Selected channel at V_{DD}				1	µA
		Selected channel at 0 V				–1	
C_i	Input capacitance	Analog inputs		20	45	50	pF
		Control Inputs			5	25	
	Input on resistance	V_{DD} = 5.5 V				500	Ω
	Delay time, delay from $\overline{CS}$ falling edge to SDO valid, $t_{d(CSL-SDOV)}$	V_{DD} = REF = 5.5 V, 30 pF				40	ns
	Delay time, delay from FS falling edge to SDO valid, $t_{d(FSL-SDOV)}$	V_{DD} = REF = 5.5 V, 30 pF				1	ns
	Delay time, delay from SCLK rising edge to SDO valid, $t_{d(SCLKH-SDOV)}$	V_{DD} = REF = 5.5 V, 30 pF				11	ns
	Delay time, delay from 17th SCLK rising edge to SDO 3-state, $t_{d(SCLK17H-SDOZ)}$	V_{DD} = REF = 5.5 V, 30 pF				30	ns
t_c	Conversion time	Conversion clock = internal oscillator			28		SCLK
$t_{(sample)}$	Sampling time	See Note 3		300			ns
Autopower down	Action time	I_{CC} start to decrease			0.5		SCLK
	Wakeup time	I_{CC} down to MIN [$I_{CC(AUTOPWDN)}$]			1	2	ms
	Autopower down				0.5		SCLK

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTE 3: Minimal $t_{(sample)}$ is given by 0.9 × 50 pF × (R_S + 0.5 kΩ), where R_S is the source output impedance.

ac specifications (f_i = 20 kHz)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion	400 KSPS, $V_{DD} = V_{REF}$ = 5 V	70	72		dB
THD	Total harmonic distortion	400 KSPS, $V_{DD} = V_{REF}$ = 5 V		–84	–80	dB
ENOB	Effective number of bits	400 KSPS, $V_{DD} = V_{REF}$ = 5 V		11.8		Bits
SFDR	Spurious free dynamic range	400 KSPS, $V_{DD} = V_{REF}$ = 5 V		–84	–80	dB
Analog Input						
	Full power bandwidth, –3 dB			1		MHz
	Full-power bandwidth, –1 dB			500		kHz

external reference specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Reference input voltage	V_{DD} = =4.5 V ~ 5.5 V				V_{DD}	V
	Reference input impedance	V_{DD} = 5.5 V	$\overline{CS}$ = 1, SCLK = 0	100			MΩ
			$\overline{CS}$ = 0, SCLK = 20 MHz	20	25		kΩ
	Reference current	$V_{DD} = V_{REF}$ = 5.5 V			100	400	μA
	Reference input capacitance	$V_{DD} = V_{REF}$ = 5.5 V	$\overline{CS}$ = 1, SCLK = 0	5		15	pF
			$\overline{CS}$ = 0, SCLK = 20 MHz	20	45	50	
V_{REF}	Reference voltage	V_{DD} = =4.5 V – 5.5 V				V_{DD}	V

dc specification, $V_{DD} = V_{REF}$ = 4.5 V to 5.5 V, SCLK frequency = 20 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
INL	Integral linearity error (see Note 5)				±0.6	±1	LSB
DNL	Differential linearity error	See Note 4			±0.5	±1	LSB
E_O	Offset error (see Note 6)	See Note 4	TLC2551/52			±1.5	LSB
			TLC2555			±2.5	
E_G	Gain error (see Note 6)	See Note 4	TLC2551/52			±2	LSB
			TLC2555			±5	
E_t	Total unadjusted error (see Note 7)	See Note 4	TLC2551/52			±2	LSB
			TLC2555			±5	

NOTES: 4. Analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (0000000000).
5. Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Zero error is the difference between 000000000000 and the converted output for zero input voltage: full-scale error is the difference between 111111111111 and the converted output for full-scale input voltage.
7. Total unadjusted error comprises linearity, zero, and full-scale errors.

PARAMETER MEASUREMENT INFORMATION

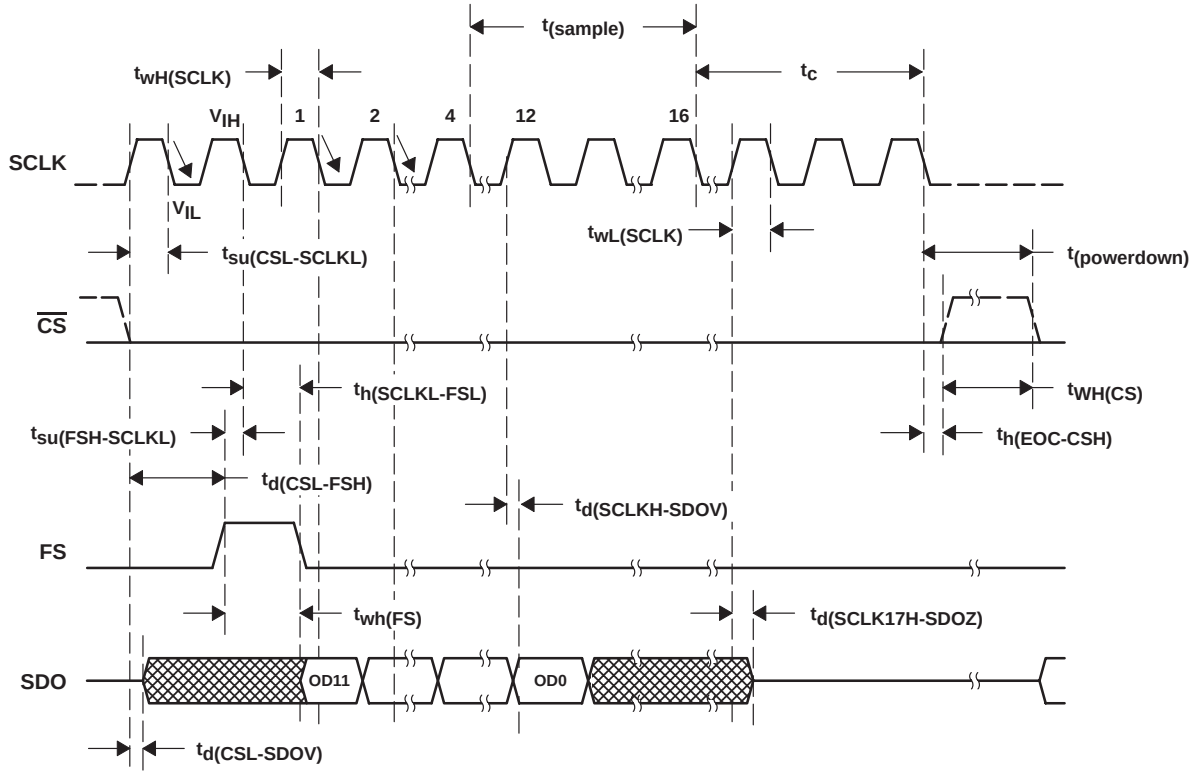


Figure 6. Critical Timing TLC2551 (FS is active)

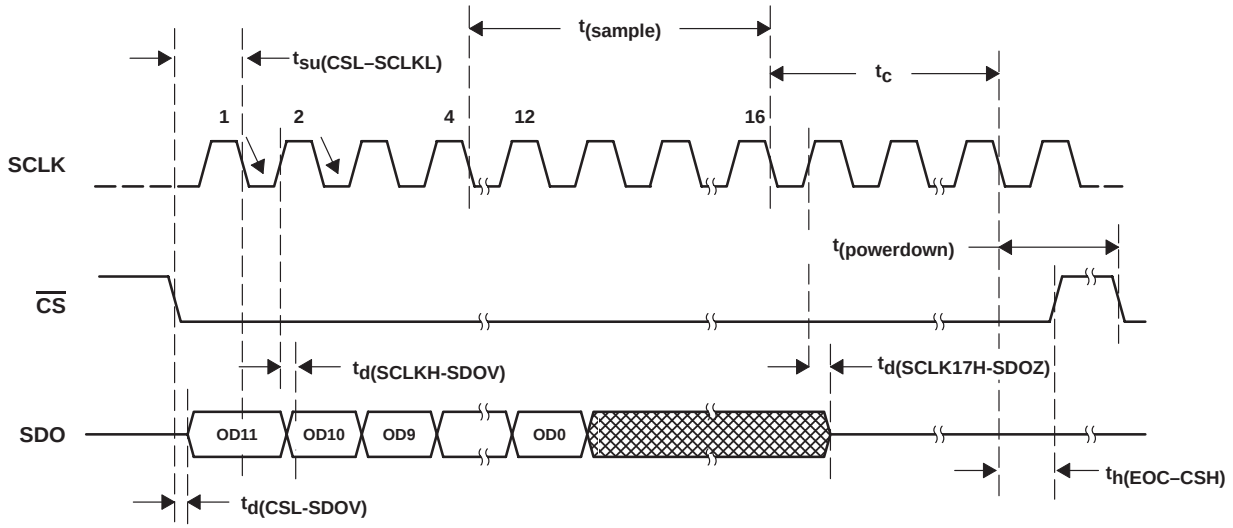


Figure 7. Critical Timing TLC2551 (FS = 1)

PARAMETER MEASUREMENT INFORMATION

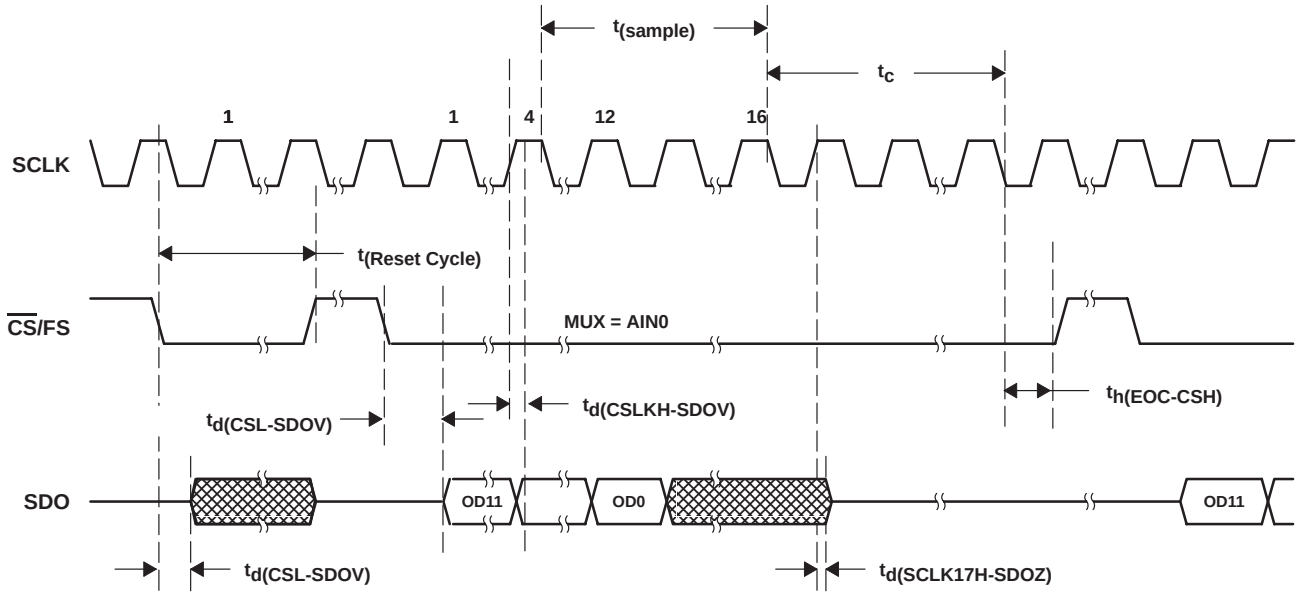


Figure 8. Critical Timing TLC2552 Reset Cycle

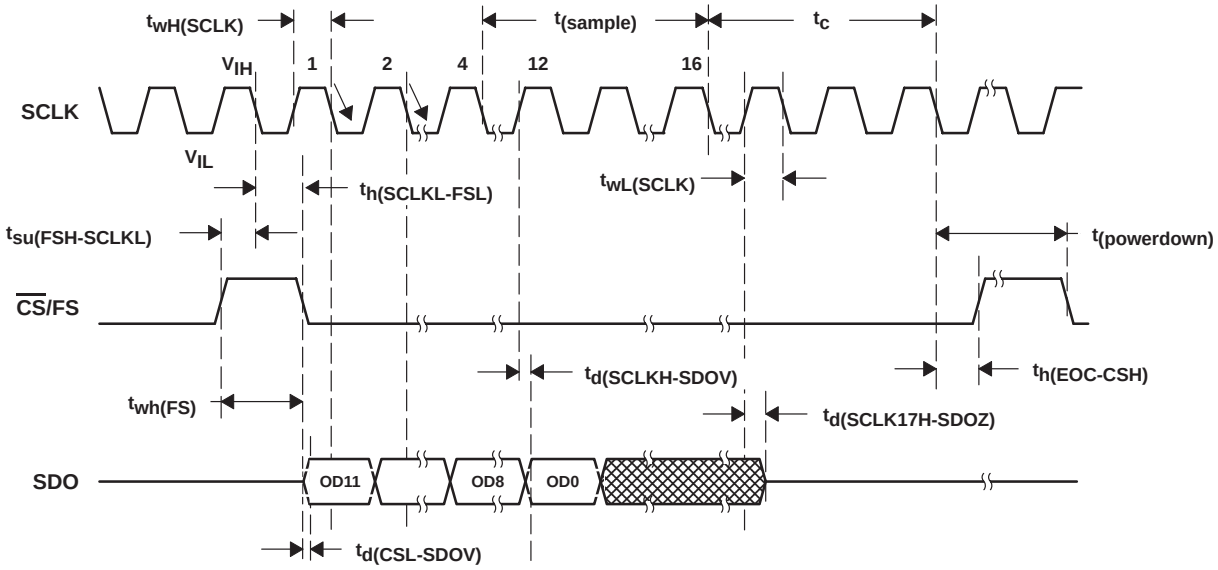


Figure 9. Critical Timing TLC2555 Power-Down Cycle

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY vs TEMPERATURE

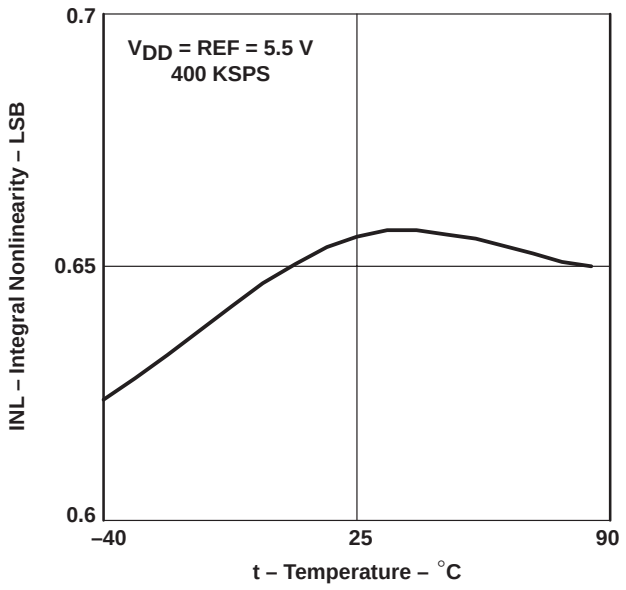


Figure 10

DIFFERENTIAL NONLINEARITY vs TEMPERATURE

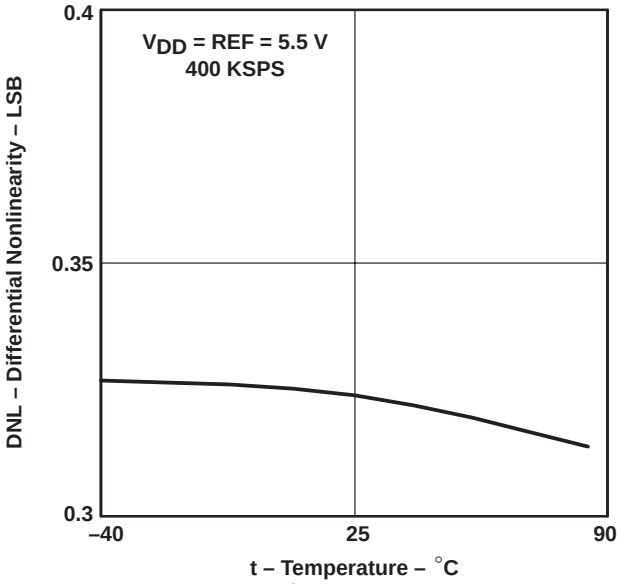


Figure 11

OFFSET ERROR vs TEMPERATURE

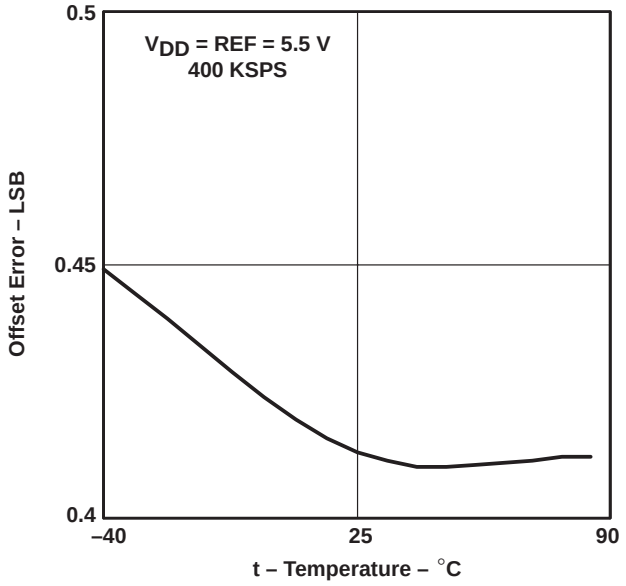


Figure 12

GAIN ERROR vs TEMPERATURE

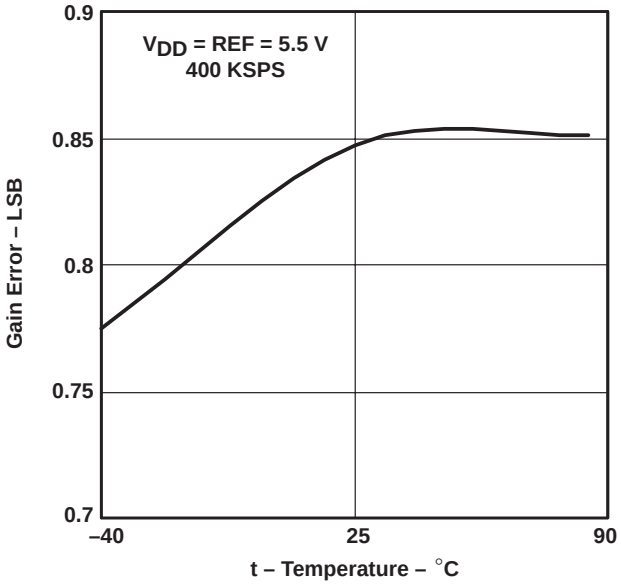


Figure 13

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs TEMPERATURE

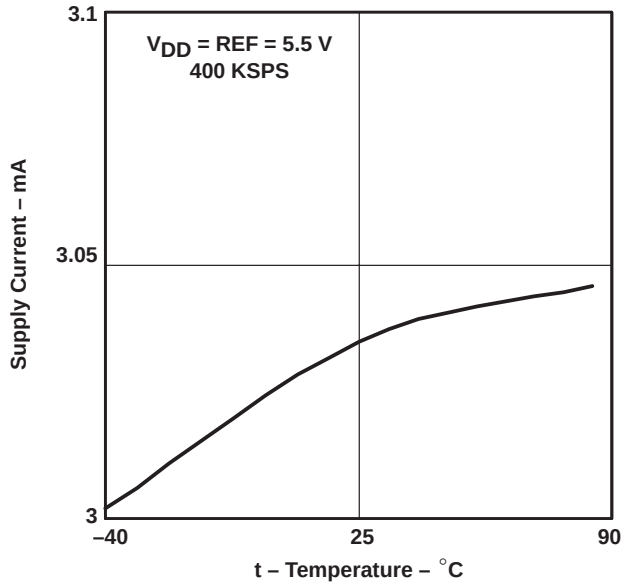


Figure 14

DIFFERENTIAL NONLINEARITY vs DIGITAL OUTPUT CODES

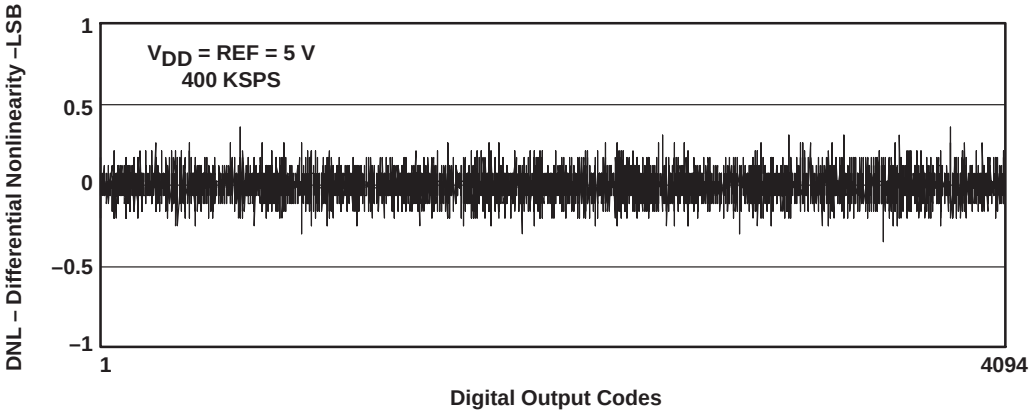


Figure 15

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY vs DIGITAL OUTPUT CODES

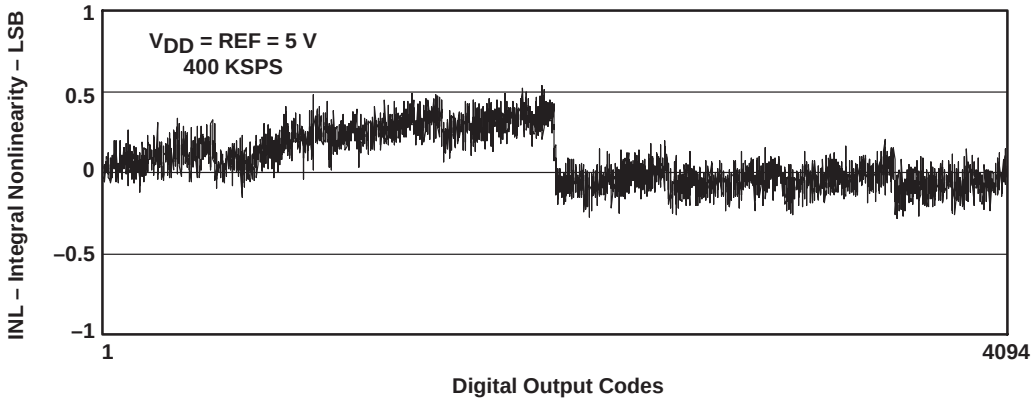


Figure 16

2048 POINTS FAST FOURIER TRANSFORM (FFT)

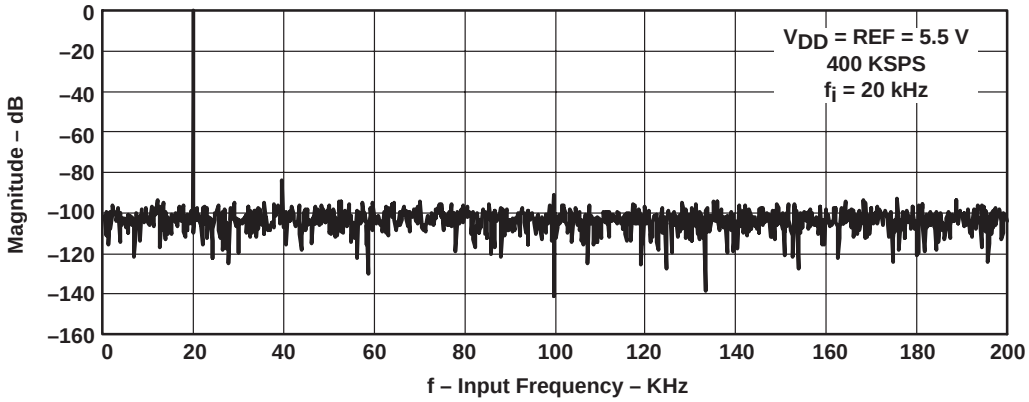


Figure 17

TYPICAL CHARACTERISTICS

SINAD
vs
FREQUENCY

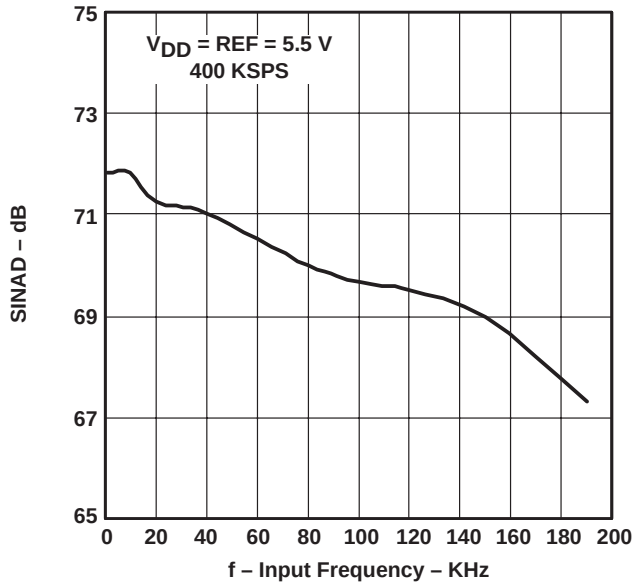


Figure 18

ENOB
vs
FREQUENCY

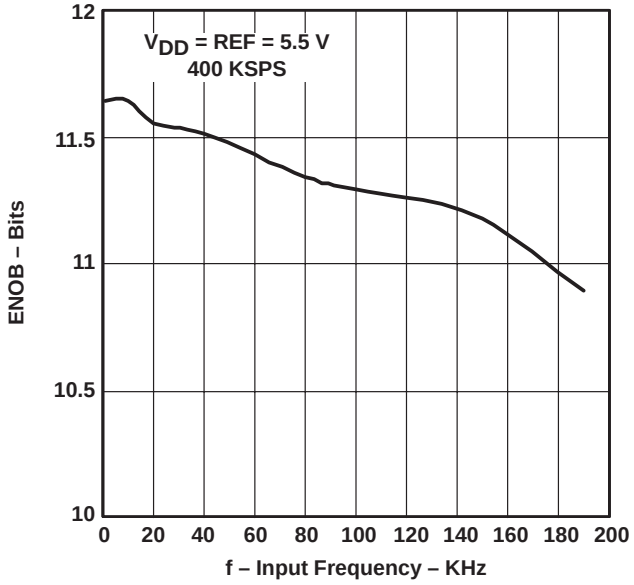


Figure 19

THD
vs
FREQUENCY

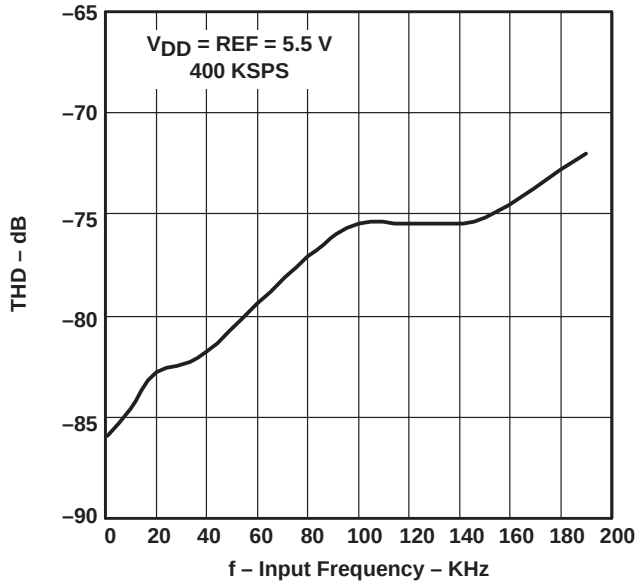
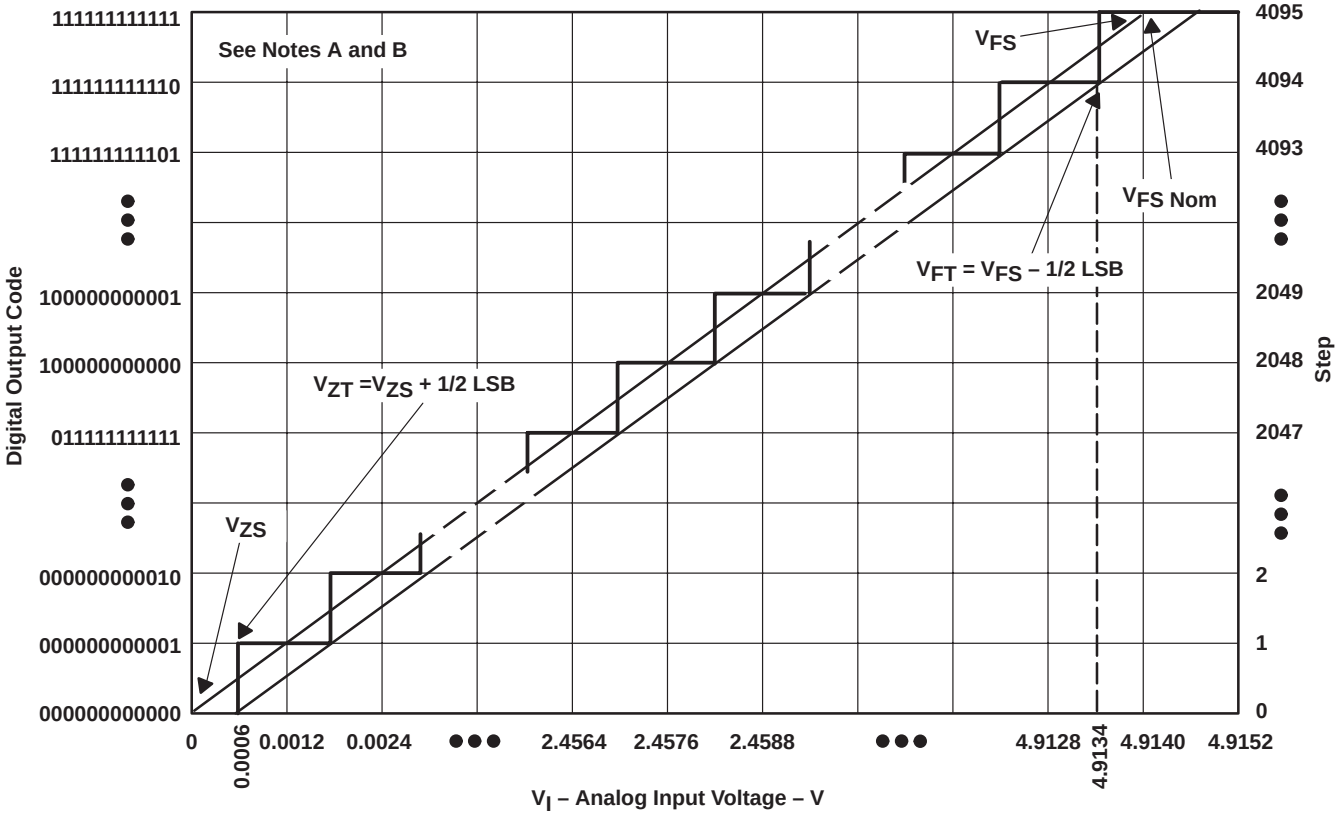


Figure 20

TYPICAL CHARACTERISTICS

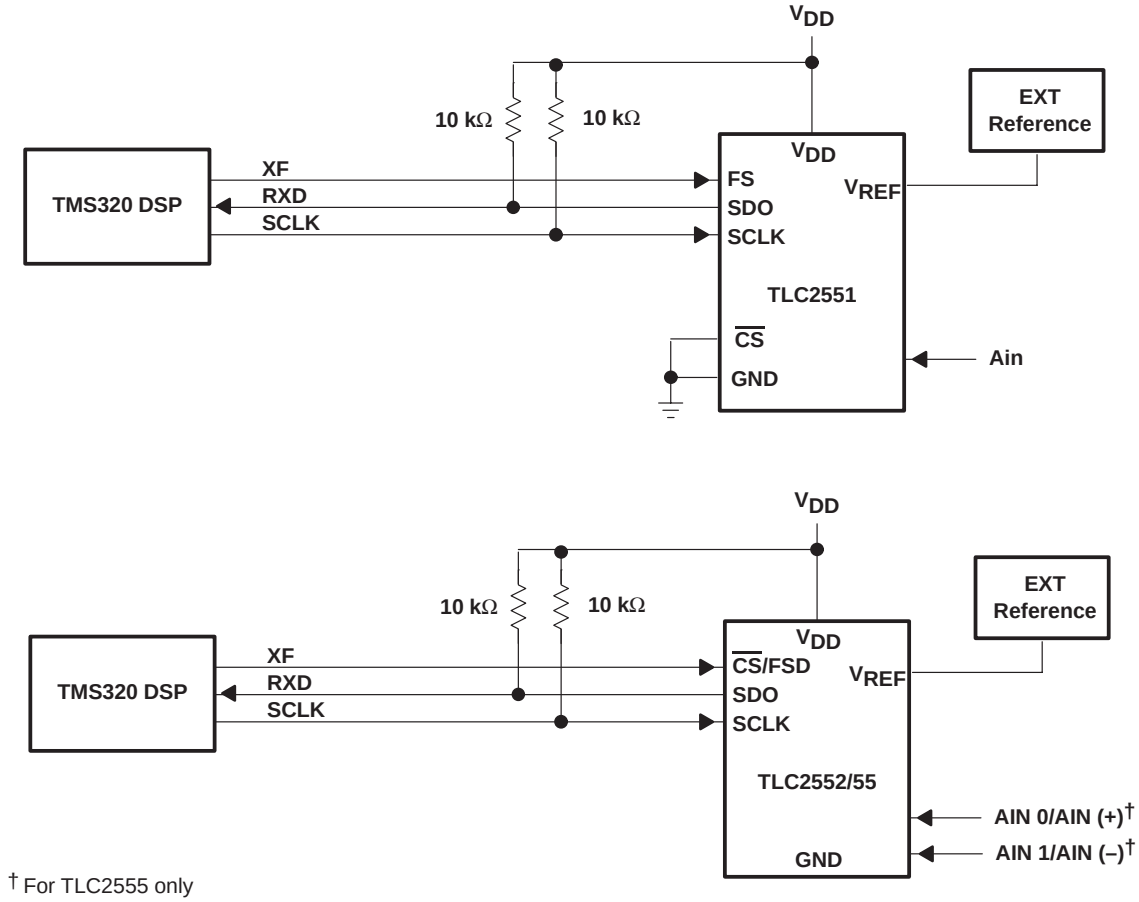


NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V, and the transition to full scale (V_{FT}) is 4.9134 V, 1 LSB = 1.2 mV.

B. The full scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 21. Ideal 12-Bit ADC Conversion Characteristics

APPLICATION INFORMATION



† For TLC2555 only

Figure 22. Typical Interface to a TMS320 DSP

simplified analog input analysis

Using the equivalent circuit in Figure 23, the time required to charge the analog input capacitance from 0 to Vs within 1/2 LSB can be derived as follows.

The capacitance charging voltage is given by:

$$Vc = Vs\left(1 - EXP\left(\frac{-tch}{Rt \times Ci}\right)\right) \quad (1)$$

Where:

Rt = Rs + Zi
tch = Charge time

The input impedance Zi is 0.5 kΩ at 5 V, and is higher (~ 0.6 kΩ) at 2.7 V. The final voltage to 1/2 LSB is given by:

$$Vc\ (1/2\ LSB) = Vs - \left(\frac{Vs}{8192}\right) \quad (2)$$

APPLICATION INFORMATION

simplified analog input analysis (continued)

Equating equation 1 to equation 2 and solving for cycle time t_c gives:

$$Vs - \left(\frac{VS}{8192}\right) = Vs\left(1 - EXP\left(\frac{-tch}{Rt \times Ci}\right)\right) \quad (3)$$

and time to change to 1/2 LSB (equal to minimum sampling time) is:

$$tch\ (1/2\ LSB) = Rt \times Ci \times In(8192) = Min[t(sample)]$$

Where:

In(8192) = 9.011

Therefore, with the values given, the time for the analog input signal to settle is:

$$tch\ (1/2\ LSB) = (Rs + 0.5\ k\Omega) \times Ci \times In(8192) \quad (4)$$

This time must be less than the converter sample time shown in the timing diagrams. This is 12× SCLKs.

$$t_{(sample)} = 12\times \frac{1}{f(SCLK)} \geq Min\left[t_{(sample)}\right] = tch\left(\frac{1}{2}\ LSB\right) \quad (5)$$

Therefore the maximum SCLK frequency is:

$$max\left[f_{(SCLK)}\right] = \frac{12}{tch\ (1/2\ LSB)} = \frac{12}{[In(8192) \times Rt \times Ci]} \quad (6)$$

maximum conversion throughput

For a supply voltage of 5 V, if the source impedance is less than 1 kΩ, and the ADC analog input capacitance Ci is less than 50 pF, this equates to a minimum sampling time tch $\left(\frac{1}{2}\ LSB\right)$ of 0.676 µs (<1 µs). Since the sampling time requires 12 SCLKs, the fastest SCLK frequency is 12 tch$\left(\frac{1}{2}\ LSB\right)$ = 12 MHz for $R_S \leq 1$ kΩ.

The minimal total cycle time, $t_{(cycle)}$, is given as:

$$t_{(cycle)} = t_{(sample)} + t_c + t_{(overhead)} = \frac{16}{Max\left[f(SCLK)\right]} + \frac{14}{f[(SCLK)] \times 0.5} + 0.1\ \mu s = 3.77\ \mu s$$

This is equivalent to a maximum throughput, max[fs] of 265 KSPS.

The throughput can be even higher with a smaller source impedance. When source impedance is 100 Ω, the minimum sampling time becomes:

$$tch\ (1/2\ LSB) = Rt \times Ci \times In(8192) = 0.27\ \mu s$$

APPLICATION INFORMATION

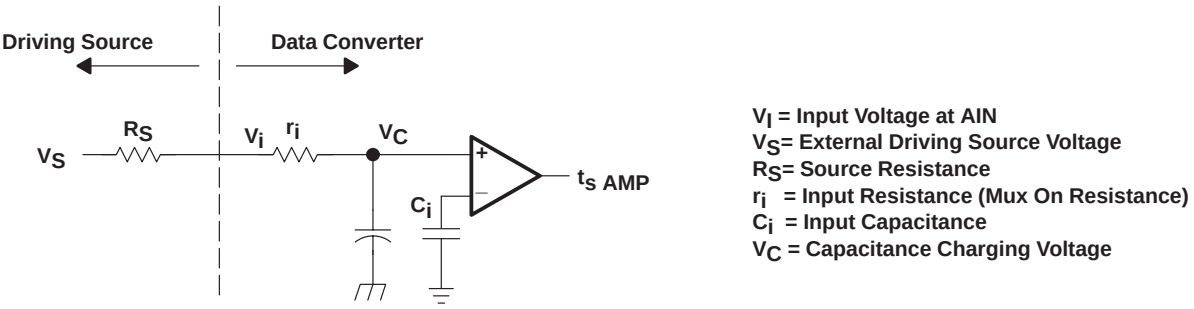
maximum conversion throughput (continued)

The maximum SCLK frequency possible is 12/tch $\left(\frac{1}{2}\ LSB\right)$ = 44 MHz. Then a 20 MHz clock (maximum SCLK frequency allowed for the internal comparator can be used. The minimal total cycle time is then reduced to:

$$t_{(cycle)} = t_{(sample)} + tc + t_{overhead} = \frac{16}{max\left[f(SCLK)\right]} + \frac{16}{max\left[f(SCLK)\right]/2} + 0.1\ \mu s = 2.3\ \mu s$$

The maximum throughput, MAX[fs], is 1/2.3 μs = 134 KSPS for this case.

Driving Source Requirements:



V_I = Input Voltage at AIN
V_S= External Driving Source Voltage
R_S= Source Resistance
r_i = Input Resistance (Mux On Resistance)
C_i = Input Capacitance
V_C = Capacitance Charging Voltage

NOTE: Noise and distortion must for the source be equivalent to the resolution of the converter. R_S must be real at the input frequency.

Figure 23. Equivalent Input Circuit Including the Driving Source

power down calculations

Total power consumption at different conversion rate f_S, ($f_S \le$ MAX [f_S]) can be calculated by:

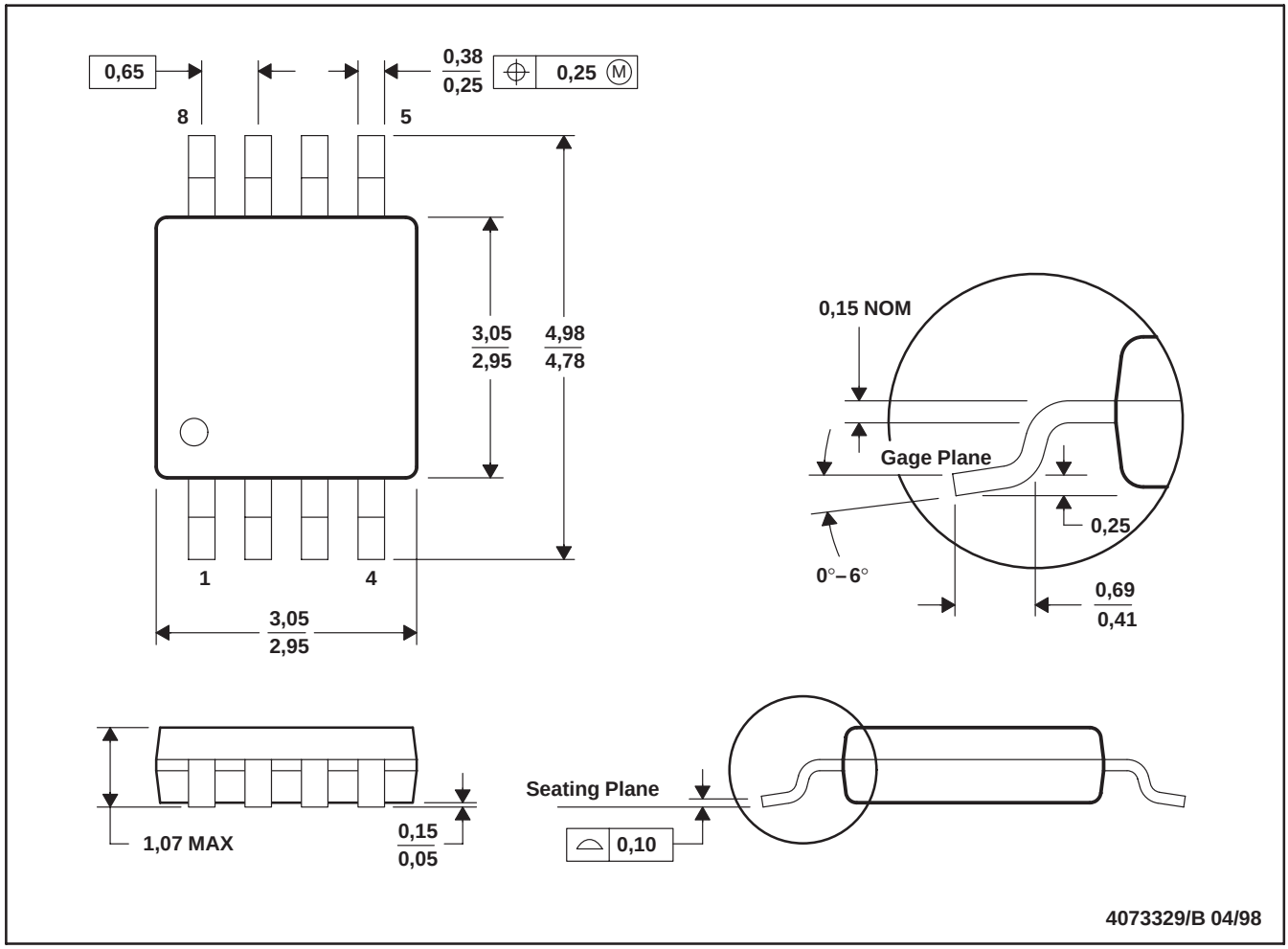
$V_{DD} \times i(AVERAGE) = V_{DD}\ [(f_S/MAX\ [f_S]) \times i(ON) + (1–f_S/MAX\ [f_S]) \times i(OFF)]$

If V_{DD} = 5 V for TLC2551, and the sampling rate f_S = 10 kHz, the maximum sampling rate f_{SMAX} = 200 kHz

then i(ON) = ~3.5 mA operating current
and i(OFF) = ~8 μA auto-powerdown current
so $V_{DD} \times i(AVERAGE) = 5 \times (0.05 \times 3500\ \mu A + 0.95 \times 8\ \mu A)$
$= (5 \times 182.6)\ \mu W$
$= 0.9$ mW

MECHANICAL DATA

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**

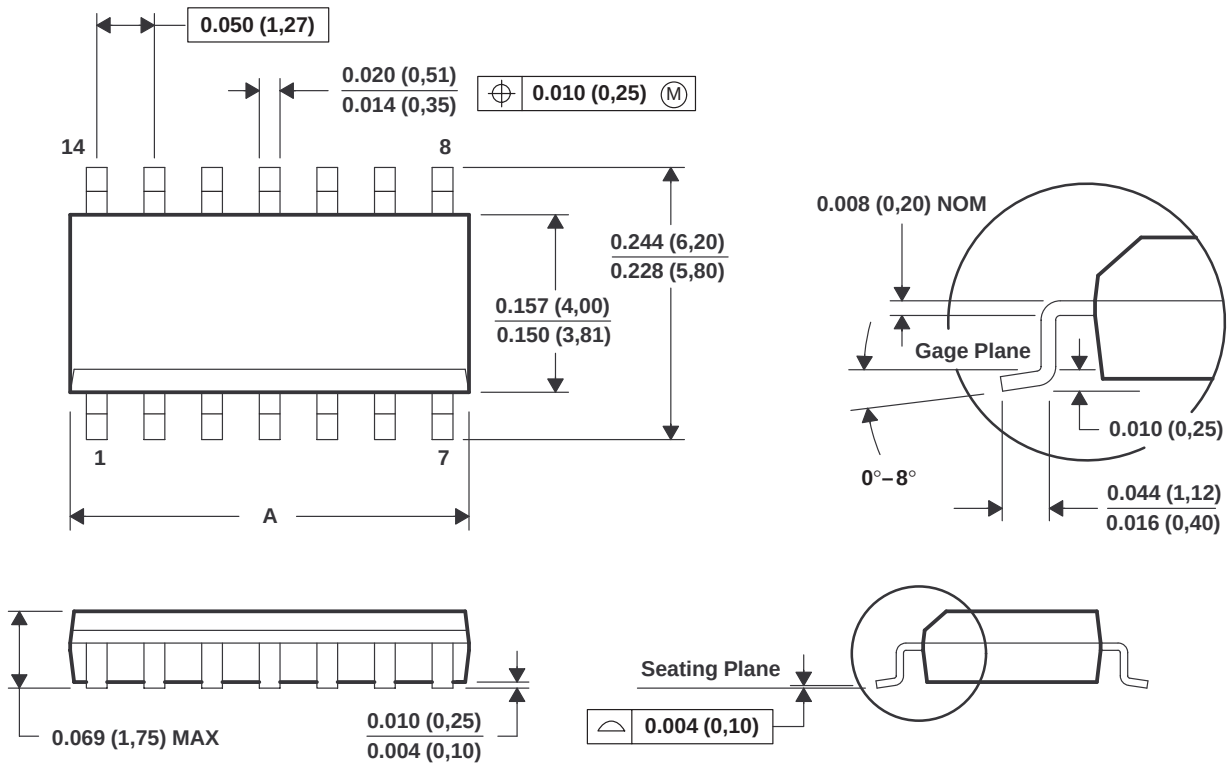


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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