

# CLC425

## Ultra Low Noise Wideband Op Amp

### General Description

The CLC425 combines a wide bandwidth (**1.9GHz GBW**) with very low input noise (**1.05nV/√Hz**, **1.6pA/√Hz**) and low dc errors (**100μV V<sub>OS</sub>**, **2μV/°C drift**) to provide a very precise, wide dynamic-range op amp offering closed-loop gains of  $\geq 10$ .

Singularly suited for very wideband high-gain operation, the CLC425 employs a traditional voltage-feedback topology providing all the benefits of balanced inputs, such as low offsets and drifts, as well as a 96dB open-loop gain, a 100dB CMRR and a 95dB PSRR.

The CLC425 also offers great flexibility with its externally adjustable supply current, allowing designers to easily choose the optimum set of power, bandwidth, noise and distortion performance. Operating from  $\pm 5V$  power supplies, the CLC425 defaults to a 15mA quiescent current, or by adding one external resistor, the supply current can be adjusted to less than 5mA.

The CLC425's combination of ultra-low noise, wide gain-bandwidth, high slew rate and low dc errors will enable applications in areas such as medical diagnostic ultrasound, magnetic tape & disk storage, communications and opto-electronics to achieve maximum high-frequency signal-to-noise ratios.

The CLC425 is available in the following versions:

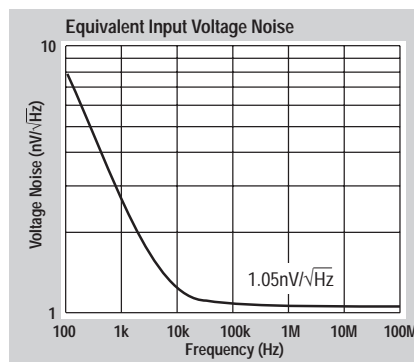
CLC425AJP	-40°C to +85°C	8-pin PDIP
CLC425AJE	-40°C to +85°C	8-pin SOIC
CLC425A8B	-55°C to +125°C	8-pin Cerdip, MIL-STD-883, Level B
CLC425ALC	-40°C to +85°C	dice
CLC425AMC	-55°C to +125°C	dice, MIL-STD-883, Level B
CLC425AJM5	-40°C to +85°C	5-pin SOT
DESC SMD number : 5962-93259.		

### Features

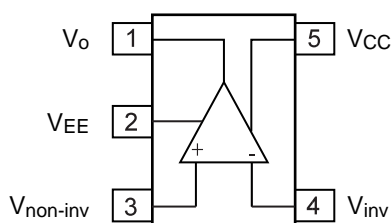
- 1.9GHz gain-bandwidth product
- 1.05nV/√Hz input voltage noise
- 0.8pA/√Hz @  $I_{CC} \leq 5mA$
- 100μV input offset voltage, 2μV/°C drift
- 350V/μs slew rate
- 15mA to 5mA adjustable supply current
- Gain range  $\pm 10$  to  $\pm 1,000V/V$
- Evaluation boards & simulation macromodel
- 0.9dB NF @  $R_S = 700\Omega$

### Applications

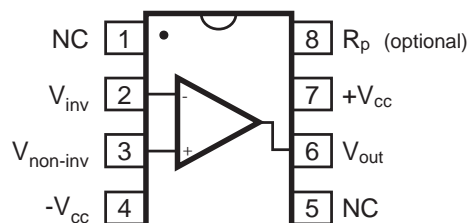
- Instrumentation sense amplifiers
- Ultrasound pre-amps
- Magnetic tape & disk pre-amps
- Photo-diode transimpedance amplifiers
- Wide band active filters
- Low noise figure RF amplifiers
- Professional audio systems
- Low-noise loop filters for PLLs



**Pinout**  
SOT23-5



**Pinout**  
DIP & SOIC



# CLC425 Electrical Characteristics ( $V_{CC} = \pm 5V$ ; $A_V = +20$ ; $R_i = 499\Omega$ ; $R_g = 26.1\Omega$ ; $R_L = 100\Omega$ ; unless noted)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS				UNITS	SYMBOL
Ambient Temperature	CLC425 AJ	+25°C	-40°C	+25°C	+85°C			
<b>FREQUENCY DOMAIN RESPONSE</b>								
gain bandwidth product	$V_{out} < 0.4V_{pp}$	1.9	1.5	1.5	1.0	GHz	GBW	
-3dB bandwidth	$V_{out} < 0.4V_{pp}$	95	75	75	50	MHz	SSBW	
	$V_{out} < 5.0V_{pp}$	40	30	30	20	MHz	LSBW	
gain flatness	$V_{out} < 0.4V_{pp}$							
peaking	DC to 30MHz	0.3	0.7	0.5	0.7	dB	GFP	
rolloff	DC to 30MHz	0.1	0.7	0.5	0.7	dB	GFR	
linear phase deviation	DC to 30MHz	0.7	1.5	1.5	2.5	°	LPD	
<b>TIME DOMAIN RESPONSE</b>								
rise and fall time	0.4V step	3.7	4.7	4.7	7.0	ns	TRS	
settling time to 0.2%	2V step	22	30	30	40	ns	TSS	
overshoot	0.4V step	5	12	10	12	%	OS	
slew rate	2V step	350	250	250	200	V/ $\mu$ s	SR	
<b>DISTORTION AND NOISE RESPONSE</b>								
2 <sup>nd</sup> harmonic distortion	$1V_{pp}$ , 10MHz	-53	48	48	46	dBc	HD2	
3 <sup>rd</sup> harmonic distortion	$1V_{pp}$ , 10MHz	-75	65	65	60	dBc	HD3	
3 <sup>rd</sup> order intermodulation intercept	10MHz	35				dBm	IMD	
equivalent noise input								
voltage	1MHz to 100MHz	1.05	1.25	1.25	1.8	nV/ $\sqrt{Hz}$	VN	
current	1MHz to 100MHz	1.6	4.0	2.5	2.5	pA/ $\sqrt{Hz}$	ICN	
noise figure	$R_S = 700\Omega$	0.9				dB	NF	
<b>STATIC DC PERFORMANCE</b>								
open-loop gain	DC	96	77	86	86	dB	AOL	
*input offset voltage		$\pm 100$	$\pm 1000$	$\pm 800$	$\pm 1000$	$\mu$ V	VIO	
average drift		$\pm 2$	8	—	4	$\mu$ V/°C	DVIO	
*input bias current		12	40	20	20	$\mu$ A	IB	
average drift		-100	-250	—	-120	nA/°C	DIB	
input offset current		$\pm 0.2$	3.4	2.0	2.0	$\mu$ A	IIO	
average drift		$\pm 3$	$\pm 50$	—	$\pm 25$	nA/°C	DIIO	
power supply rejection ratio	DC	95	82	88	86	dB	PSRR	
common mode rejection ratio	DC	100	88	92	90	dB	CMRR	
*supply current	$R_L = \infty$	15	18	16	16	mA	ICC	
<b>MISCELLANEOUS PERFORMANCE</b>								
input resistance	common-mode	2	0.6	1.6	1.6	M $\Omega$	RINC	
	differential-mode	6	1	3	3	k $\Omega$	RIND	
input capacitance	common-mode	1.5	2	2	2	pF	CINC	
	differential-mode	1.9	3	3	3	pF	CIND	
output resistance	closed loop	5	50	10	10	m $\Omega$	ROUT	
output voltage range	$R_L = \infty$	$\pm 3.8$	$\pm 3.5$	$\pm 3.7$	$\pm 3.7$	V	VO	
	$R_L = 100\Omega$	$\pm 3.4$	$\pm 2.8$	$\pm 3.2$	$\pm 3.2$	V	VOL	
input voltage range	common mode	$\pm 3.8$	$\pm 3.4$	$\pm 3.5$	$\pm 3.5$	V	CMIR	
output current	source	80	70	70	70	mA	IOP	
	sink	80	45	55	55	mA	ION	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Absolute Maximum Ratings

$V_{CC}$	$\pm 7V$
$I_{out}$ short circuit protected to ground, however maximum reliability is obtained if $I_{out}$ does not exceed...	125mA
common-mode input voltage	$\pm V_{CC}$
maximum junction temperature	+150°C
operating temperature range:	
AJ	-40°C to +85°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD (human body model)	1000V

## Miscellaneous Ratings

Recommended gain range  $\pm 10$  to  $\pm 1,000V/V$

### Notes:

\* AJ : 100% tested at +25°C.

## Package Thermal Resistance

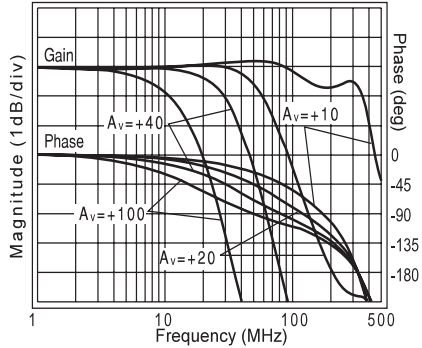
Package	$\theta_{JC}$	$\theta_{JA}$
AJP	70°C/W	125°C/W
AJE	65°C/W	145°C/W
A8B	45°C/W	135°C/W
AJM5	115°C/W	185°C/W

## Reliability Information

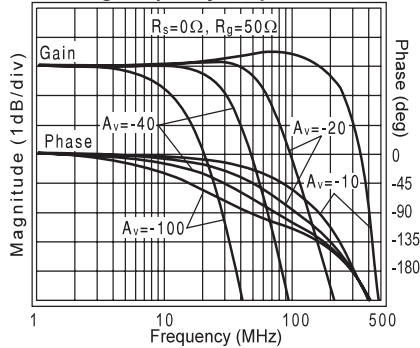
Transistor count	31
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# CLC425 Typical Performance ( $T_A=25^\circ\text{C}$ , $V_{CC}=\pm 5\text{V}$ , $R_g=26.1\Omega$ , $R_f=499\Omega$ , $R_L=100\Omega$ , unless noted)

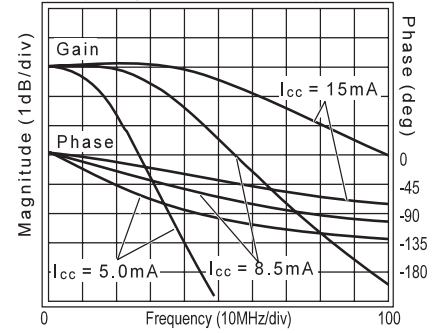
**Non-Inverting Frequency Response**



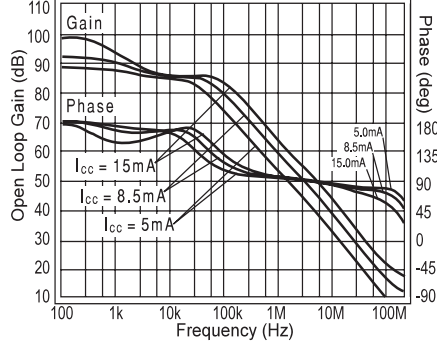
**Inverting Frequency Response**



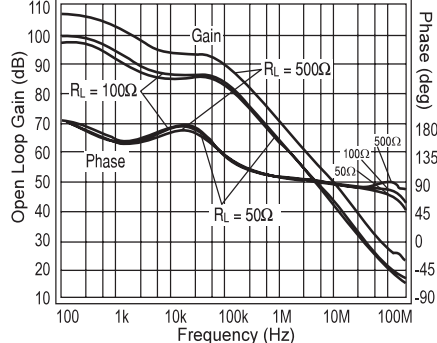
**Frequency Response vs.  $I_{CC}$  ( $A_v=+20$ )**



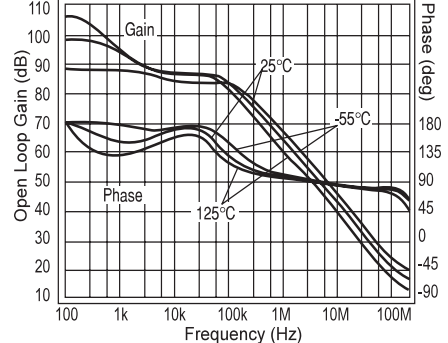
**Open Loop Gain and Phase vs.  $I_{CC}$**



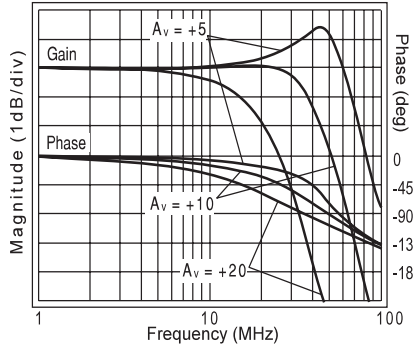
**Open Loop Gain and Phase vs.  $R_L$**



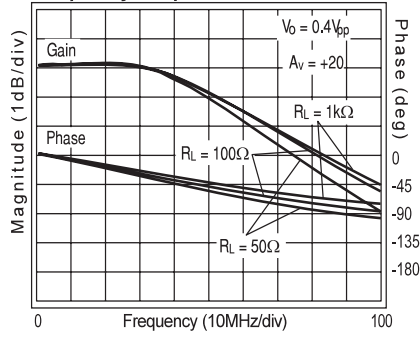
**Open Loop Gain and Phase vs. Temp**



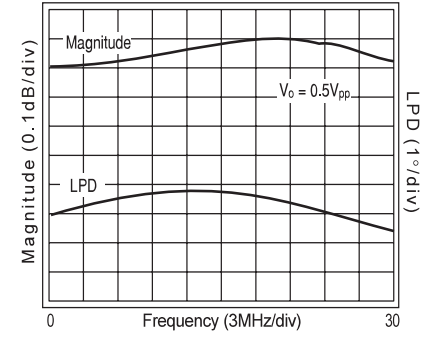
**Non-Inverting Response ( $I_{CC}=5.0\text{mA}$ )**



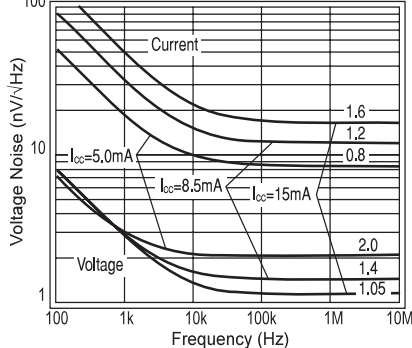
**Frequency Response for Various  $R_L$ s**



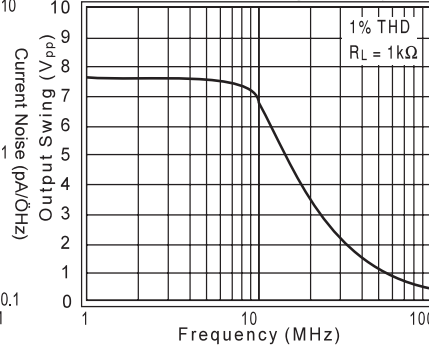
**Gain Flatness & Linear Phase Deviation**



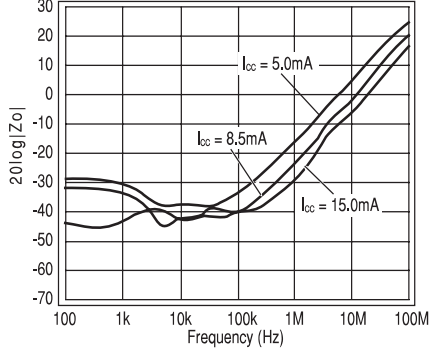
**Equivalent Input Noise**



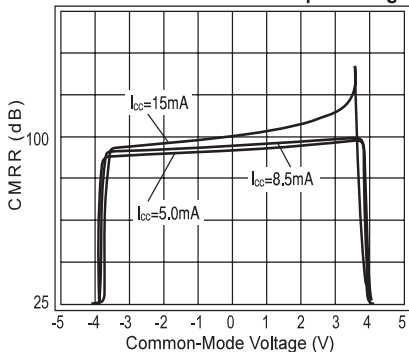
**Maximum Output Swing vs. Frequency**



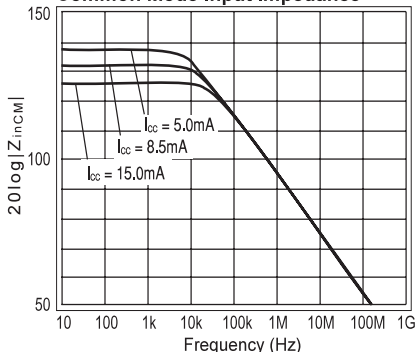
**Closed-Loop Output Impedance**



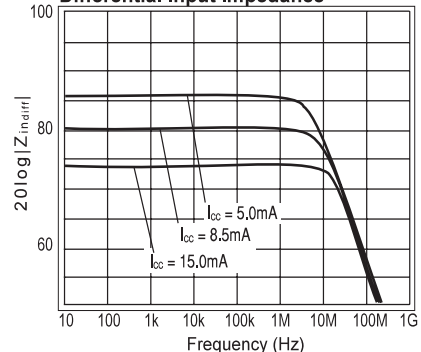
**CMRR vs Common-Mode Input Voltage**



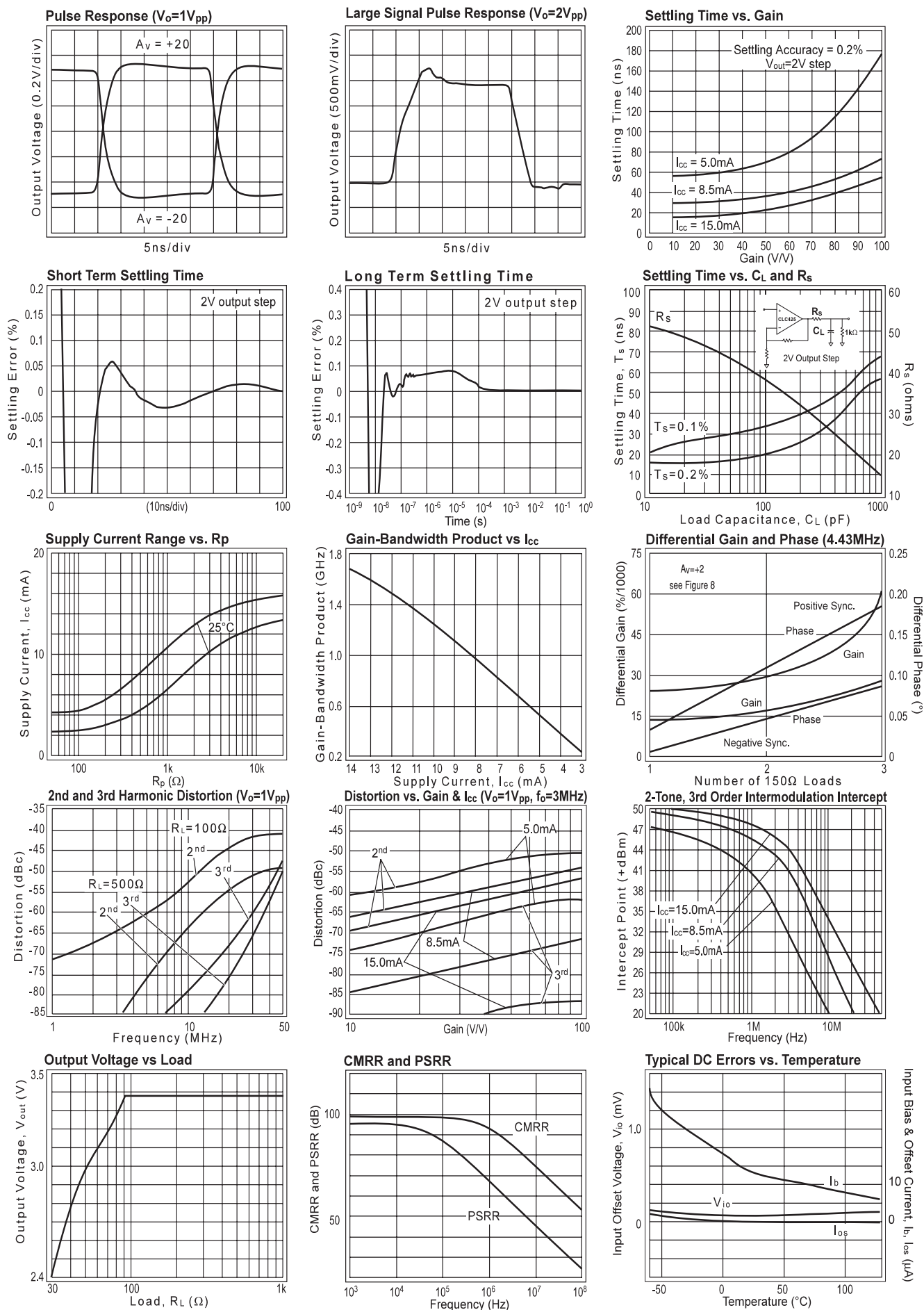
**Common Mode Input Impedance**

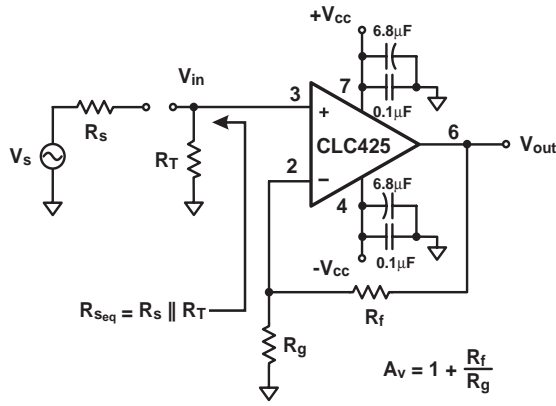


**Differential Input Impedance**



# CLC425 Typical Performance $(T_A=25^\circ\text{C}, V_{CC}=\pm 5\text{V}, R_G=26.1\Omega, R_I=499\Omega, R_L=100\Omega, \text{ unless noted})$





**Figure 1: Non-inverting Amplifier Configuration**

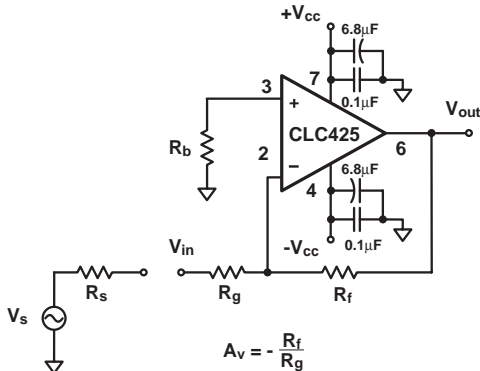
### Introduction

The CLC425 is a very wide gain-bandwidth, ultra-low noise voltage feedback operational amplifier which enables application areas such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high-frequency signal-to-noise ratios. The set of characteristic plots located in the "Typical Performance" section illustrates many of the performance trade-offs. The following discussion will enable the proper selection of external components in order to achieve optimum device performance.

### Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain-setting ( $R_g$ ) and feedback ( $R_f$ ) resistors should equal the equivalent source resistance ( $R_{seq}$ ) as defined in Figure 1. Combining this constraint with the non-inverting gain equation also seen in Figure 1, allows both  $R_f$  and  $R_g$  to be determined explicitly from the following equations:  $R_f = A_v R_{seq}$  and  $R_g = R_f / (A_v - 1)$ . When driven from a  $0\Omega$  source, such as that from the output of an op amp, the non-inverting input of the CLC425 should be isolated with at least a  $25\Omega$  series resistor.

As seen in Figure 2, bias current cancellation is accomplished for the inverting configuration by placing a resistor ( $R_b$ ) on the non-inverting input equal in value to the resistance seen by the inverting input ( $R_f || (R_g + R_s)$ ).  $R_b$  is recommended to be no less than  $25\Omega$  for best CLC425 performance. The additional noise contribution of  $R_b$  can be minimized through the use of a shunt capacitor.

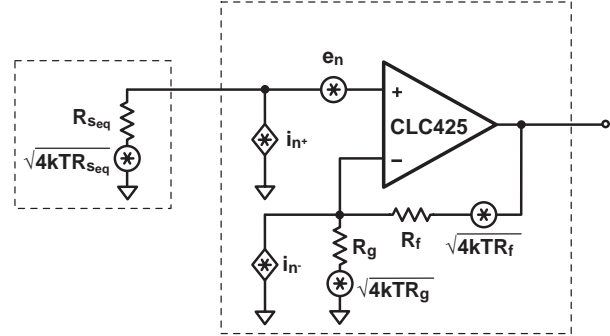


**Figure 2: Inverting Amplifier Configuration**

### Total Input Noise vs. Source Resistance

In order to determine maximum signal-to-noise ratios from the CLC425, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 3 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise ( $e_n$ ) and current noise ( $i_n = i_{n+} = i_{n-}$ ) sources, there also exists thermal voltage noise ( $e_t = \sqrt{4kTR}$ ) associated with each of the external resistors. Equation 1 provides the general form for total equivalent input voltage noise density ( $e_{ni}$ ). Equation 2 is a simplification of Equation 1 that assumes



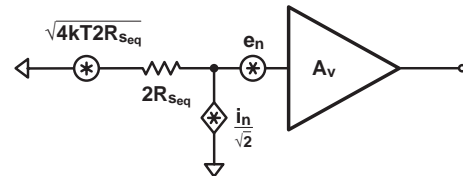
$$4kT = 16.4e - 21 \text{ Joules @ } 25^\circ\text{C}$$

**Figure 3: Non-inverting Amplifier Noise Model**

$$e_{ni} = \sqrt{e_n^2 + (i_{n+} R_{seq})^2 + 4kTR_{seq} + (i_{n-} (R_f || R_g))^2 + 4kT(R_f || R_g)}$$

**Equation 1: General Noise Equation**

$R_f || R_g = R_{seq}$  for bias current cancellation. Figure 4 illustrates the equivalent noise model using this assumption. Figure 5 is a plot of  $e_{ni}$  against equivalent source resistance ( $R_{seq}$ ) with all of the contributing voltage noise sources of Equation 2 shown. This plot gives the expected  $e_{ni}$  for a given  $R_{seq}$  which assumes  $R_f || R_g = R_{seq}$  for bias current cancellation. The total equivalent output voltage noise ( $e_{no}$ ) is  $e_{ni} * A_v$ .



**Figure 4: Noise Model with  $R_f || R_g = R_{seq}$**

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{seq})^2 + 4kT(2R_{seq})}$$

**Equation 2: Noise Equation with  $R_f || R_g = R_{seq}$**

As seen in Figure 5,  $e_{ni}$  is dominated by the intrinsic voltage noise ( $e_n$ ) of the amplifier for equivalent source resistances below  $33.5\Omega$ . Between  $33.5\Omega$  and  $6.43k\Omega$ ,  $e_{ni}$  is dominated by the thermal noise ( $e_t = \sqrt{4kTR_{seq}}$ ) of the external resistors. Above  $6.43k\Omega$ ,  $e_{ni}$  is dominated by the amplifier's current noise ( $\sqrt{2i_n R_{seq}}$ ). The point at which the CLC425's voltage noise and current noise contribute equally occurs for  $R_{seq} = 464\Omega$  (i.e.  $e_n / \sqrt{2i_n}$ ). As an example, configured with a gain of  $+20V/V$  giving a  $-3dB$  of  $90MHz$  and driven from an  $R_{seq} = 25\Omega$ , the CLC425 produces a total equivalent input noise voltage ( $e_{ni} * \sqrt{1.57 * 90MHz}$ ) of  $16.5\mu V_{rms}$ .

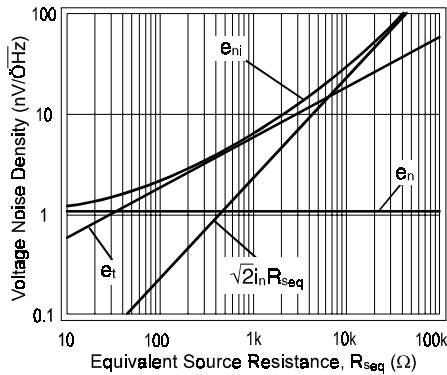


Figure 5: Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then  $R_f || R_g$  does not need to equal  $R_{seq}$ . In this case, according to Equation 1,  $R_f || R_g$  should be as low as possible in order to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration of Figure 2 if  $R_{seq}$  is replaced by  $R_b$  and  $R_g$  is replaced by  $R_g + R_s$ . With these substitutions, Equation 1 will yield an  $e_{ni}$  referred to the non-inverting input. Referring  $e_{ni}$  to the inverting input is easily accomplished by multiplying  $e_{ni}$  by the ratio of non-inverting to inverting gains.

### Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10 \log \left( \frac{S_i / N_i}{S_o / N_o} \right) = 10 \log \left( \frac{e_{ni}^2}{e_t^2} \right)$$

The Noise Figure formula is shown in Equation 3. The addition of a terminating resistor  $R_T$ , reduces the external thermal noise but increases the resulting NF. The NF is increased because  $R_T$  reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10 \log \left( \frac{e_n^2 + i_n^2 \left( R_{seq} + (R_f || R_g)^2 \right) + 4kTR_{seq} + 4kT(R_f || R_g)}{4kTR_{seq}} \right)$$

$R_{seq} = R_s$  for Unterminated Systems  
 $R_{seq} = R_s || R_T$  for Terminated Systems

Equation 3: Noise Figure Equation

The noise figure is related to the equivalent source resistance ( $R_{seq}$ ) and the parallel combination of  $R_f$  and  $R_g$ . To minimize noise figure, the following steps are recommended:

- Minimize  $R_f || R_g$
- Choose the optimum  $R_s$  ( $R_{OPT}$ )

$R_{OPT}$  is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \cong (e_n / i_n)$$

Figure 6 is a plot of NF vs  $R_s$  with  $R_f || R_g = 9.09$  ( $A_v = +10$ ). The NF curves for both Untermated and Terminated systems are shown. The Terminated curve assumes  $R_s = R_T$ . The table indicates the NF for various source resistances including  $R_s = R_{OPT}$ .

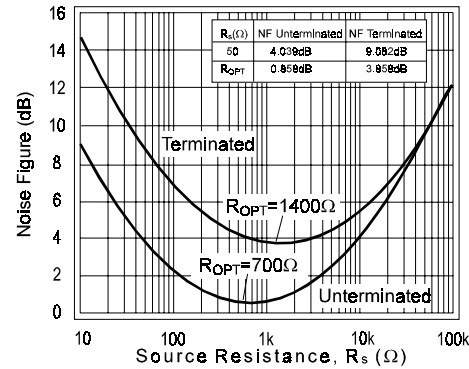


Figure 6: Noise Figure vs Source Resistance

### Supply Current Adjustment

The CLC425's supply current can be externally adjusted downward from its nominal value by adding an optional resistor ( $R_p$ ) between pin 8 and the negative supply as shown in Figure 7. Several of the plots found within the plot pages demonstrate the CLC425's behavior at different supply currents. The plot labeled " $I_{cc}$  vs.  $R_p$ " provides the means for selecting  $R_p$  and shows the result of standard IC process variation which is bounded by the  $25^\circ C$  curve.

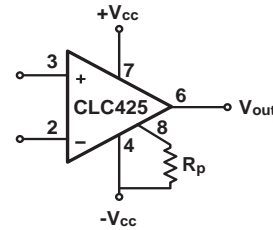


Figure 7: External Supply Current Adjustment

### Non-Inverting Gains Less Than 10V/V

Using the CLC425 at lower non-inverting gains requires external compensation such as the shunt compensation as shown in Figure 8. The quiescent supply current must also be reduced to 5mA with  $R_p$  for stability. The compensation capacitors are chosen to reduce frequency response peaking to less than 1dB. The plot in the "Typical Performance" section labeled "Differential Gain and Phase" shows the video performance of the CLC425 with this compensation circuitry.

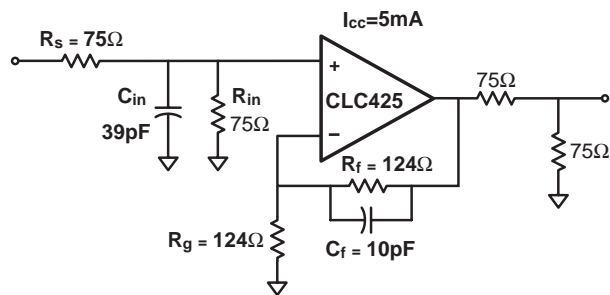


Figure 8: External Shunt Compensation

### Inverting Gains Less Than 10V/V

The lag compensation of Figure 9 will achieve stability for lower gains. Placing the network between the two input terminals does not affect the closed-loop nor noise gain, but is best used for the inverting configuration because of its affect on the non-inverting input impedance.

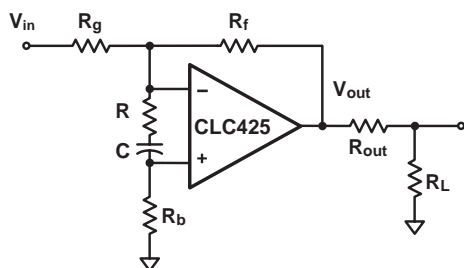


Figure 9: External Lag Compensation

### Single-Supply Operation

The CLC425 can be operated with single power supply as shown in Figure 10. Both the input and output are capacitively coupled to set the dc operating point.

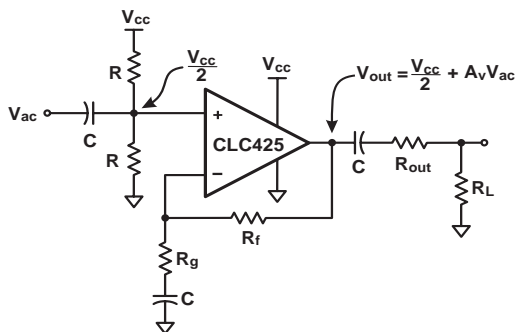


Figure 10: Single Supply Operation

### Low Noise Transimpedance Amplifier

The circuit of Figure 11 implements a low-noise transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by  $R_f$ . The simulated frequency response is shown in Figure 12 and shows the influence  $C_f$  has over gain flatness. Equation 4 provides the total input current noise density ( $i_{ni}$ ) equation for the basic transimpedance configuration and is plotted against feedback resistance ( $R_f$ ) showing all contributing noise sources in Figure 13. This plot indicates the expected total equivalent input current noise density ( $i_{ni}$ ) for a given feedback resistance ( $R_f$ ). The total equivalent output voltage noise density ( $e_{no}$ ) is  $i_{ni} * R_f$ .

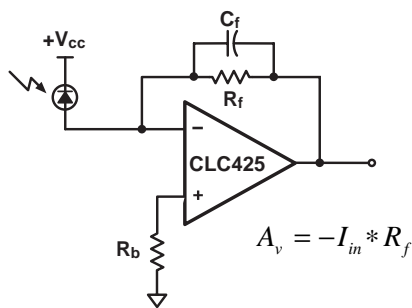


Figure 11: Transimpedance Amplifier Configuration

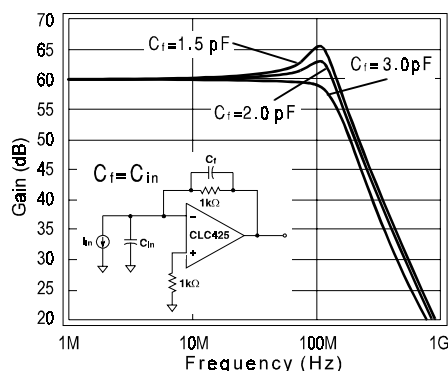


Figure 12: Transimpedance Amplifier Frequency Response

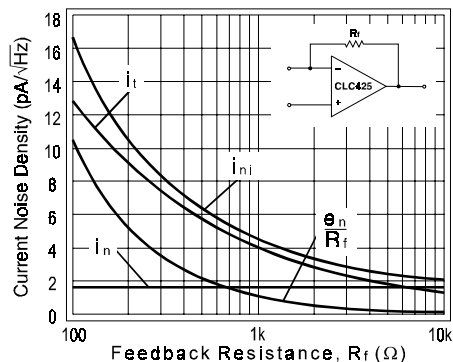


Figure 13: Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 4: Total Equivalent Input Referred Current

### Very Low Noise Figure Amplifier

The circuit of Figure 14 implements a very low Noise Figure amplifier using a step-up transformer combined with a CLC425 and a CLC404. The circuit is configured with a gain of 35.6dB. The circuit achieves measured Noise Figures of less than 2.5dB in the 10-40MHz region. 3<sup>rd</sup> order intercepts exceed +30dBm for frequencies less than 40MHz and gain flatness of 0.5dB is measured in the 1-50MHz pass bands. Application Note OA-14 provides greater detail on these low Noise Figure techniques.

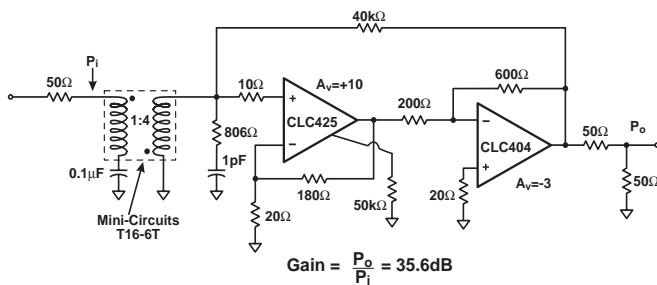


Figure 14: Very Low Noise Figure Amplifier

### Low Noise Integrator

The CLC425 implements a deBoo integrator shown in Figure 15. Integration linearity is maintained through positive feedback. The CLC425's low input offset voltage and matched inputs allowing bias current cancellation provide for very precise integration. Stability is maintained through the constraint on the circuit elements.

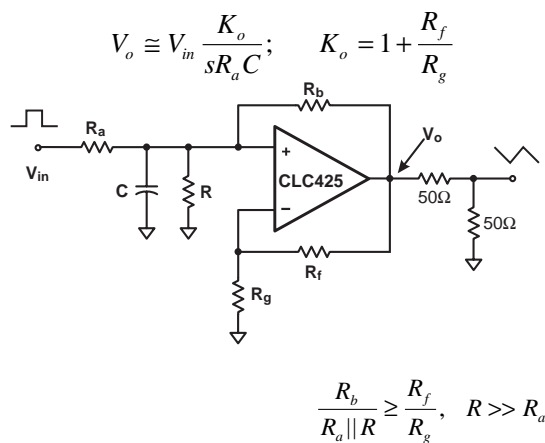


Figure 15: Low Noise Integrator

### High-Gain Sallen-Key Active Filters

The CLC425 is well suited for high-gain Sallen-Key type of active filters. Figure 16 shows the 2<sup>nd</sup> order Sallen-Key low pass filter topology. Using component predistortion methods as discussed in OA-21 enables the proper selection of components for these high-frequency filters.

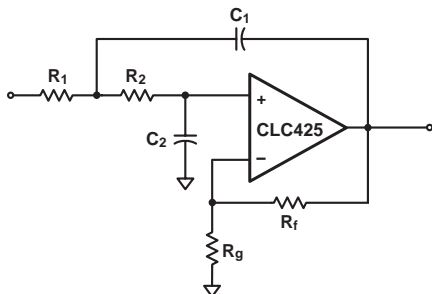


Figure 16: Sallen-Key Active Filter Topology

### Low Noise Magnetic Media Equalizer

The CLC425 implements a high-performance low-noise equalizer for such applications as magnetic tape channels as shown in Figure 17. The circuit combines an integrator with a bandpass filter to produce the low-noise equalization. The circuit's simulated frequency response is illustrated in Figure 18.

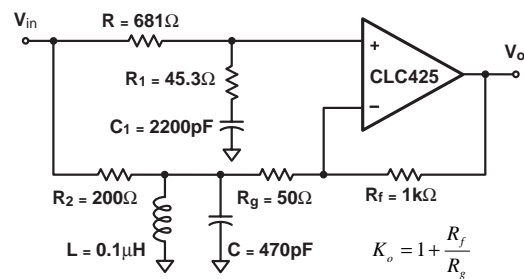


Figure 17: Low Noise Magnetic Media Equalizer

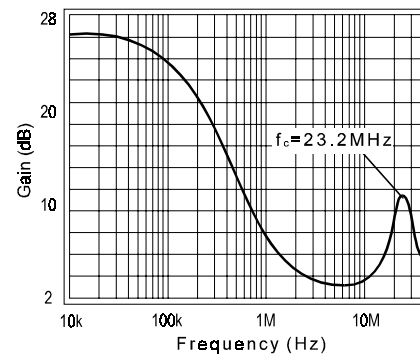


Figure 18: Equalizer Frequency Response

### Low-Noise Phase-Locked Loop Filter

The CLC425 is extremely useful as a Phase-Locked Loop filter in such applications as frequency synthesizers and data synchronizers. The circuit of Figure 19 implements one possible PLL filter with the CLC425.

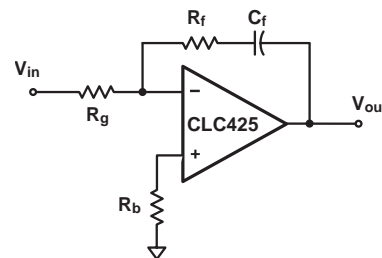


Figure 19: Phased-Locked Loop Filter

### Decreasing the Input Noise Voltage

The input noise voltage of the CLC425 can be reduced from its already low 1.05nV/√Hz by slightly increasing the supply current. Using a 50kΩ resistor to ground on pin 8, as shown in the circuit of Figure 14, will increase the quiescent current to ≈17mA and reduce the input noise voltage to < 0.95nV/√Hz.

### Printed Circuit Board Layout

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillation, see OA-15 for more information. National suggests the CLC730013-DIP, CLC730027-SOIC, or CLC730068-SOT evaluation board as a guide for high-frequency layout and as an aid in device testing and characterization.

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