



Peak EMI Reducing Solution

Features

- Generates an EMI optimized clock signal at output.
- Input frequency: 25 MHz.
- Frequency outputs:
 - USB Clock (48 MHz unmodulated)
 - 50 MHz (modulated), $\pm 1\%$ centre spread
- Modulation rate: 39 KHz.
- Spread Spectrum ON/OFF control
- Supply voltage range $2.5V \pm 5\%$.
- Available in 8-pin SOIC package.
- Commercial Temperature range.

Product Description

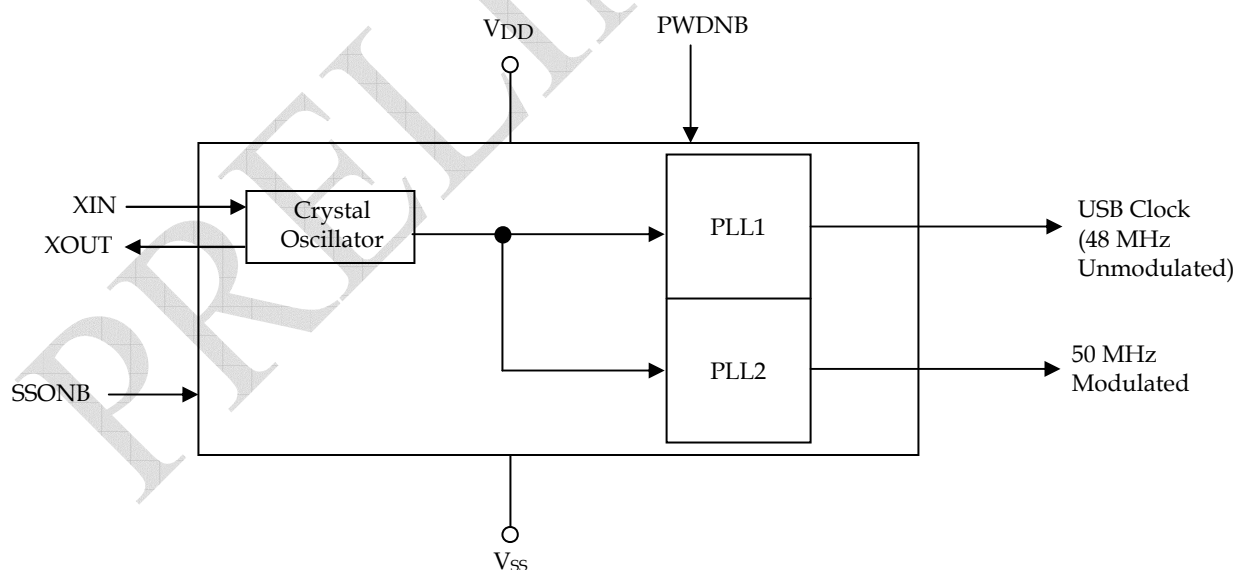
The ASM3P2853A is a versatile spread spectrum frequency modulator. The ASM3P2853A reduces electromagnetic interference (EMI) at the clock source. The ASM3P2853A allows significant system cost savings by reducing the number of circuit board layers and

shielding that are required to pass EMI regulations. The ASM3P2853A modulates the output of PLL in order to spread the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation.

Applications

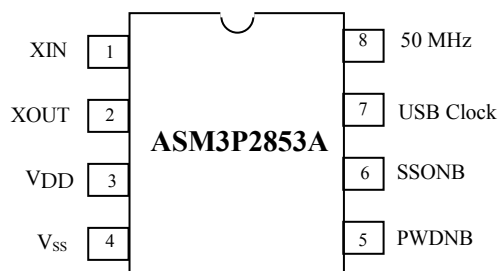
ASM3P2853A is targeted towards EMI management for high speed digital applications such as PC peripheral devices, consumer electronics and embedded controller systems.

Block Diagram





Pin Configuration



Pin Description

Pin Name	Type	Description
XIN	I	Connection to crystal or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
XOUT	O	Connection to crystal. If using an external reference clock, this pin must be left unconnected.
V _{DD}	P	Power supply for the analog and digital blocks
V _{SS}	P	Ground to entire chip.
PWDNB	I	Power-down control pin. Pull low to enable the power-down mode. Connect to VDD, if not used.
SSONB	I	Digital logic input used to enable spread spectrum function (Active LOW). Spread spectrum is enabled when LOW, disabled when HIGH.
USB Clock	O	Clock output -1 (48 MHz unmodulated)
50 MHz	O	Clock output -2 (50 MHz modulated)

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Unit
V_{DD}	Supply voltage, DC	$(V_{SS} - 0.5)$ to 7	V
V_I	Input voltage, DC	$(V_{SS}-0.5)$ to $(V_{DD}+0.5)$	V
V_O	Output voltage, DC	$(V_{SS}-0.5)$ to $(V_{DD} + 0.5)$	V
I_{IK}	Input clamp current ($V_I < 0$ or $V_I > V_{DD}$)	-50 to +50	mA
I_{OK}	Output clamp current ($V_I < 0$ or $V_I > V_{DD}$)	-50 to +50	mA
T_J	Junction temperature	150	°C
	Lead temperature (soldering 10 sec)	260	°C
	Input static discharge voltage protection (MIL –STD 883E, Method 3015.7)	2	kV

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Conditions

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	$2.5V \pm 5\%$	2.375	2.5	2.625	V
Ambient Operating Temperature Range	T_A		0	-	+70	°C
Crystal Resonator Frequency	F_{XIN}		25			MHz
Output Driver Load Capacitance	C_L		-	-	15	pF

Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	25 MHz
Frequency tolerance	± 50 ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω



DC Electrical Characteristics

Parameter	Symbol	Conditions / Description	Min	Typ	Max	Unit
Overall						
Supply Current, Dynamic	I_{DD}	$V_{DD}=2.5V$, $F_{XIN}=25MHz$, $C_L=15pF$	15	20	25	mA
Supply Current, Static	I_{DDL}	$V_{DD} = 2.5V$, $X_{IN} = 0$, $PWDNB = 0$	-	1.5	-	mA
All input pins						
High-Level Input Voltage	V_{IH}	$V_{DD}=2.5V$	1.7	-	-	V
Low-Level Input Voltage	V_{IL}	$V_{DD}=2.5V$	-	-	0.7	V
High-Level Input Current	I_{IH}		-	-	25	μA
Low-Level Input Current (pull-up)	I_{IL}		-	-	-25	μA
Clock Outputs						
High-Level Output Source Current	I_{xOH}	$V_{DD} = 2.5V$, $V(X_{IN}) = 0$, $V_O=2V$	-10	-12	-15	mA
Low-Level Output Sink Current	I_{xOL}	$V_{DD}= V(X_{IN}) = 2.5V$, $V_O=0.4V$	10	12	15	mA
High-Level Output Source Current	I_{OH}	$V_O=2V$	-	8	-	mA
Low-Level Output Sink Current	I_{OL}	$V_O=0.4V$	-	8	-	mA
Output Impedance	Z_O		-	42	-	Ω

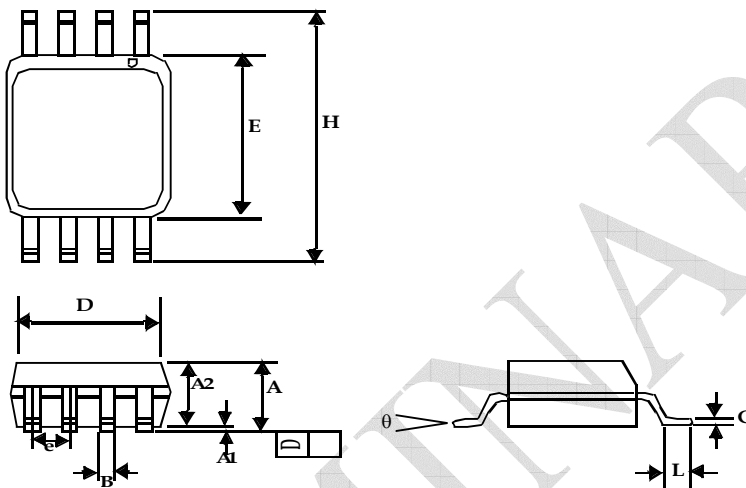


AC Electrical Characteristics

Parameter	Symbol	Conditions/ Description	Min	Typ	Max	Unit
Rise Time*	t_r	Measured from 20% to 80% of the signal level	-	2	-	nS
Fall Time*	t_f	Measured from 80% to 20% of the signal level	-	1.2	-	nS
Jitter (Cycle to Cycle)	t_{jc}		-	-	200	pS
Jitter (Period)	t_p		-	175	-	pS
Clock Duty Cycle	t_d	Ratio of pulse width (as measured from rising edge to next falling edge at VDD/2) to one clock period	45	50	55	%
* C_L = 15 pF, Input clock frequency = 25 MHz						



8-Pin SOIC package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°



Ordering Codes

Part number	Package Configuration	Temperature Range
ASM3P2853AF-08-ST	8-pin SOIC ,TUBE	Commercial
ASM3P2853AF-08-SR	8-pin SOIC, TAPE & REEL	Commercial

Ordering Information

A S M 3 P 2 8 5 3 A F - 0 8 - S R

OR - SOT23/T/R
 TT - TSSOP, TUBE
 TR - TSSOP, T/R
 QT - QFN, TUBE
 BT - BGA, TUBE
 BR - BGA, T/R

ST - SOIC, TUBE
 SR - SOIC, T/R
 QR - QFN, T/R
 VT - TVSOP, TUBE
 VR - TVSOP, T/R
 JR - SSOP, T/R
 JT - SSOP, TUBE

PIN COUNT

Pb FREE

PART NUMBER

X = Automotive (-40C to +125C) I = Industrial (-40C to +85C) P or n/c = Commercial (0C to +70C)

1 - reserved 6 - power management
 2 - Non PLL based 7 - power management
 3 - EMI Reduction 8 - power management
 4 - DDR support products 9 - Hi performance

Alliance Semiconductor Mixed Signal Product



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Preliminary Information
Part Number: ASM3P2853A
Document Version: v0.7

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

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