+2.7 V to +5.5 V, I²C INTERFACE, VOLTAGE OUTPUT, 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Micropower Operation: 140 µA @ 5 V**
- **Power-On Reset to Zero**
- **+2.7-V to +5.5 V-Power Supply**
- **Specified Monotonic by Design**
- **Settling Time: 10 µs to ±0.003%FS**
- **I²C™ Interface up to 3.4 Mbps**
- **On-Chip Output Buffer Amplifier, Rail-to-Rail Operation**
- **Double-Buffered Input Register**
- **Address Support for up to Two DAC7571s**
- **Small 6 Lead SOT Package**
- **Operation From –40°C to 105°C**

APPLICATIONS

- **Process Control**
- **Data Acquistion Systems**
- **Closed-Loop Servo Control**
- **PC Peripherals**
- **Portable Instrumentation**

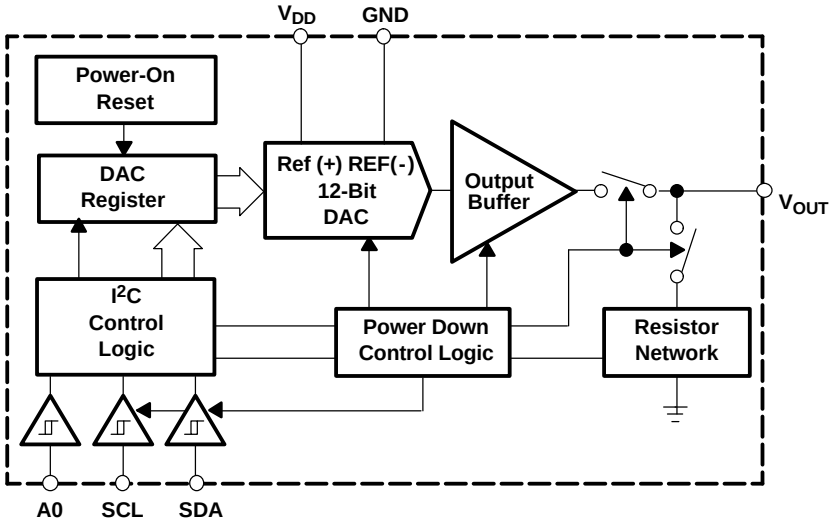
DESCRIPTION

The DAC7571 is a low-power, single channel, 12-bit buffered voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC7571 utilizes an I²C compatible two wire serial interface that operates at clock rates up to 3.4 Mbps with address support of up to two DAC7571s on the same data bus.

The output voltage range of the DAC is set to V_{DD}. The DAC7571 incorporates a power-on-reset circuit that ensures that the DAC output powers up at zero volts and remains there until a valid write to the device takes place. The DAC7571 contains a power-down feature, accessed via the internal control register, that reduces the current consumption of the device to 50 nA at 5 V.

The low power consumption of this part in normal operation makes it ideally suited for portable battery operated equipment. The power consumption is less than 0.7 mW at V_{DD} = 5 V reducing to 1 µW in power-down mode.

The DAC7571 is available in a 6-lead SOT 23 package.

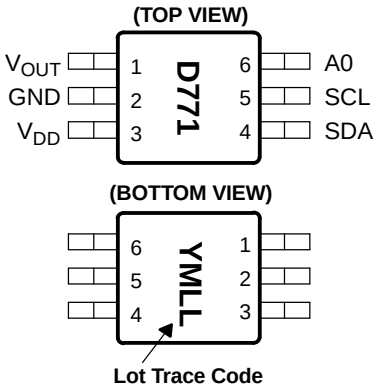


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC7571	SOT23-6	DBV	-40°C to +105°C	D771	DAC7571IDBVT	250 Piece Small Tape and Reel
					DAC7571IDBVR	3000 Piece Tape and Reel

PIN CONFIGURATIONS



PIN DESCRIPTION (SOT23-6)

PIN	NAME	DESCRIPTION
1	V_{OUT}	Analog output voltage from DAC
2	GND	Ground reference point for all circuitry on the part
3	V_{DD}	Analog Voltage Supply Input
4	SDA	Serial Data Input
5	SCL	Serial Clock Input
6	A0	Device Address Select
LOT TRACE CODE:	**Y**ear (3 = 2003); **M**onth (1–9 = JAN–SEP; A=OCT, B=NOV, C=DEC); **LL**– Random code generated when assembly is requested	

ABSOLUTE MAXIMUM RATINGS(1)

		UNITS
V_{DD} to GND		-0.3V to +6V
Digital Input voltage to GND		-0.3 V to +V_{DD} + 0.3 V
V_{OUT} to GND		-0.3 V to +V_{DD} + 0.3 V
Operating temperature range		-40°C to + 105°C
Storage temperature range		-65°C to + 150°C
Junction temperature range (T_J max)		+ 150°C
Power dissipation		($T_J$max - T_A)$R_{\Theta JA}$
Thermal impedance, $R_{\Theta JA}$		240°C/W
Lead temperature, soldering	Vapor phase (60s)	215°C
	Infrared (15s)	220°C

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications -40°C to +105°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7571			UNITS
		MIN	TYP	MAX	
STATIC PERFORMANCE(1)					
Resolution		12			Bits
Relative accuracy				±0.195	% of FSR
Differential nonlinearity	Assured monotonic by design			±1	LSB
Zero code error	All zeroes loaded to DAC register		5	20	mV

(1) Linearity calculated using a reduced code range of 48 to 4047; output unloaded.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = +2.7 V to +5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications -40°C to +105°C unless otherwise noted.

PARAMETER	CONDITIONS	DAC7571			UNITS
		MIN	TYP	MAX	
Full-scale error	All ones loaded to DAC register		-0.15	-1.25	% of FSR
Gain error				±1.25	% of FSR
Zero code error drift			±7		µV/°C
Gain temperature coefficient			±3		ppm of FSR/°C
OUTPUT CHARACTERISTICS(2)					
Output voltage range		0		V_{DD}	V
Output voltage settling time	1/4 Scale to 3/4 scale change (400_H to $C00_H$)		8	10	µ s
Slew rate			1		V/µs
Capacitive load stability	R_L =∞		470		pF
	R_L = 2kΩ		1000		pF
Code change glitch impulse	1 LSB Change around major carry		20		nV-s
Digital feedthrough			0.5		nV-s
DC output impedance			1		Ω
Short-circuit current	V_{DD} = +5V		50		mA
	V_{DD} = +3V		20		mA
Power-up time	Coming out of power-down mode, V_{DD} = +5V		2.5		µ s
	Coming out of power-down mode, V_{DD} = +3V		5		µ s
LOGIC INPUTS(3)					
Input current				± 1	µ A
V_{IN}L, Input low voltage	V_{DD} = +3V			0.3×V_{DD}	V
V_{IN}H, Input high voltage	V_{DD} = +5V	0.7×V_{DD}			V
Pin capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD} (normal operation)	DAC active and excluding load current				
V_{DD} = +3.6V to +5.5V	V_{IH} = V_{DD} and V_{IL} = GND		135	200	µ A
V_{DD} = +2.7V to +3.6V	V_{IH} = V_{DD} and V_{IL} = GND		115	160	µ A
I_{DD} (all power-down modes)					
V_{DD} = +3.6 V to +5.5 V	V_{IH} = V_{DD} and V_{IL} = GND		0.2	1	µ A
V_{DD} = +2.7V to +3.6V	V_{IH} = V_{DD} and V_{IL} = GND		0.05	1	µ A
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2mA, V_{DD} = +5V		93		%

(2) Specified by design and characterization, not production tested.
(3) Specified by design and characterization, not production tested.

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		High-speed mode, C_B - 100pF max			3.4	MHz
		High-Speed mode, C_B - 400pF max			1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HD}; t_{STA}	Hold Time (Repeated) START Condition	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode	160			ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
		High-speed mode, C_B - 100pF max	160			ns
		High-speed mode, C_B - 400pF max	320			ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode, C_B - 100pF max	60			ns
		High-speed mode, C_B - 400pF max	120			ns
t_{SU}; t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7			µs
		Fast mode	600			ns
		High-speed mode	160			ns
t_{SU}; t_{DAT}	Data Setup Time	Standard mode	250			ns
		Fast mode	100			ns
		High-speed mode	10			ns
t_{HD}; t_{DAT}	Data Hold Time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
		High-speed mode, C_B - 100pF max	0		70	ns
		High-speed mode, C_B - 400pF max	0		150	ns
t_{RCL}	Rise Time of SCL Signal	Standard mode			1000	ns
		Fast mode	$20 + 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		40	ns
		High-speed mode, C_B - 400pF max	20		80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode			1000	ns
		Fast mode	$20 + 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		80	ns
		High-speed mode, C_B - 400pF max	20		160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode			300	ns
		Fast mode	$20 + 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		40	ns
		High-speed mode, C_B - 400pF max	20		80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode			1000	ns
		Fast mode	$20 + 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		80	ns
		High-speed mode, C_B - 400pF max	20		160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode			300	ns
		Fast mode	$20 + 0.1C_B$		300	ns
		High-speed mode, C_B - 100pF max	10		80	ns
		High-speed mode, C_B - 400pF max	20		160	ns

TIMING CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{SU}; t_{STO}	Setup Time for STOP Condition	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode	160			ns
C_B	Capacitive Load for SDA and SCL				400	pF
t_{SP}	Pulse Width of Spike Suppressed	Fast mode			50	ns
		High-speed mode			10	ns
V_{NH}	Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	Standard mode	$0.2V_{DD}$			V
		Fast mode				
		High-speed mode				
V_{NL}	Noise Margin at the LOW Level for Each Connected Device (Including Hysteresis)	Standard mode	$0.1V_{DD}$			V
		Fast mode				
		High-speed mode				

TYPICAL CHARACTERISTICS: V_{DD} = +5 V

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (-40°C)

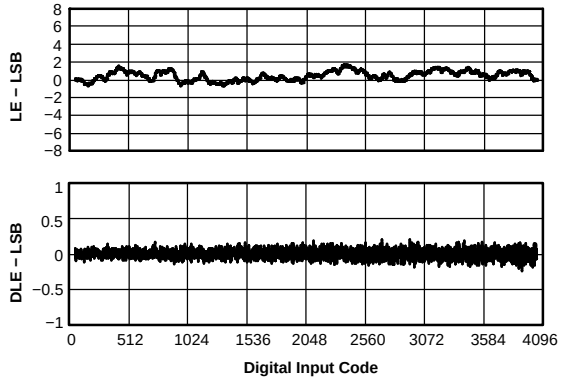


Figure 1.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+25 ° C)

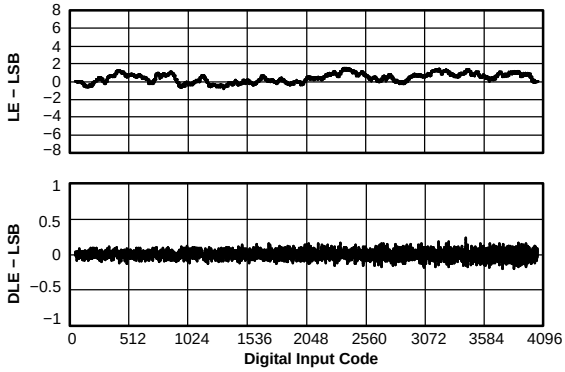


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+105° C)

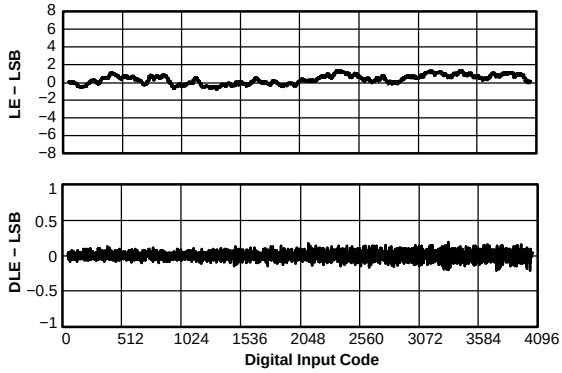


Figure 3.

TYPICAL TOTAL UNADJUSTED ERROR

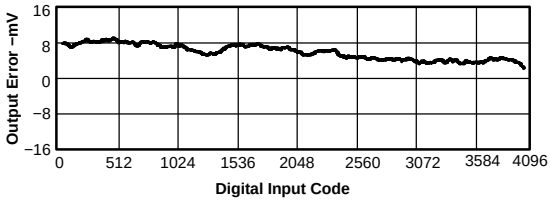


Figure 4.

ZERO-SCALE ERROR VS TEMPERATURE

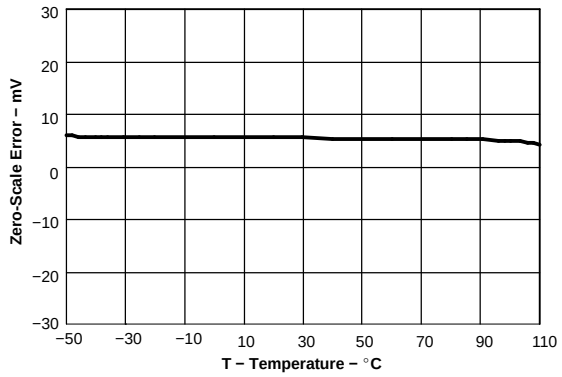


Figure 5.

FULL-SCALE ERROR VS TEMPERATURE

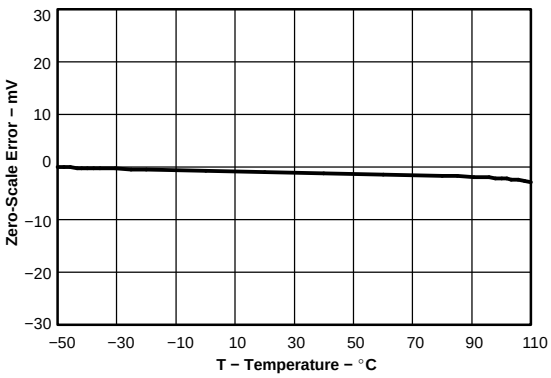


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

I_{DD} HISTOGRAM

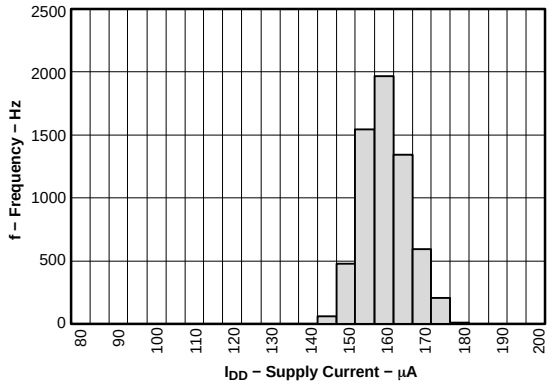


Figure 7.

SOURCE AND SINK CURRENT CAPABILITY

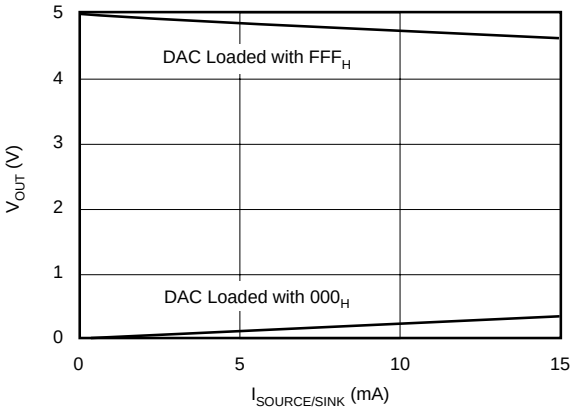


Figure 8.

SUPPLY CURRENT vs CODE

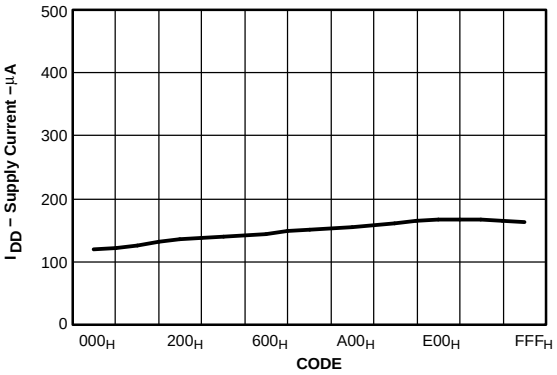


Figure 9.

SUPPLY CURRENT vs TEMPERATURE

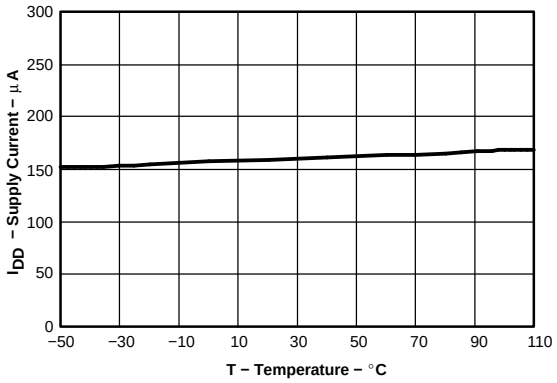


Figure 10.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

SUPPLY CURRENT vs SUPPLY VOLTAGE

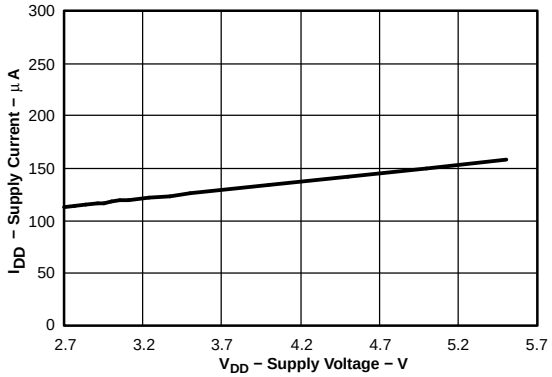


Figure 11.

POWER-DOWN CURRENT vs SUPPLY VOLTAGE

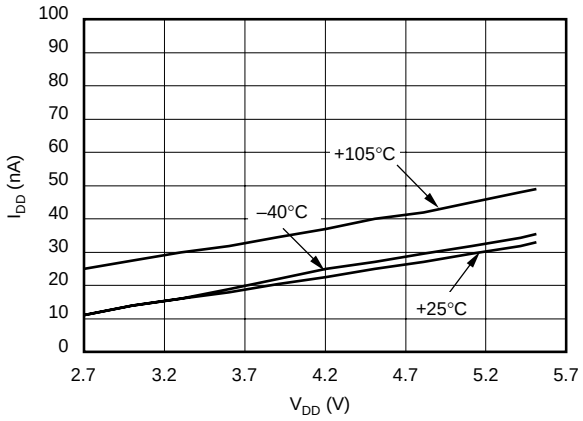


Figure 12.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

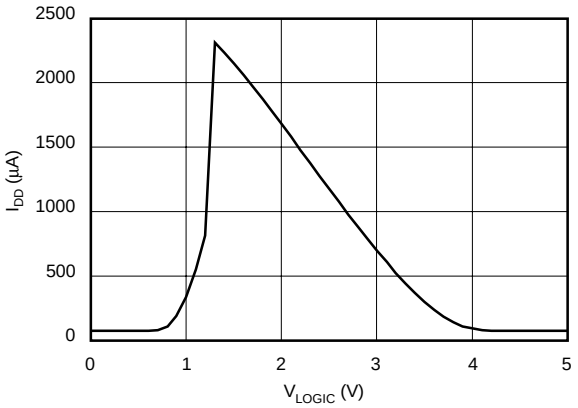


Figure 13.

FULL-SCALE SETTLING TIME

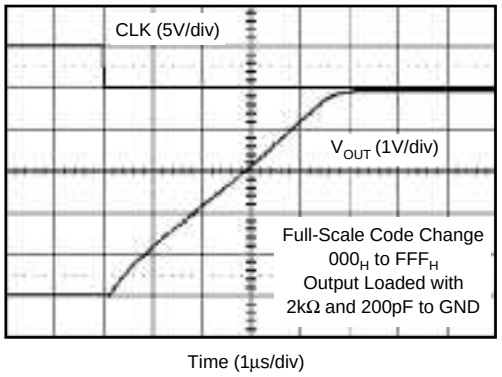


Figure 14.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

FULL-SCALE SETTLING TIME

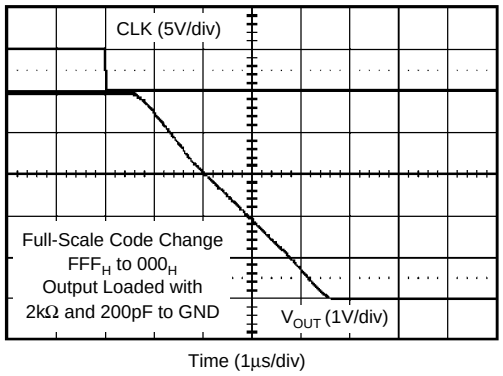


Figure 15.

HALF-SCALE SETTLING TIME

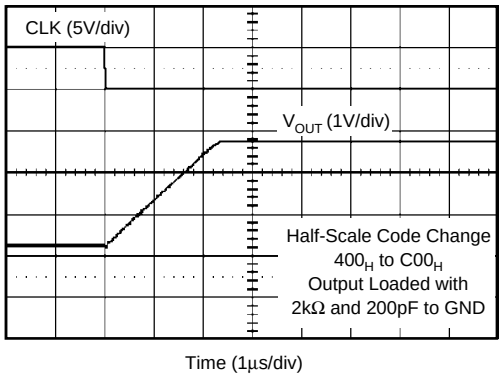


Figure 16.

HALF-SCALE SETTLING TIME

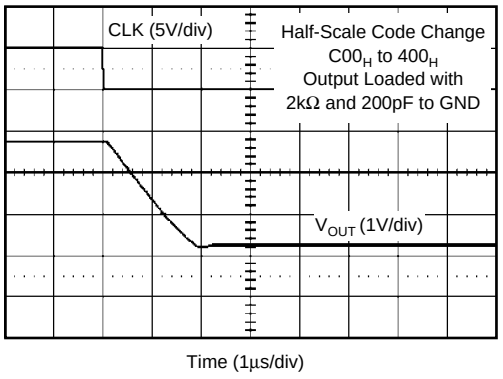


Figure 17.

POWER-ON RESET TO 0V

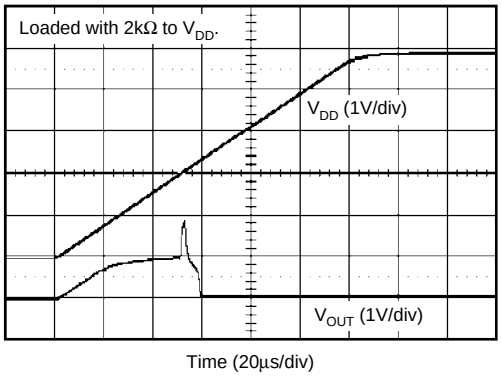


Figure 18.

EXITING POWER-DOWN (800$_H$Loaded)

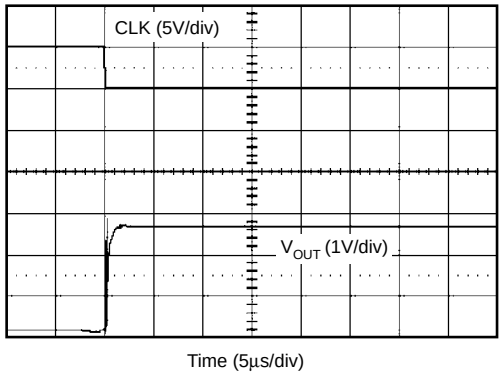


Figure 19.

CODE CHANGE GLITCH

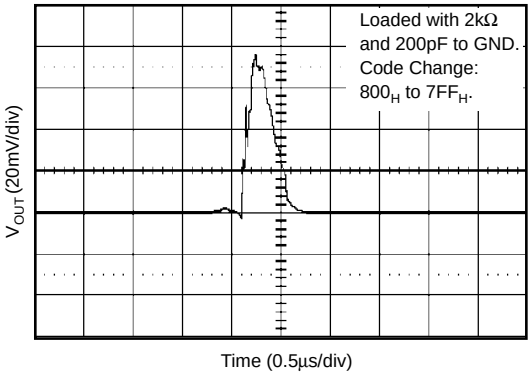


Figure 20.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At T_A = +25°C, +V_{DD} = +2.7V, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (-40 °C)

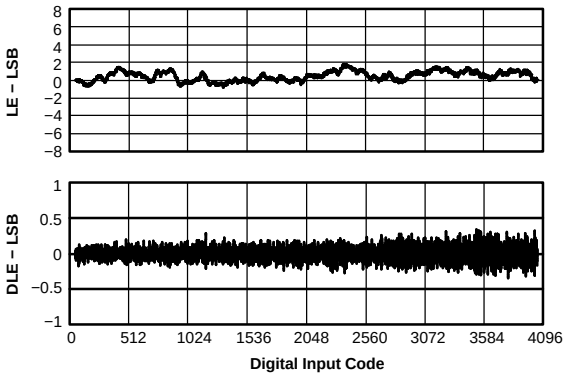


Figure 21.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+25 °C)

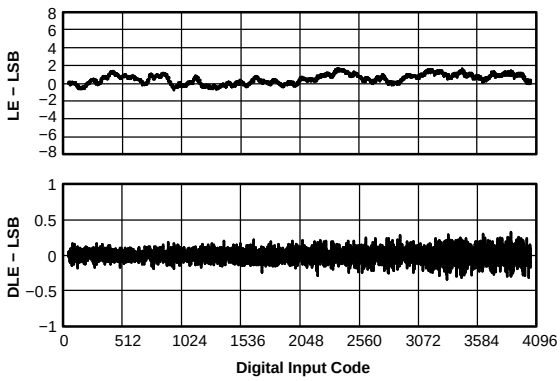


Figure 22.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS CODE (+105 °C)

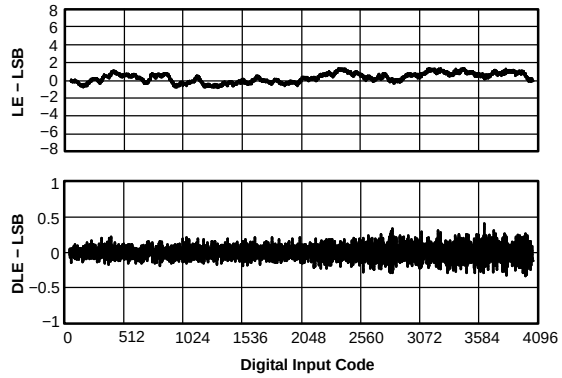


Figure 23.

ABSOLUTE ERROR

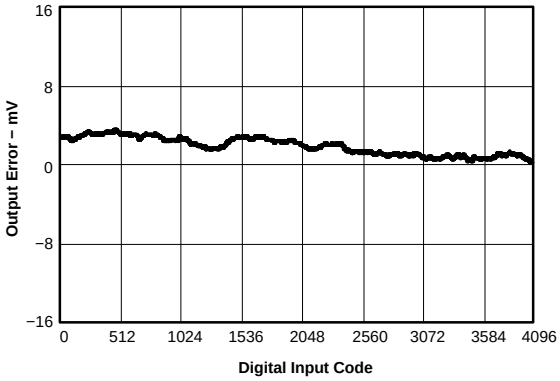


Figure 24.

ZERO-SCALE ERROR VS TEMPERATURE

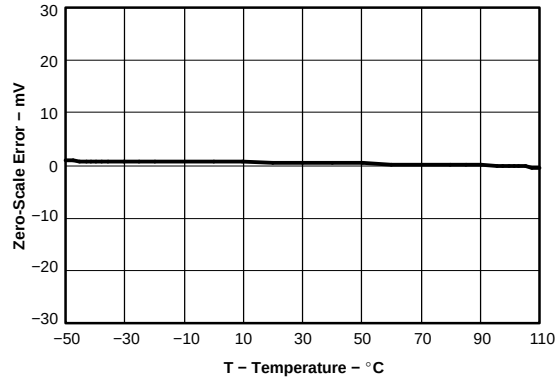


Figure 25.

FULL-SCALE ERROR VS TEMPERATURE

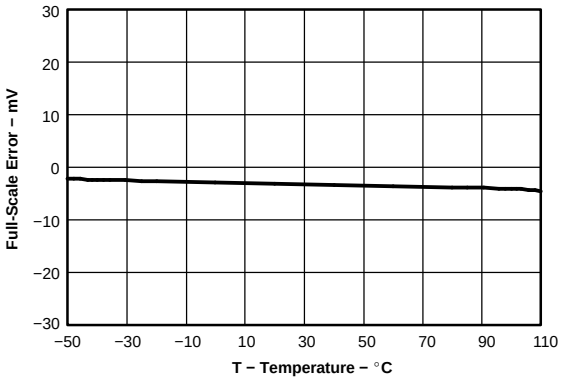


Figure 26.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

I_{DD} HISTOGRAM

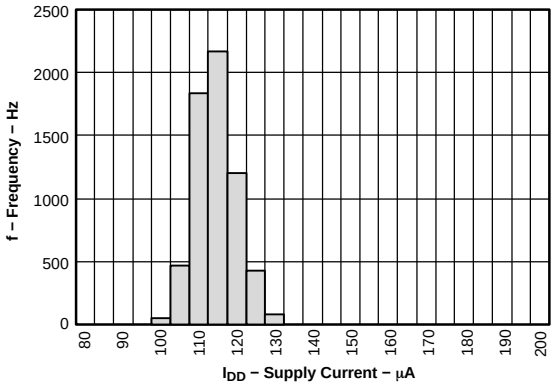


Figure 27.

SOURCE AND SINK CURRENT CAPABILITY

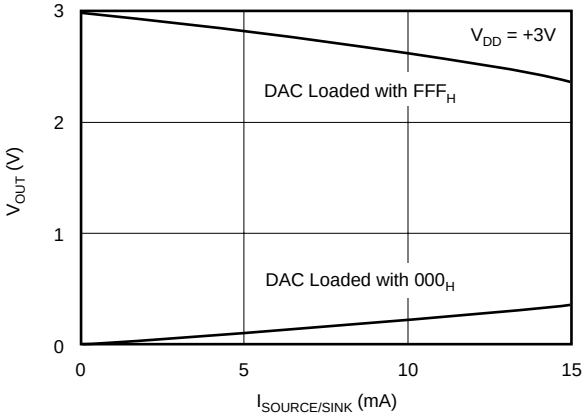


Figure 28.

SUPPLY CURRENT vs CODE

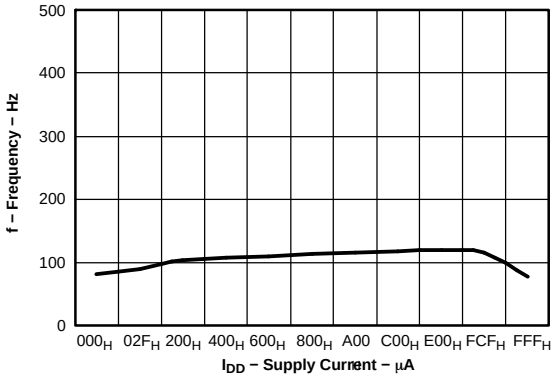


Figure 29.

SUPPLY CURRENT vs 9 TEMPERATURE

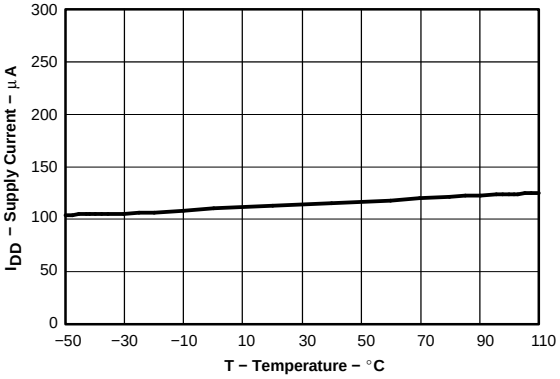


Figure 30.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

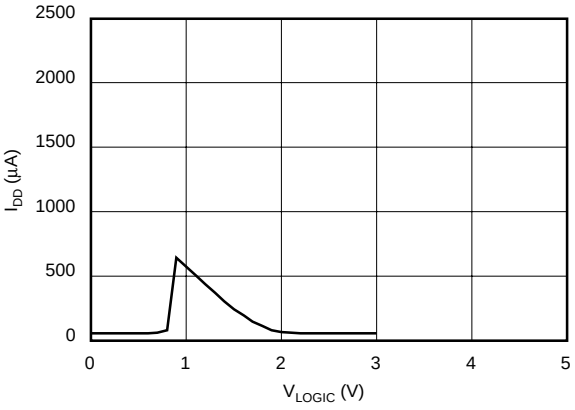


Figure 31.

FULL SCALE SETTLING TIME

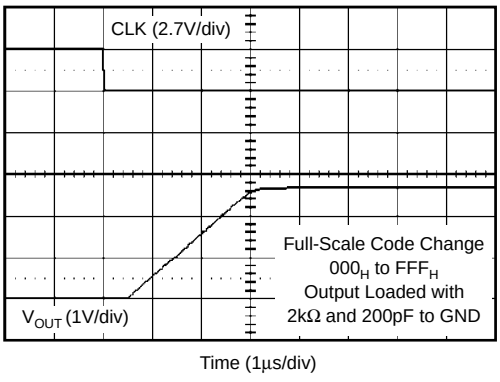


Figure 32.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

FULL SCALE SETTLING TIME

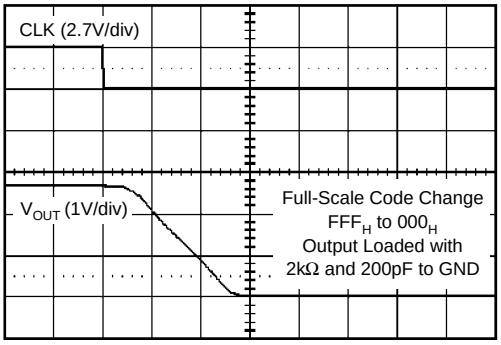


Figure 33.

HALF SCALE SETTLING TIME

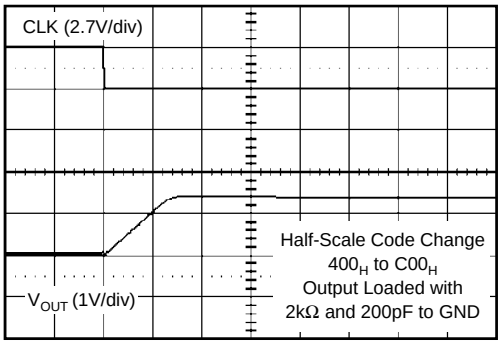


Figure 34.

HALF SCALE SETTLING TIME

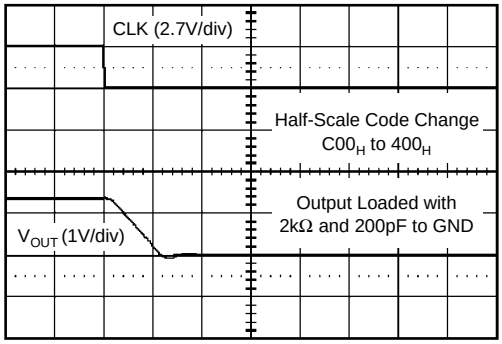


Figure 35.

POWER ON RESET 0 V

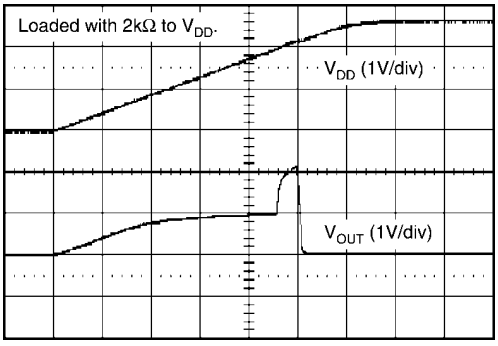


Figure 36.

EXITING-POWER DOWN (800$_H$Loaded)

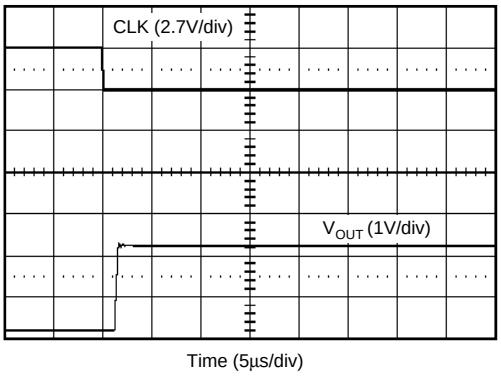


Figure 37.

CODE CHANGE GLITCH

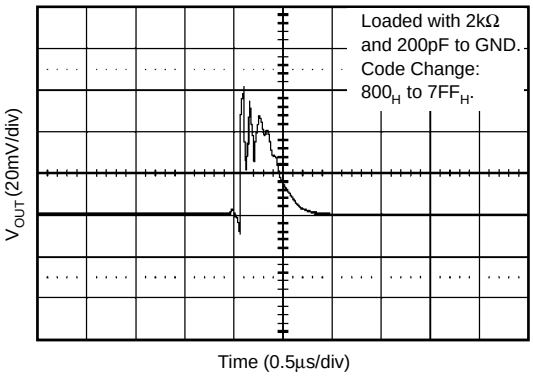


Figure 38.

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC7571 consists of a string DAC followed by an output buffer amplifier. Figure 39 shows a block diagram of the DAC architecture.

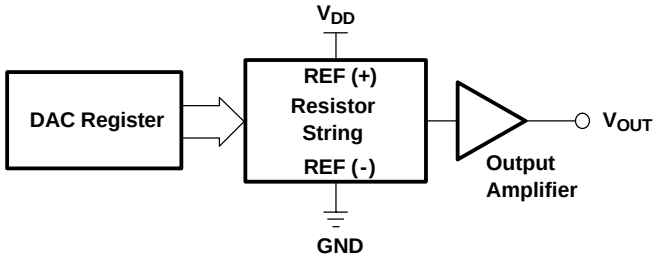


Figure 39. R-String DAC Architecture

The input coding to the DAC7571 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = V_{DD} \times \frac{D}{4096}$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 4095.

RESISTOR STRING

The resistor string section is shown in Figure 40. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is ensured monotonic because it is a string of resistors. The negative tap of the resistor string is tied to GND. The positive tap of the resistor string is tied to V_{DD}.

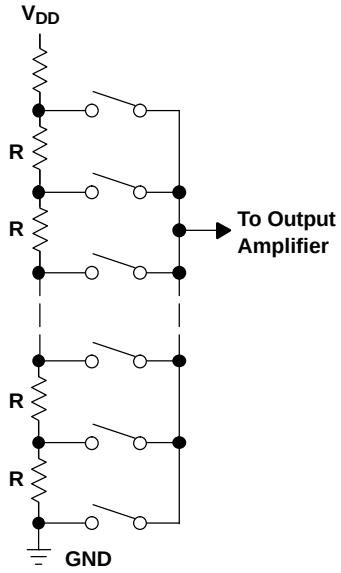


Figure 40. Resistor String

THEORY OF OPERATION (continued)

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics. The slew rate is 1V/µs with a half-scale settling time of 8 µs with the output unloaded.

I²C Interface

The DAC7571 uses an I²C interface as defined by Philips Semiconductor to receive data in slave mode (see I²C-Bus Specification, Version 2.1, January 2000). The DAC7571 supports the following data transfer modes, described in the I²C-Bus Specification: Standard Mode (100 kbit/s), Fast Mode (400 kbit/s) and High-Speed Mode (3.4 Mbit/s). Ten-bit addressing and general call addres are *not* supported.

For simplicity, standard mode and fast mode are referred to as F/S-mode and high-speed mode is referred tg as HS-mode.

The 2-wire I²C serial bus protocol operates as follows:

- The *Master* initiates data transfer by establishing a *Start* condition. The *Start* condition is defined when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 41. The byte following the start condition is the address byte consisting of the 7-bit slave address followed by the $\overline{W}$ bit.

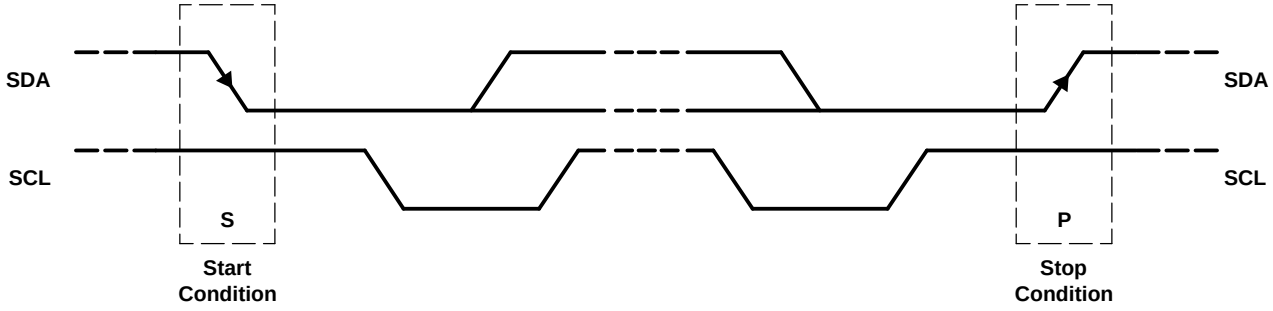


Figure 41. START and STOP Conditions

- The addressed *Slave* responds by pulling the SDA pin low during the ninth clock pulse, termed the *Acknowledge* bit (see Figure 42). At this stage all other devices on the bus remain idle while the selected device waits for data to be written to its shift register.

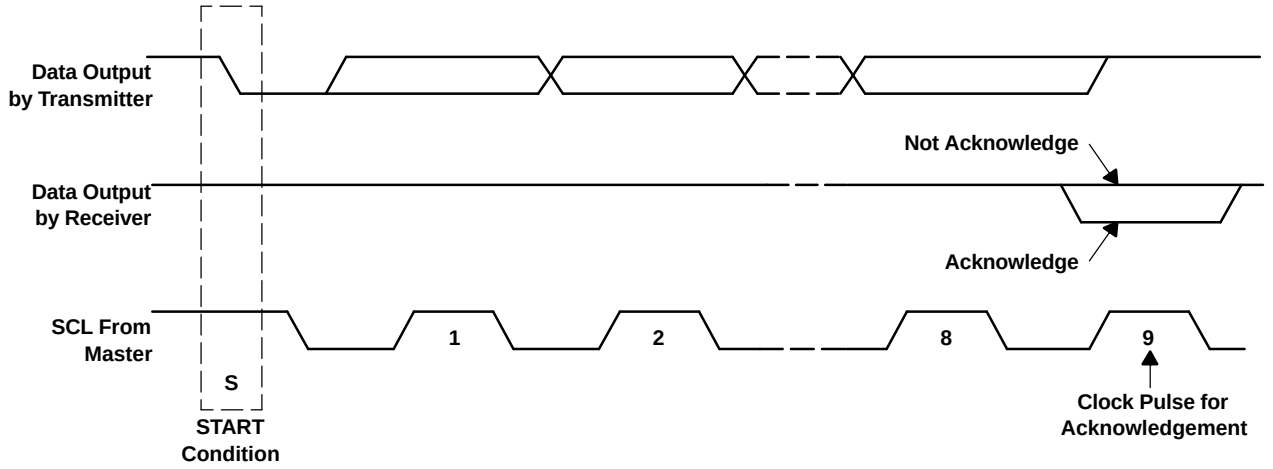


Figure 42. Acknowledge on the I²C Bus

- Data is transmitted over the serial bus in sequences of nine clock cycles (8 data bits followed by an acknowledge bit. The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 43).

THEORY OF OPERATION (continued)

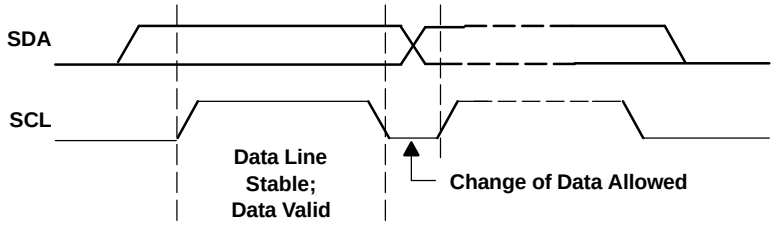


Figure 43. Bit Transfer on the I^2C Bus

- When all data bits have been written, a *Stop* condition is established (see Figure 44). In writing to the DAC7571, the master must pull the SDA line high during the tenth clock pulse to establish a *Stop* condition.

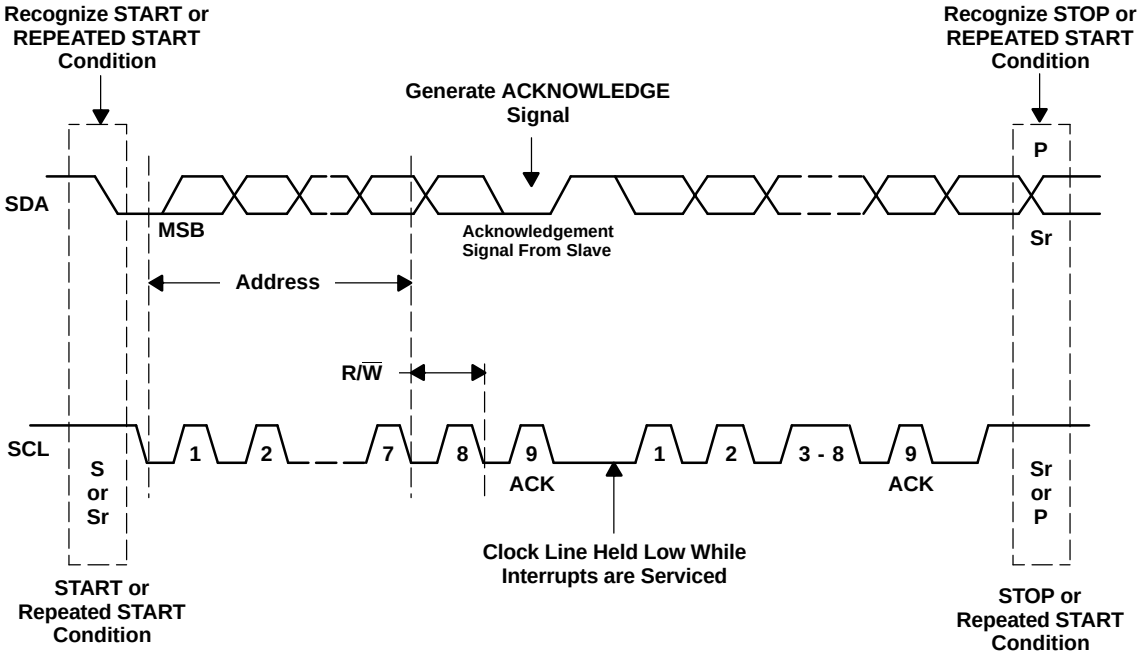
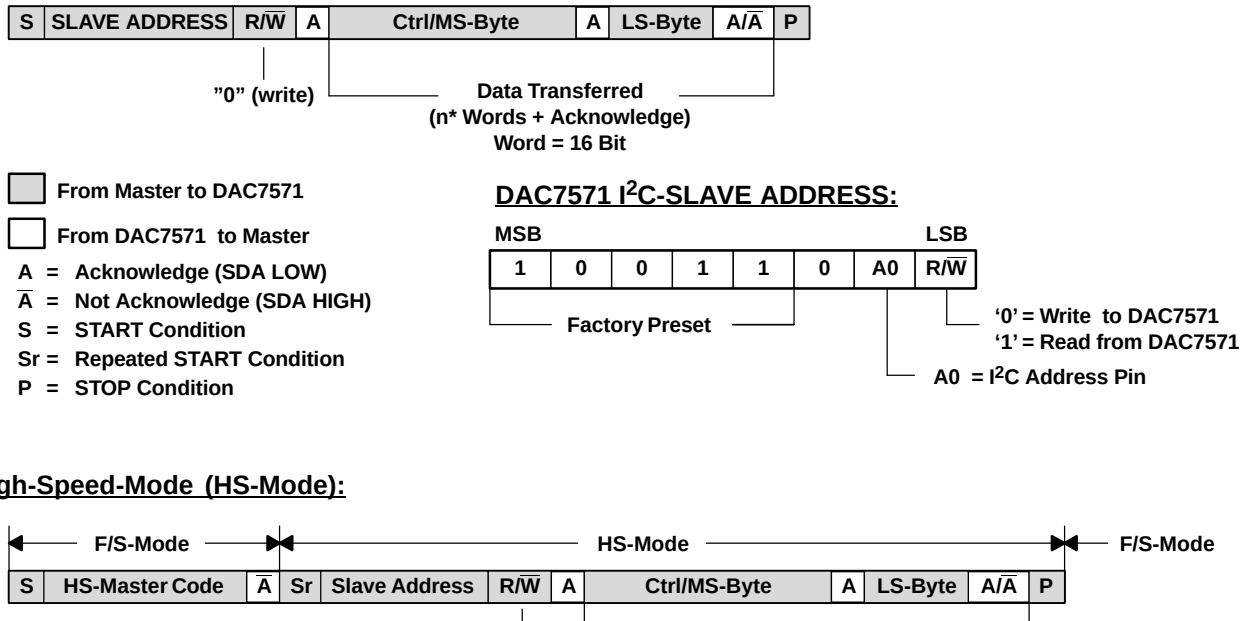


Figure 44. Bus Protocol

THEORY OF OPERATION (continued)

Standard-and Fast-Mode:



High-Speed-Mode (HS-Mode):

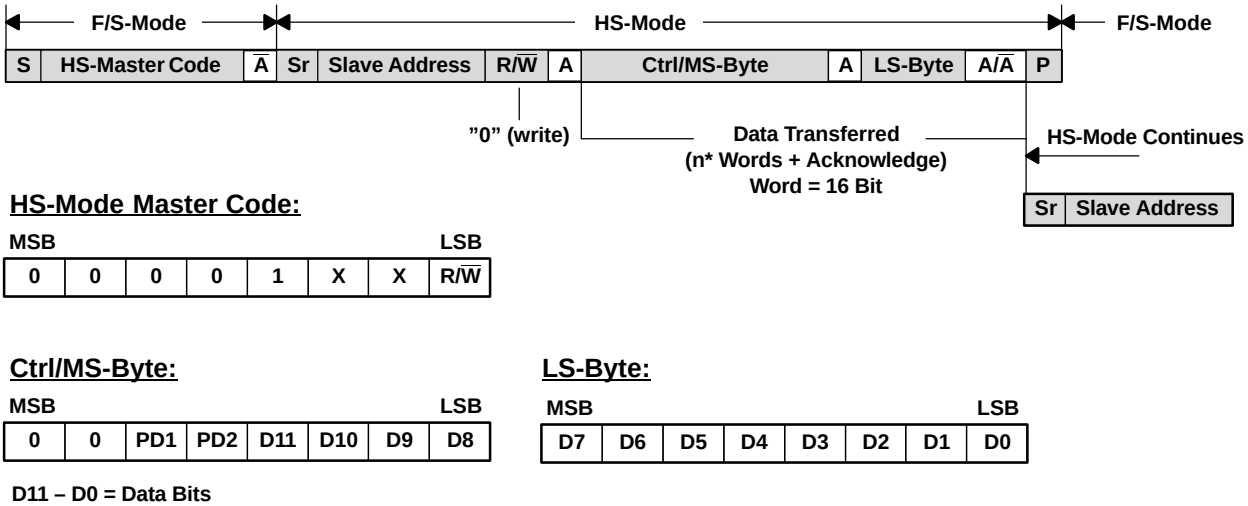


Figure 45. Master Transmitter Addressing DAC7571 as a Slave Receiver With a 7-Bit Address

ADDRESS BYTE

MSB							R/W
1	0	0	1	1	0	A0	0

The address byte is the first byte received by the DAC7571 following the START condition from the master device. The first five bits (MSBs) of the slave address are factory preset to 100110. The next bit of the address byte is the device select bit, A0. In order for DAC7571 to respond, the logic state of address bit A0 should match the logic state of address pin A0. A maximum of two devices with the same preset code can therefore be connected on the same bus at one time. The A0 Address Input can be connected to V_{DD} or digital ground, or can be actively driven by TTL or CMOS logic levels. The device address is set by the state of the A0 pin upon power-up of the DAC7571. The last bit of the address byte (R/$\overline{W}$) should always be zero. Following the START condition, the DAC7571 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 100110 code, the appropriate device select bit and the R/$\overline{W}$ bit, the DAC7571 outputs an acknowledge signal on the SDA line. Upon receipt of a broadcast address 10010000, the DAC7571 responds regardless of the state of the A0 pin.

MASTER TRANSMITTER WRITING TO A SLAVE RECEIVER (DAC7571) IN STANDARD/FAST MODES

I^2C protocol starts when the bus is dile, that is, when SDA and SCL lines are stable high. The master then pulls the SDA line low while SCL is still high indicting that serial data transfer has started. This is called a *start condition*, and can only be asserted by the master. After the start conditioin, the master generates the serial clock and puts out an address byte. While generating the bit stream, the master ensures the timing for valid data. For each valid I^2C bit, the SDA line should remain stable during the entire high period of the SCL line. The address byte consists of 7 address bits (1001 100, assuming A0=0) and a direction bit (R/$\overline{W}$=0). After sending the address byte, the master generates a ninth SCL pulse and monitors the state of the SDA line during the high period of this ninth clock cycle.

The SDA line being pulled low by a receiver during the high period of this 9^{th} clock cylce is called an *acknowledge* signal. If the master receives an acknowledge signal, it knows that a DAC7571 successfully matched the address which the master sent. Upon the receipt of this acknowledge, the master knows that the communication link with a DAC7571 has been established and more data can be sent. The master continues by sending a Control/MS-byte, which sets DAC7571 operation mode and specifies the first 4 MSBs of data. After sending the Control/MS-byte, the master expects an acknowledge signal from the DAC7571. Upon the receipt of the acknowledge, the master sends an LS-byte that represents the 8 least significant bits of DAC7571's 12-bit conversion data. After receiving the LS-byte, the DAC7571 sends an acknowledge. At the falling edge of the acknowledge signal, following the LS-byte, the DAC7571 performs a digital to analog conversion. For further DAC updates, the master can keep repeating Control/MS-byte and LS-byte sequences expecting an acknowledge after each byte. After the required number of digital to analog conversions is complete, the master can break the communication link with the DAC7571 by pulling the SDA line from low to high while SCL line is high. This is called a *stop condition* . A stop condition brings the bus back to idle (SDA and SCL both high). A stop condition indicates that communication with the DAC7571 has ended. All devices on the bus, including the DAC7571, waits for a new start condition followed by a mtaching address byte. DAC7571 stays in a programmed state until the receipt of a stop condition.

Table 1. Write Sequence in Standard/Fast Modes

Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master	Start								Begin Sequence(1)
Master	1	0	0	1	1	0	A0	0	Write Addressing (LSB=0, R/$\overline{W}$ = 0)
DAC7571	DAC7571 Acknowledges								
Master	0	0	PD1	PD0	D11	D10	D9	D8	Writing Control/MS-Byte
DAC7571	DAC7571 Acknowledges								
Master	D7	D6	D5	D4	D3	D2	D1	D0	Writing LS-Byte
DAC7571	DAC7571 Acknowledges								
Master	Stop or Repeated Start(2)								Done

(1) Once DAC7571 is addressed, high-byte-low-byte sequences can repeat until a stop condition is received.
(2) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

POWER-ON RESET

The DAC7571 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0 V. It remains at a zero-code output until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the DAC output while it is in the process of powering up.

POWER-DOWN MODES

The DAC7571 contains four separate modes of operation. These modes are programmable via two bits (PD1 and PD0). Table 2 shows how the state of these bits correspond to the mode of operation.

Table 2. Modes of Operation for the DAC7571

PD1	PD0	OPERATING MODE
0	0	Normal Operation
0	1	1kΩ to AGND, PWD
1	0	100kΩ to AGND, PWD
1	1	High Impedance, PWD

When both bits are set to 0, the device works normally with normal power consumption of 150 µA at 5V. However, for the three power-down modes, the supply current falls to 200 nA at 5V (50 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while in power-down mode. There are three different options: The output is connected internally to AGND through a 1 kΩ resistor, a 100 kΩ resistor, or it is left open-circuited (high impedance). The output stage is illustrated in Figure 46.

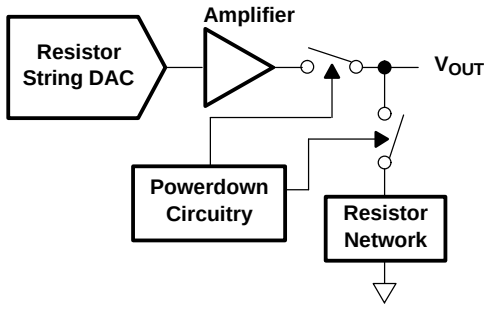


Figure 46. Output Stage During Power-Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time required to exit power down is typically 2.5 µs for AV_{DD} = 5 V and 5 µs for AV_{DD} = 3V. See the Typical Characteristics for more information.

CURRENT CONSUMPTION

The DAC7571 typically consumes 150 µA at V_{DD} = 5 V and 120 µA at V_{DD} = 3 V. Additional current consumption can occur due to the digital inputs if V_{IH} << V_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC. In power-down mode, typical current consumption is 200 nA. Ten to 20 ms after a power-down command is issued, the power-down current typically drops below 10 mA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC7571 output stage is capable of driving loads of up to 1000 pF while remaining stable. Within the offset and gain error margins, the DAC7571 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2 kΩ can be driven by the DAC7571 while achieving a typical load regulation of 1%. As the load resistance drops below 2 kΩ, the load regulation error increases. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This may occur within approximately the top 20 mV of the DAC's digital input-to-voltage output transfer characteristic.

OUTPUT VOLTAGE STABILITY

The DAC7571 exhibits excellent temperature stability of 5 ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage to stay within a ±25 µV window for a ±1°C ambient temperature change. Good power-supply rejection ratio (PSRR) performance reduces supply noise present on V_{DD} from appearing at the outputs to well below 10 µV-s. Combined with good dc noise performance and true 12-bit differential linearity, the DAC7571 becomes a perfect choice for closed-loop control applications.

APPLICATIONS

USING REF02 AS A POWER SUPPLY FOR THE DAC7571

Due to the extremely low supply current required by the DAC7571, a possible configuration is to use a REF02 +5V precision voltage reference to supply the required voltage to the DAC7571's supply input as well as the reference input, as shown in Figure 47. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC7571. If the REF02 is used, the current it needs to supply to the DAC7571 is 150 µA typical and 200 µA max for V_{DD} = 5V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5 mW load on a given DAC output) is: 135 µA + (5 mW/5 V) = 1.14 mA.

The load regulation of the REF02 is typically (0.005%×V_{DD})/mA, which results in an error of 285 mV for the 1.14 mA current drawn from it. This corresponds to a 0.2 LSB error for a 0 V to 5 V output range.

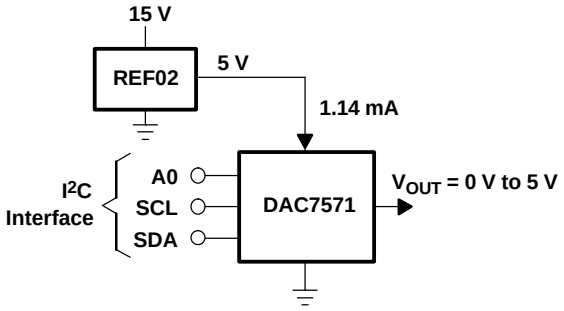


Figure 47. REF02 as Power Supply to DAC7571

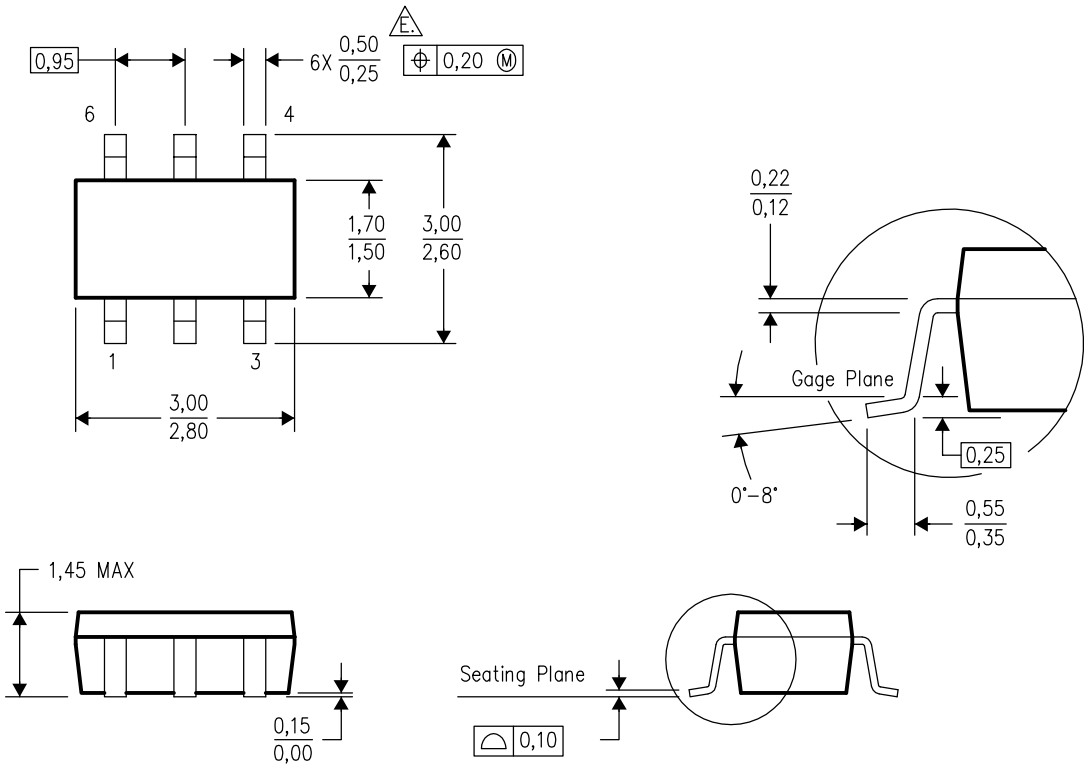
LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1 µF to 10 µF and 0.1 µF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

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