

128Mb F-die SDRAM Specification

Revision 1.2

May 2004

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Revision History

Revision 0.0 (August, 2003)

- First release.

Revision 0.1 (November, 2003)

- completed DC characteristics.

Revision 0.2 (November, 2003)

- Preliminary spec release.

Revision 1.0 (January, 2004)

- Revision 1.0 spec release.
- Modified ICC4 current from 110mA -> 140mA at x16
- Modified tSH from 0.8ns -> 1.0ns at 166MHz.

Revision 1.1 (February, 2004)

- Corrected typo.

Revision 1.2 (May, 2004)

- Added Note 5. sentence of tRDL parameter

SDRAM 128Mb F-die (x4, x8, x16)

CMOS SDRAM

8M x 4Bit x 4 Banks / 4M x 8Bit x 4 Banks / 2M x 16Bit x 4 Banks SDRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - . CAS latency (2 & 3)
 - . Burst length (1, 2, 4, 8 & Full page)
 - . Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM (x4,x8) & L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)

GENERAL DESCRIPTION

The K4S280432F / K4S280832F / K4S281632F is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits / 4 x 4,194,304 words by 8 bits / 4 x 2,097,152 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

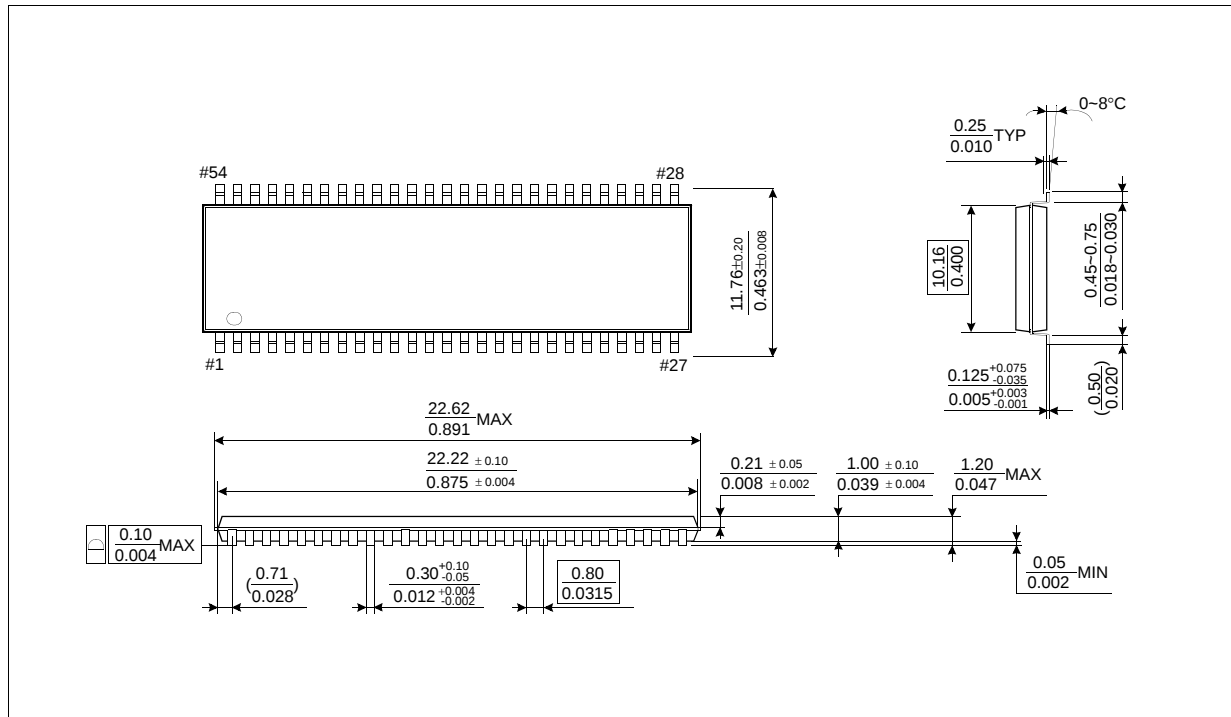
Ordering Information

Part No.	Organization	Max Freq.	Interface	Package
K4S280432F-TC(L)75	32M x 4	133MHz (CL=3)	LVTTTL	54pin TSOP(II)
K4S280832F-TC(L)75	16M x 8	133MHz (CL=3)		
K4S281632F-TC(L)60/75	8M x 16	166MHz (CL=3)		

Organization	Row Address	Column Address
32Mx4	A0~A11	A0-A9, A11
16Mx8	A0~A11	A0-A9
8Mx16	A0~A11	A0-A8

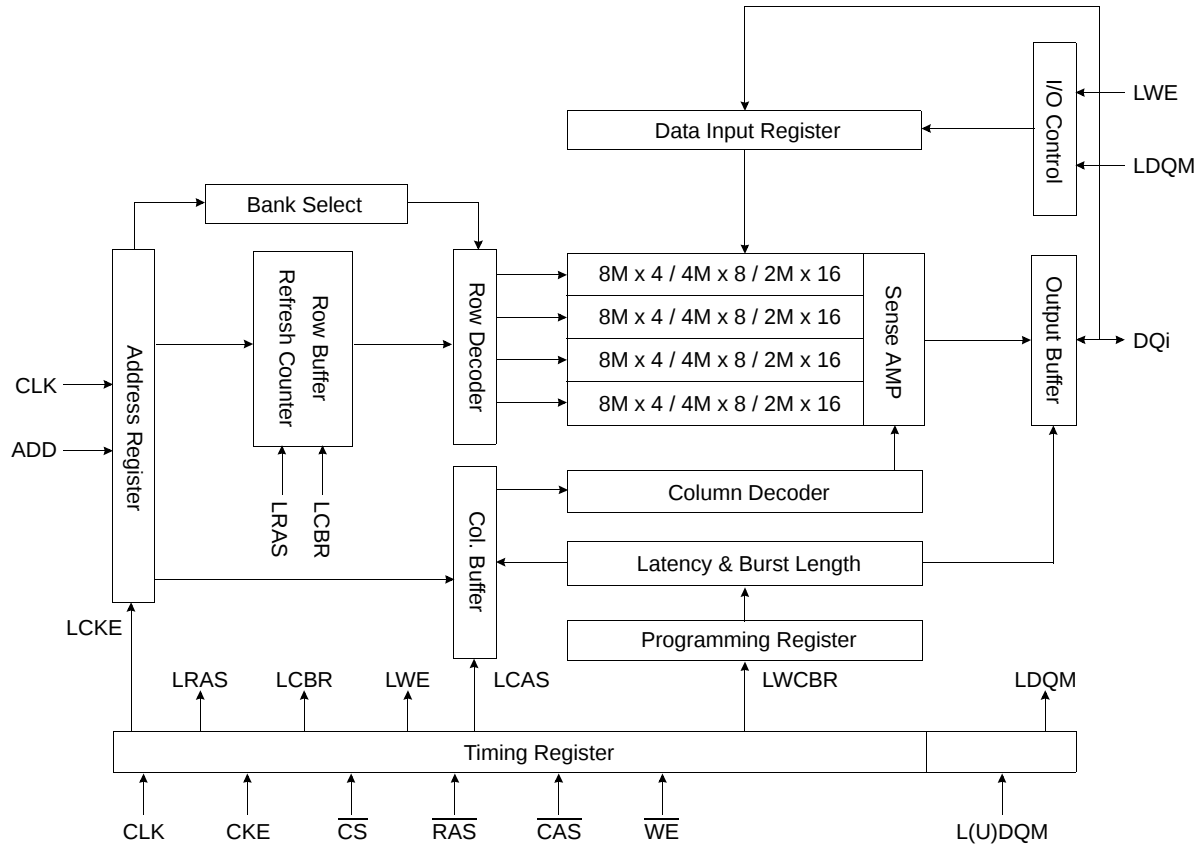
Row & Column address configuration

Package Physical Dimension



54Pin TSOP(II) Package Dimension

FUNCTIONAL BLOCK DIAGRAM



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SDRAM 128Mb F-die (x4, x8, x16)

CMOS SDRAM

PIN CONFIGURATION (Top view)

x16	x8	x4			x4	x8	x16
VDD	VDD	VDD	1	54	VSS	VSS	VSS
DQ0	DQ0	N.C	2	53	N.C	DQ7	DQ15
VDDQ	VDDQ	VDDQ	3	52	VSSQ	VSSQ	VSSQ
DQ1	N.C	N.C	4	51	N.C	N.C	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6	49	VDDQ	VDDQ	VDDQ
DQ3	N.C	N.C	7	48	N.C	N.C	DQ12
DQ4	DQ2	N.C	8	47	N.C	DQ5	DQ11
VDDQ	VDDQ	VDDQ	9	46	VSSQ	VSSQ	VSSQ
DQ5	N.C	N.C	10	45	N.C	N.C	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12	43	VDDQ	VDDQ	VDDQ
DQ7	N.C	N.C	13	42	N.C	N.C	DQ8
VDD	VDD	VDD	14	41	VSS	VSS	VSS
LDQM	N.C	N.C	15	40	N.C/RFU	N.C/RFU	N.C/RFU
WE	WE	WE	16	39	DQM	DQM	UDQM
CAS	CAS	CAS	17	38	CLK	CLK	CLK
RAS	RAS	RAS	18	37	CKE	CKE	CKE
CS	CS	CS	19	36	N.C	N.C	N.C
BA0	BA0	BA0	20	35	A11	A11	A11
BA1	BA1	BA1	21	34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
VDD	VDD	VDD	27	28	VSS	VSS	VSS

54Pin TSOP
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : (x4 : CA0 ~ CA9,CA11), (x8 : CA0 ~ CA9), (x16 : CA0 ~ CA8)
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
DQM	Data input/output mask	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ N	Data input/output	Data inputs/outputs are multiplexed on the same pins. (x4 : DQ0 ~ 3), (x8 : DQ0 ~ 7), (x16 : DQ0 ~ 15)
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{DD} , V _{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V _{IH}	2.0	3.0	V _{DD} +0.3	V	1
Input logic low voltage	V _{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output logic low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current	I _{LI}	-10	-	10	µA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
 2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
 3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
 Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C _{CLK}	2.5	3.5	pF
RAS, CAS, WE, CS, CE, DQM	C _{IN}	2.5	3.8	pF
Address	C _{ADD}	2.5	3.8	pF
(x4 : DQ0 ~ DQ3), (x8 : DQ0 ~ DQ7), (x16 : DQ0 ~ DQ15)	C _{OUT}	4.0	6.0	pF

DC CHARACTERISTICS (x4, x8)(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition		Version	Unit	Note
				75		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA		90	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns		2	mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞		2		
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns		20	mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		10		
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns		5	mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞		5		
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns		30	mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable		25	mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst		110	mA	1
Refresh current	Icc5	trc ≥ trc(min)		200	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	2	mA	3
			L	800	uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

3. K4S2804(08)32F-TC

4. K4S2804(08)32F-TL

5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$)

SDRAM 128Mb F-die (x4, x8, x16)

CMOS SDRAM

DC CHARACTERISTICS (x16)

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			60	75		
Operating current (One bank active)	Icc1	Burst length = 1 trc ≥ trc(min) Io = 0 mA	130	100	mA	1
Precharge standby current in power-down mode	Icc2P	CKE ≤ VIL(max), tcc = 10ns	2		mA	
	Icc2PS	CKE & CLK ≤ VIL(max), tcc = ∞	2			
Precharge standby current in non power-down mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	20		mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	10			
Active standby current in power-down mode	Icc3P	CKE ≤ VIL(max), tcc = 10ns	5		mA	
	Icc3PS	CKE & CLK ≤ VIL(max), tcc = ∞	5			
Active standby current in non power-down mode (One bank active)	Icc3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	30		mA	
	Icc3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	25		mA	
Operating current (Burst mode)	Icc4	Io = 0 mA Page burst	150	140	mA	1
Refresh current	Icc5	trc ≥ trc(min)	220	200	mA	2
Self refresh current	Icc6	CKE ≤ 0.2V	C	2	mA	3
			L	800	uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

3. K4S281632F-TC

4. K4S281632F-TL

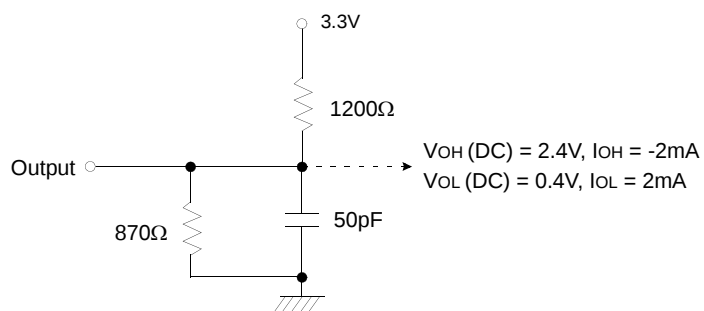
5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$)

SDRAM 128Mb F-die (x4, x8, x16)

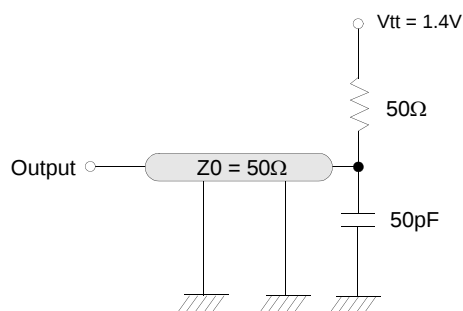
CMOS SDRAM

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

Parameter	Value	Unit
Input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version		Unit	Note
		60 (x16 only)	75		
Row active to row active delay	$t_{RRD}(\min)$	12	15	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	18	20	ns	1
Row precharge time	$t_{RP}(\min)$	18	20	ns	1
Row active time	$t_{RAS}(\min)$	42	45	ns	1
	$t_{RAS}(\max)$	100		us	
Row cycle time	$t_{RC}(\min)$	60	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2		CLK	2,5
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + t_{RP}		-	5
Last data in to new col. address delay	$t_{CDL}(\min)$	1		CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1		CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1		CLK	3
Number of valid output data	CAS latency=3	2		ea	4
	CAS latency=2	-	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. In 100MHz and below 100MHz operating conditions, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK + 20ns$ is also supported. SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + t_{RP}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	60 (x16 only)		75		Unit	Note
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tcc	6	1000	7.5	1000	ns	1
	CAS latency=2		-		10			
CLK to valid output delay	CAS latency=3	tsac		5		5.4	ns	1,2
	CAS latency=2			-		6		
Output data hold time	CAS latency=3	toH	2.5		3		ns	2
	CAS latency=2		-		3			
CLK high pulse width		tCH	2.5		2.5		ns	3
CLK low pulse width		tCL	2.5		2.5		ns	3
Input setup time		tSS	1.5		1.5		ns	3
Input hold time		tSH	1		0.8		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5		5.4	ns	
	CAS latency=2			-		6		

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)$ ns should be added to the parameter.
 - Assumed input rise and fall time $(tr \ \& \ tf) = 1$ ns.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered,
i.e., $[(tr + tf)/2-1]$ ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

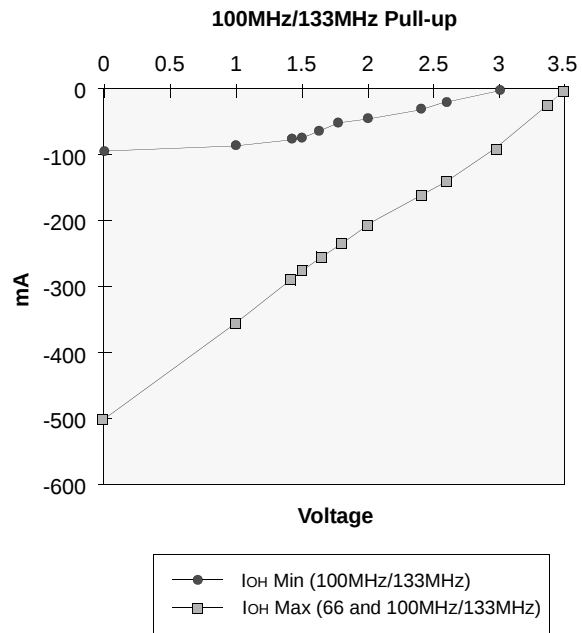
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

- Notes :**
- Rise time specification based on $0pF + 50 \ \Omega$ to V_{SS} , use these values to design to.
 - Fall time specification based on $0pF + 50 \ \Omega$ to V_{DD} , use these values to design to.
 - Measured into 50pF only, use these values to characterize to.
 - All measurements done with respect to V_{SS} .

IBIS SPECIFICATION

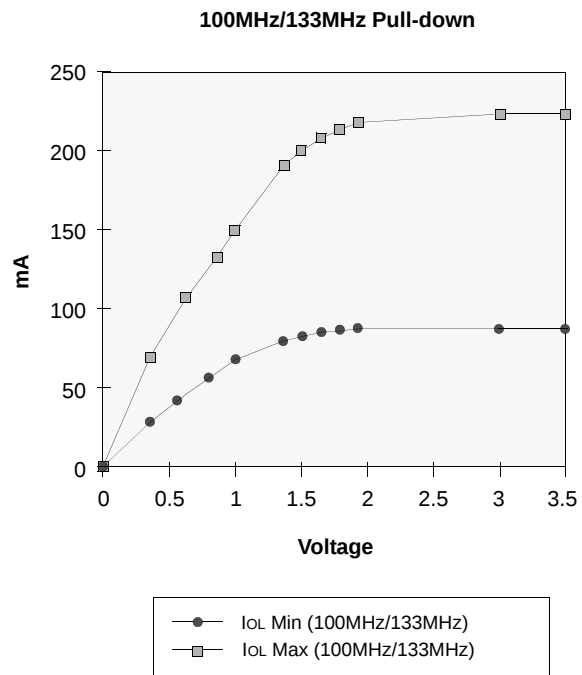
I_{OH} Characteristics (Pull-up)

Voltage	100MHz 133MHz Min	100MHz 133MHz Max
(V)	I (mA)	I (mA)
3.45		-2.4
3.3		-27.3
3.0	0.0	-74.1
2.6	-21.1	-129.2
2.4	-34.1	-153.3
2.0	-58.7	-197.0
1.8	-67.3	-226.2
1.65	-73.0	-248.0
1.5	-77.9	-269.7
1.4	-80.8	-284.3
1.0	-88.6	-344.5
0.0	-93.0	-502.4



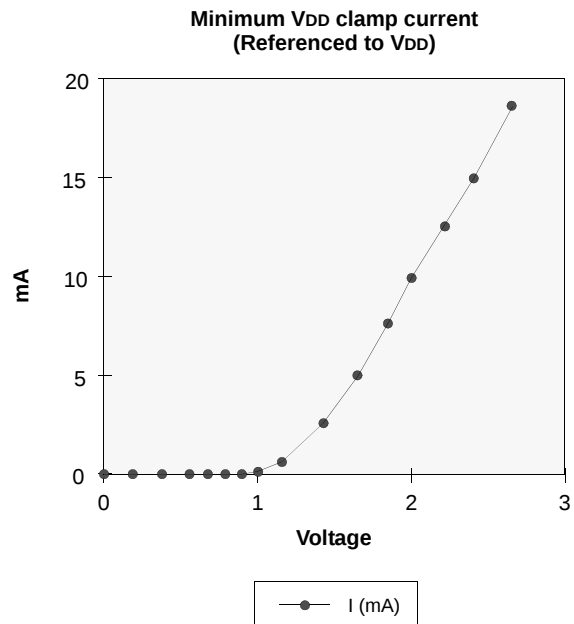
I_{OL} Characteristics (Pull-down)

Voltage	100MHz 133MHz Min	100MHz 133MHz Max
(V)	I (mA)	I (mA)
0.0	0.0	0.0
0.4	27.5	70.2
0.65	41.8	107.5
0.85	51.6	133.8
1.0	58.0	151.2
1.4	70.7	187.7
1.5	72.9	194.4
1.65	75.4	202.5
1.8	77.0	208.6
1.95	77.6	212.0
3.0	80.3	219.6
3.45	81.4	222.6

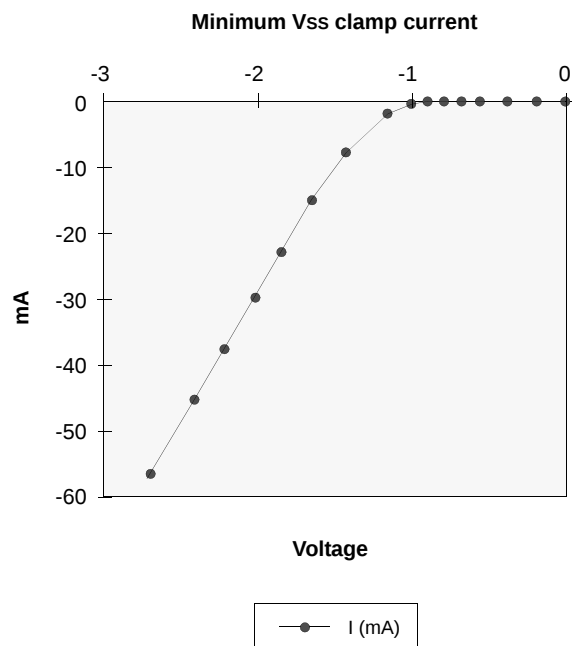


V_{DD} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

V _{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**V_{SS} Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ**

V _{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SDRAM 128Mb F-die (x4, x8, x16)

CMOS SDRAM

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A0 ~ A9, A11,	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	L		3									
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
Exit		L	H	X	X	X	X	X					
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

Notes :

- OP Code : Operand code
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
- MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)