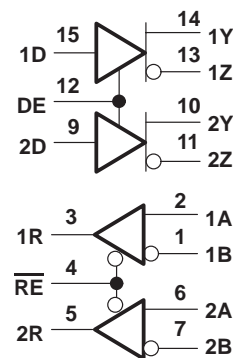
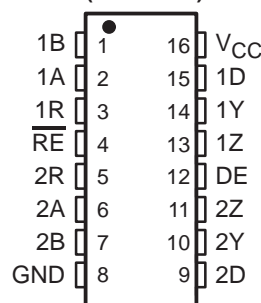


# SN65LVDS1050 HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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- Typically Meets or Exceeds ANSI TIA/EIA-644-1995 Standard
- Operates From a Single 2.4-V to 3.6-V Supply
- Signaling Rates up to 400 Mbit/s
- Bus-Terminal ESD Exceeds 12 kV
- Low-Voltage Differential Signaling With Typical Output Voltages of 285 mV and a 100  $\Omega$  Load
- Propagation Delay Times
  - Driver: 1.7 ns Typ
  - Receiver: 3.7 ns Typ
- Power Dissipation at 200 MHz
  - Driver: 25 mW Typical
  - Receiver: 60 mW Typical
- LVTTTL Input Levels Are 5 V Tolerant
- Driver Is High Impedance When Disabled or With  $V_{CC} < 1.5$  V
- Receiver Has Open-Circuit Fail Safe
- Available in Thin Shrink Outline Packaging With 20-mil Lead Pitch

SN65LVDS1050PW  
(Marked as DL1050 or DLS1050)  
(TOP VIEW)



DRIVER FUNCTION TABLE

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

H = high level, L = low level, Z = high impedance, X = don't care

## description

The SN65LVDS1050 is similar to the SN65LVDS050 except that it is characterized for operation with a lower supply voltage range and packaged in the thin shrink outline package for portable battery-powered applications.

The differential line drivers and receivers use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The drivers provide a minimum differential output voltage magnitude of 247 mV into a 100- $\Omega$  load and receipt of 100-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100- $\Omega$  characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment and other application-specific characteristics.

The SN65LVDS1050 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

RECEIVER FUNCTION TABLE

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{\text{RE}}$	R
$V_{ID} \geq 100$ mV	L	H
$-100$ mV $< V_{ID} < 100$ mV	L	?
$V_{ID} \leq -100$ mV	L	L
Open	L	H
X	H	Z

H = high level, L = low level, Z = high impedance, X = don't care



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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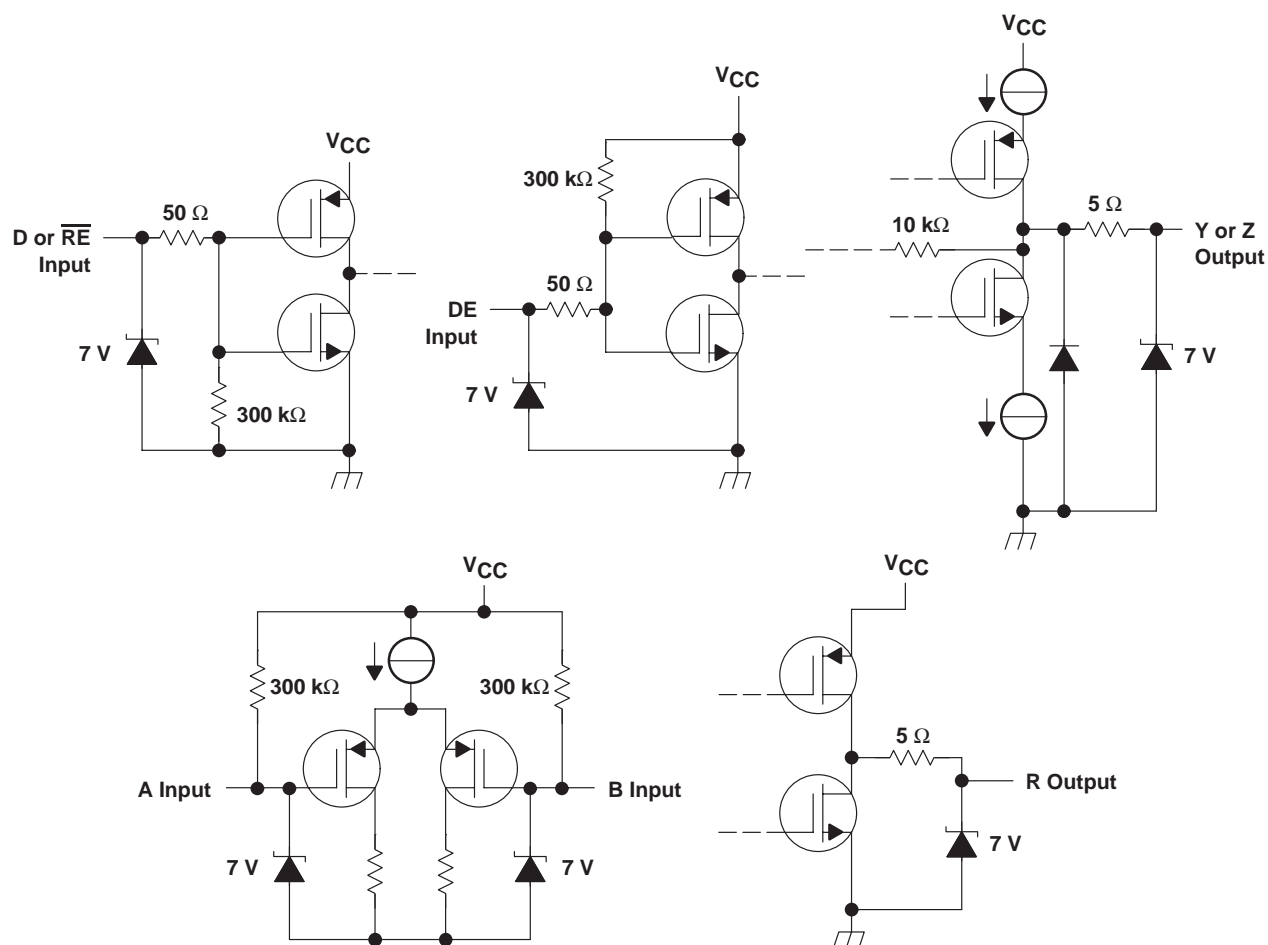
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# SN65LVDS1050

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

SLLS343A – APRIL 1999 – REVISED MARCH 2000

### equivalent input and output schematic diagrams



# SN65LVDS1050

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 4 V
Voltage range (D, R, DE, $\overline{RE}$ )	–0.5 V to 6 V
Voltage range (Y, Z, A, and B)	–0.5 V to 4 V
Electrostatic discharge: Y, Z, A, B, and GND (see Note 2)	Class 3, A:12 kV, B:600 V
All terminals	Class 3, A:7 kV, B:500 V
Continuous power dissipation	See Dissipation Rating Table
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	250°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages are with respect to network ground terminal.  
 2. Tested in accordance with MIL-STD-883C Method 3015.7.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
PW	774 mW	6.2 mW/°C	402 mW

### recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	2.4	2.7	3.6	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
Magnitude of differential input voltage, $ V_{ID} $	0.1		0.6	V
Common-mode input voltage, $V_{IC}$ (see Figure 8)	0	2.4	$-\frac{ V_{ID} }{2}$	V
			$V_{CC}-0.8$	
Operating free-air temperature, $T_A$	–40		85	°C

NOTE 3: The common-mode input voltage,  $V_{IC}$ , is not fully 644 compliant when  $V_{CC} = 2.4$  V.



# SN65LVDS1050

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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**device electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$I_{CC}$ Supply current	Driver and receiver enabled, No receiver load, Driver $R_L = 100\ \Omega$		12	20	mA
	Driver enabled, Receiver disabled, $R_L = 100\ \Omega$		10	16	
	Driver disabled, Receiver enabled, No load		3	6	
	Disabled		0.5	1	

† All typical values are at 25°C and with a 2.7-V supply.

**driver electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $ Differential output voltage magnitude	$R_L = 100\ \Omega$ , See Figure 1 and Figure 2	247	285	454	mV
$\Delta V_{OD} $ Change in differential output voltage magnitude between logic states		-50		50	
$V_{OC(SS)}$ Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$ Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$ Peak-to-peak common-mode output voltage			50	150	mV
$I_{IH}$ High-level input current	DE	$V_{IH} = 5\ V$	-0.5	-20	$\mu A$
	D		2	20	
$I_{IL}$ Low-level input current	DE	$V_{IL} = 0.8\ V$	-0.5	-10	$\mu A$
	D		2	20	
$I_{OS}$ Short-circuit output current	$V_{OY}$ or $V_{OZ} = 0\ V$		3	10	mA
	$V_{OD} = 0\ V$		3	10	
$I_{OZ}$ High-impedance output current	$V_{OD} = 600\ mV$			$\pm 1$	$\mu A$
	$V_O = 0\ V$ or $V_{CC}$			$\pm 1$	
$I_{O(OFF)}$ Power-off output current	$V_{CC} = 0\ V$ , $V_O = 3.6\ V$			$\pm 1$	$\mu A$
$C_{IN}$ Input capacitance			3		pF

**receiver electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{ITH+}$ Positive-going differential input voltage threshold	See Figure 5			100	mV
$V_{ITH-}$ Negative-going differential input voltage threshold		-100			
$V_{OH}$ High-level output voltage	$I_{OH} = -8\ mA$	2			V
$V_{OL}$ Low-level output voltage	$I_{OL} = 8\ mA$			0.4	V
$I_I$ Input current (A or B inputs)	$V_I = 0$	-2		-20	$\mu A$
	$V_I = 2.4\ V$	-1.2			
$I_{I(OFF)}$ Power-off input current (A or B inputs)	$V_{CC} = 0$			$\pm 20$	$\mu A$
$I_{IH}$ High-level input current (enables)	$V_{IH} = 5\ V$			$\pm 10$	$\mu A$
$I_{IL}$ Low-level input current (enables)	$V_{IL} = 0.8\ V$			$\pm 10$	$\mu A$
$I_{OZ}$ High-impedance output current	$V_O = 0$ or $5\ V$			$\pm 10$	$\mu A$

† All typical values are at 25°C and with a 2.7-V supply.



**driver switching characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 10 pF, See Figure 2		1.7	2.7	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			1.7	3	ns
t <sub>r</sub> Differential output signal rise time			0.8	1	ns
t <sub>f</sub> Differential output signal fall time			0.8	1	ns
t <sub>sk(p)</sub> Pulse skew ( t <sub>pHL</sub> – t <sub>pLH</sub>  )			300		ps
t <sub>sk(o)</sub> Channel-to-channel output skew‡			150		ps
t <sub>PZH</sub> Propagation delay time, high-impedance-to-high-level output	See Figure 4		7.8	10	ns
t <sub>PZL</sub> Propagation delay time, high-impedance-to-low-level output			7.3	10	ns
t <sub>PHZ</sub> Propagation delay time, high-level-to-high-impedance output			5.2	10	ns
t <sub>PLZ</sub> Propagation delay time, low-level-to-high-impedance output			6.6	10	ns

† All typical values are at 25°C and with a 2.7-V supply.

‡ t<sub>sk(o)</sub> is the maximum delay time difference between drivers on the same device.

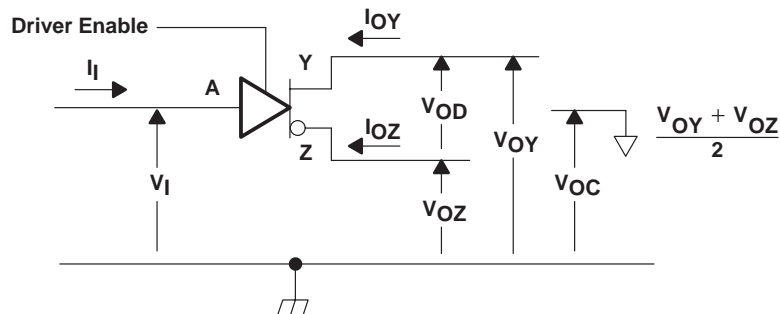
**receiver switching characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	C <sub>L</sub> = 10 pF, See Figure 6		3.7	5.2	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			3.7	4.5	ns
t <sub>sk(p)</sub> Pulse skew ( t <sub>pHL</sub> – t <sub>pLH</sub>  )			0.3		ns
t <sub>r</sub> Output signal rise time			0.8	1.5	ns
t <sub>f</sub> Output signal fall time			0.8	1.5	ns
t <sub>PZH</sub> Propagation delay time, high-level-to-high-impedance output	See Figure 7		5.4		ns
t <sub>PZL</sub> Propagation delay time, low-level-to-low-impedance output			6.3		ns
t <sub>PHZ</sub> Propagation delay time, high-impedance-to-high-level output			6.1		ns
t <sub>PLZ</sub> Propagation delay time, low-impedance-to-high-level output			6.9		ns

† All typical values are at 25°C and with a 2.7-V supply.

### PARAMETER MEASUREMENT INFORMATION

**driver**



**Figure 1. Driver Voltage and Current Definitions**

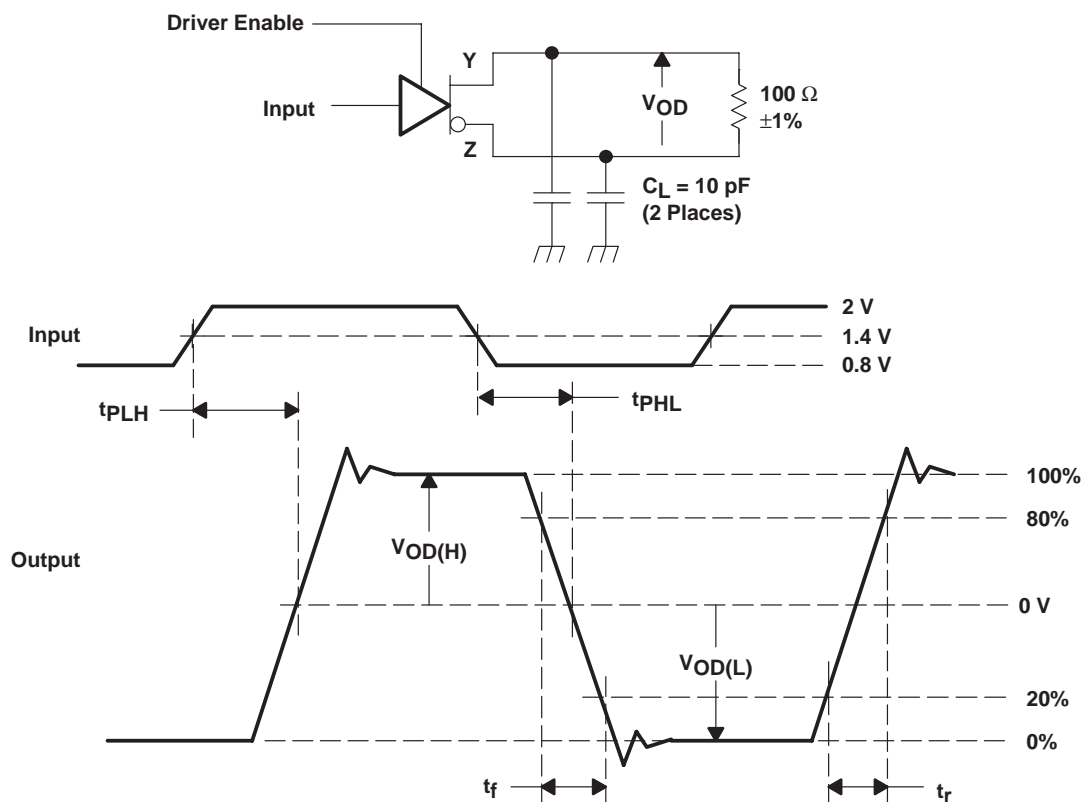
# SN65LVDS1050

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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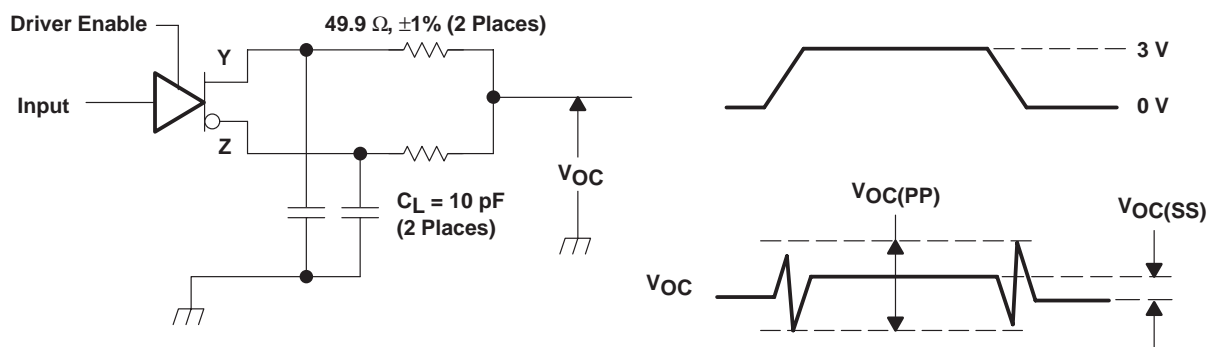
### PARAMETER MEASUREMENT INFORMATION

#### driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

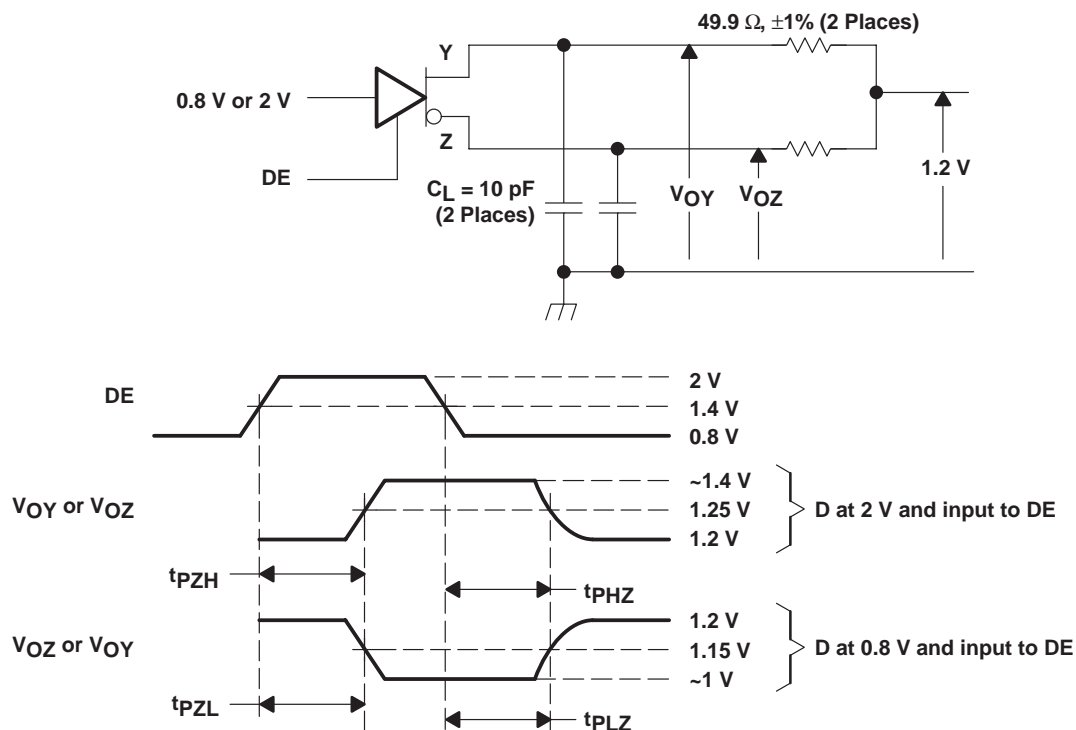


NOTE A: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of  $V_{OC(PP)}$  is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

## PARAMETER MEASUREMENT INFORMATION

driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1 \text{ ns}$ , pulse repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10 \text{ ns}$ .  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

**Figure 4. Enable and Disable Time Circuit and Definitions**

SN65LVDS1050  
HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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PARAMETER MEASUREMENT INFORMATION

receiver

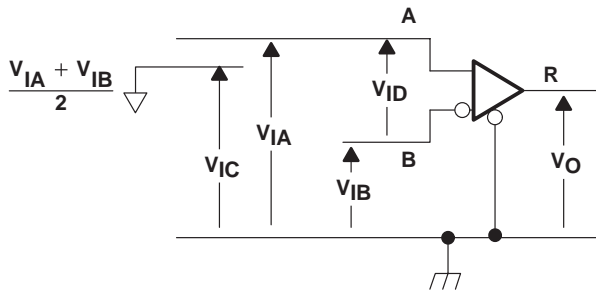


Figure 5. Receiver Voltage Definitions

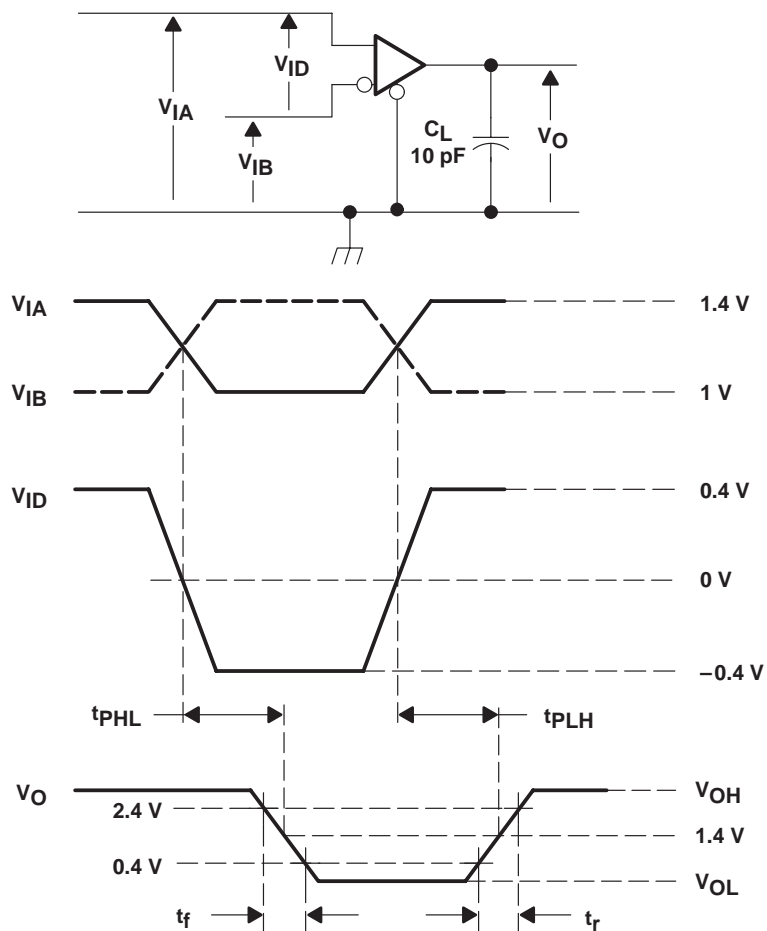
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3



## PARAMETER MEASUREMENT INFORMATION

receiver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1 \text{ ns}$ , pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2 \text{ ns}$ .  $C_L$  includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

**Figure 6. Timing Test Circuit and Waveforms**

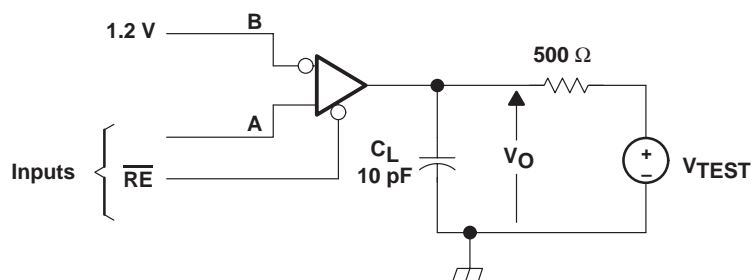
# SN65LVDS1050

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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### PARAMETER MEASUREMENT INFORMATION

receiver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width =  $500 \pm 10$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

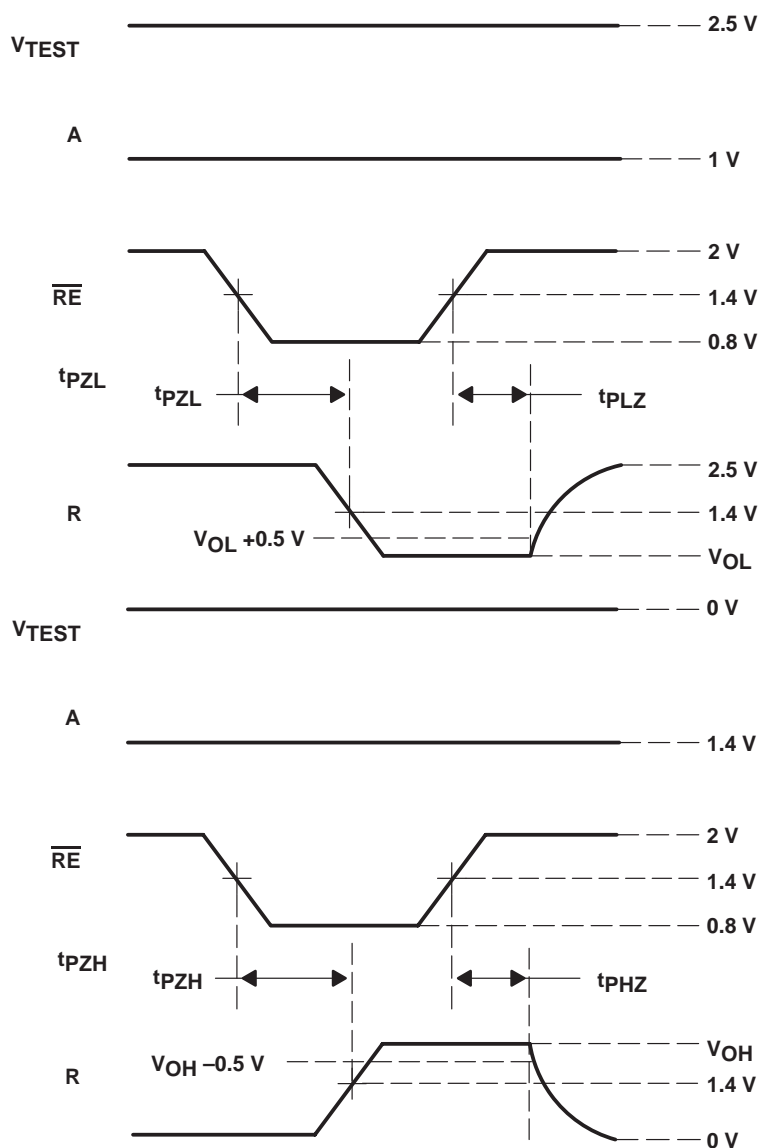


Figure 7. Enable/Disable Time Test Circuit and Waveforms

### TYPICAL CHARACTERISTICS

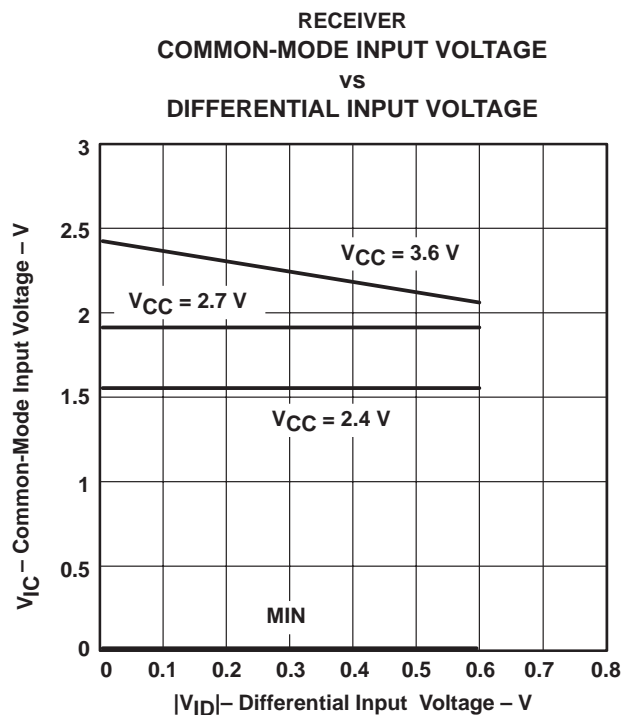


Figure 8

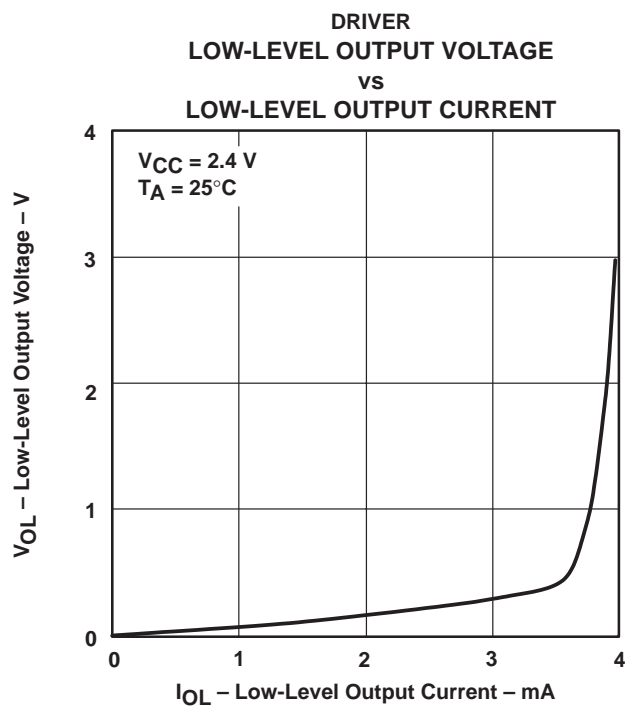


Figure 9

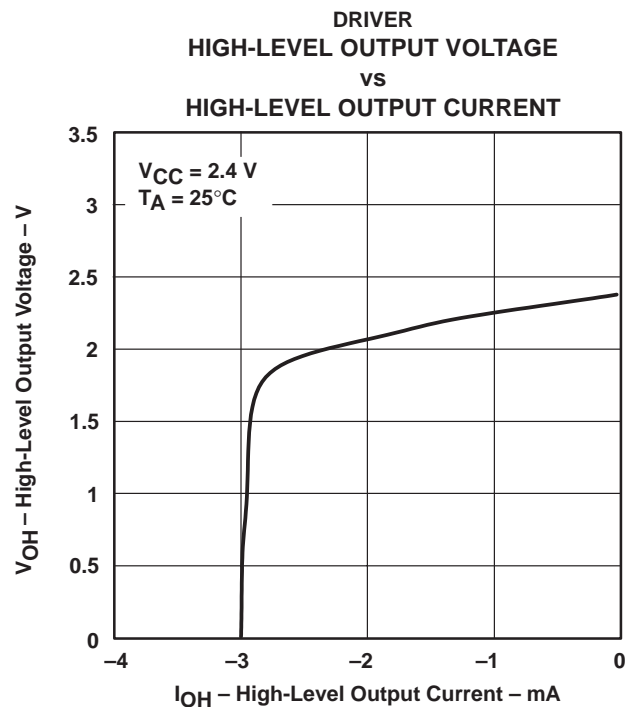


Figure 10

# SN65LVDS1050

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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### TYPICAL CHARACTERISTICS

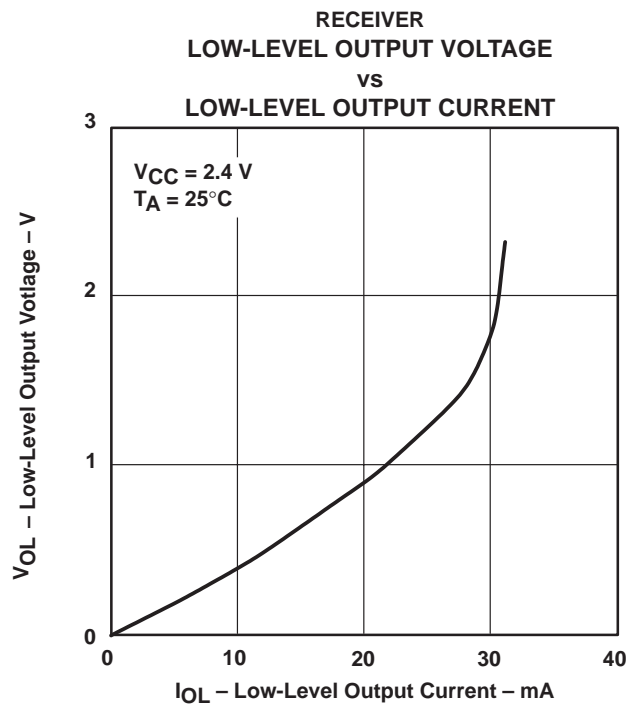


Figure 11

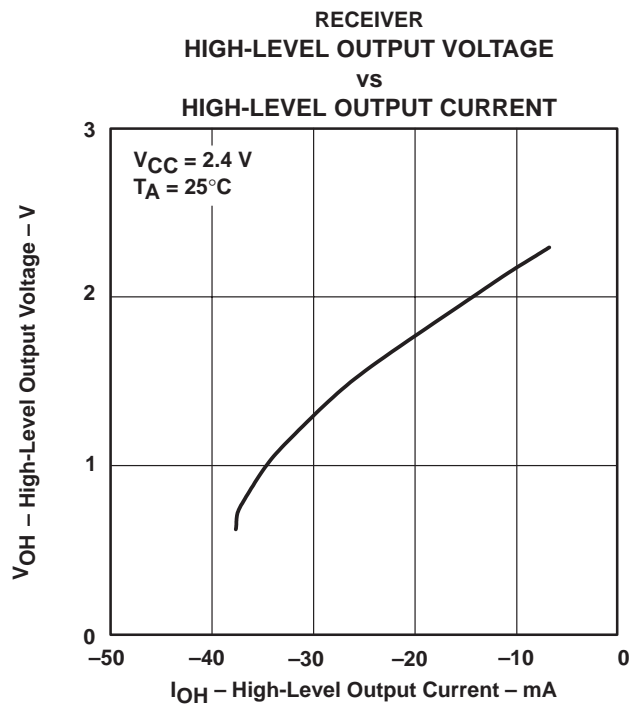


Figure 12

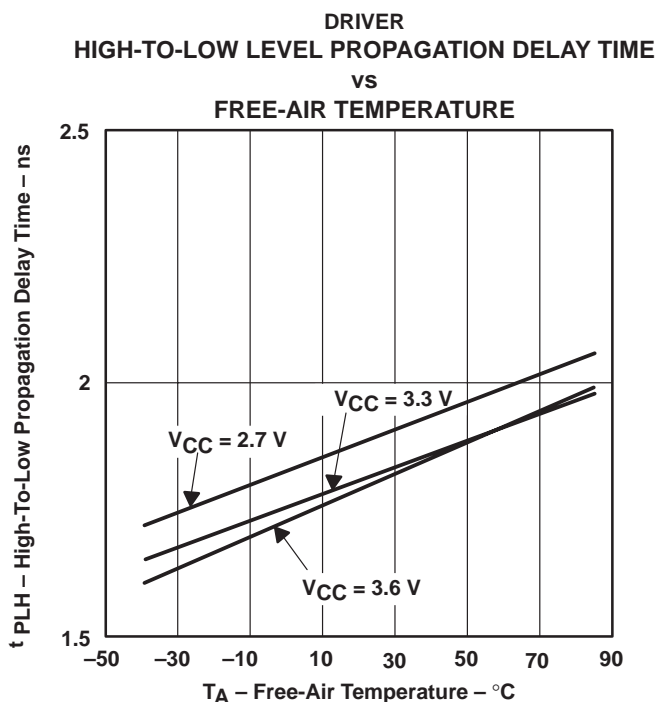


Figure 13

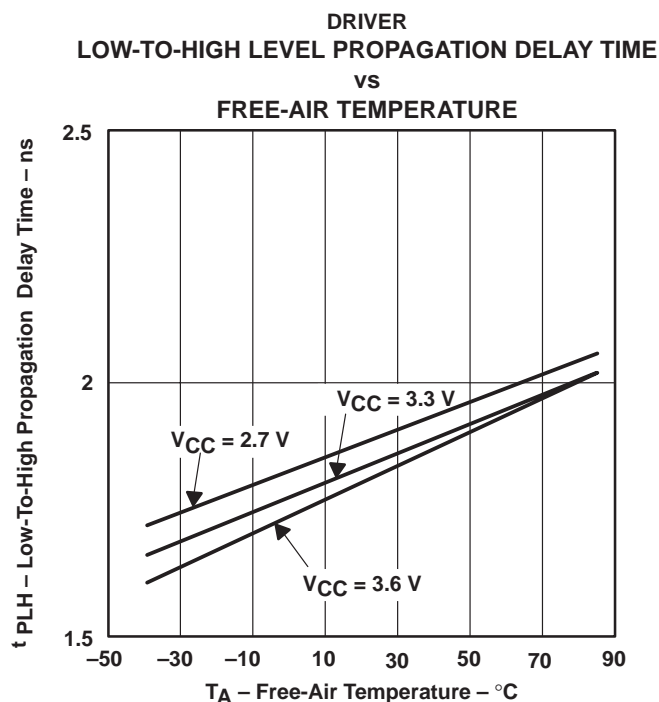


Figure 14

## TYPICAL CHARACTERISTICS

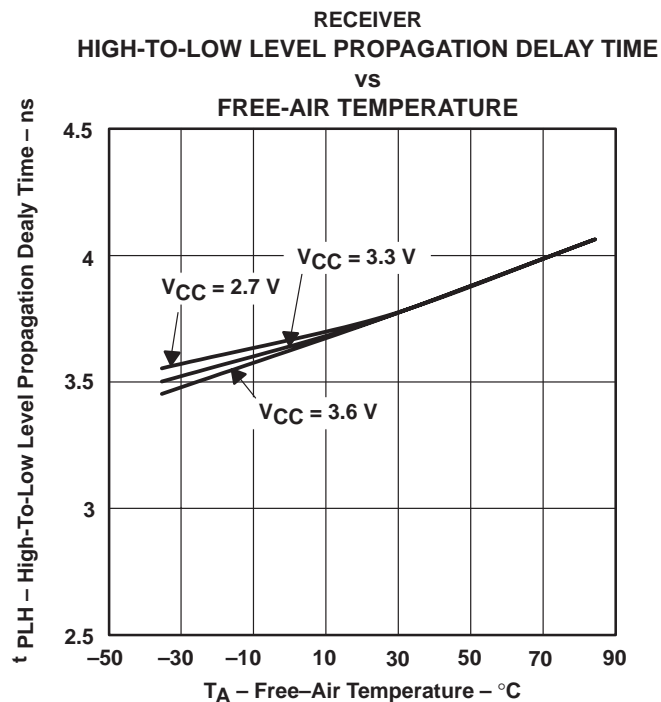


Figure 15

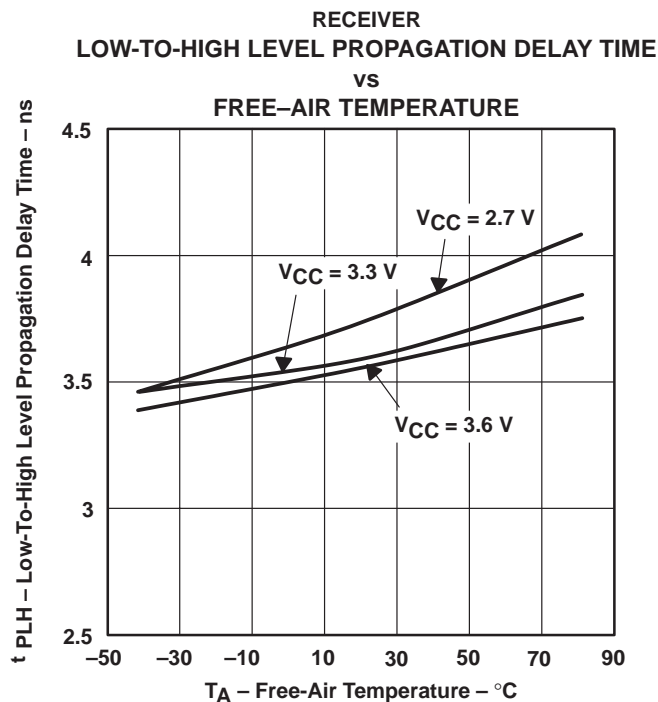


Figure 16

# SN65LVDS1050

## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

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### APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/Receivers maintain ECL speeds without the power and dual supply requirements.

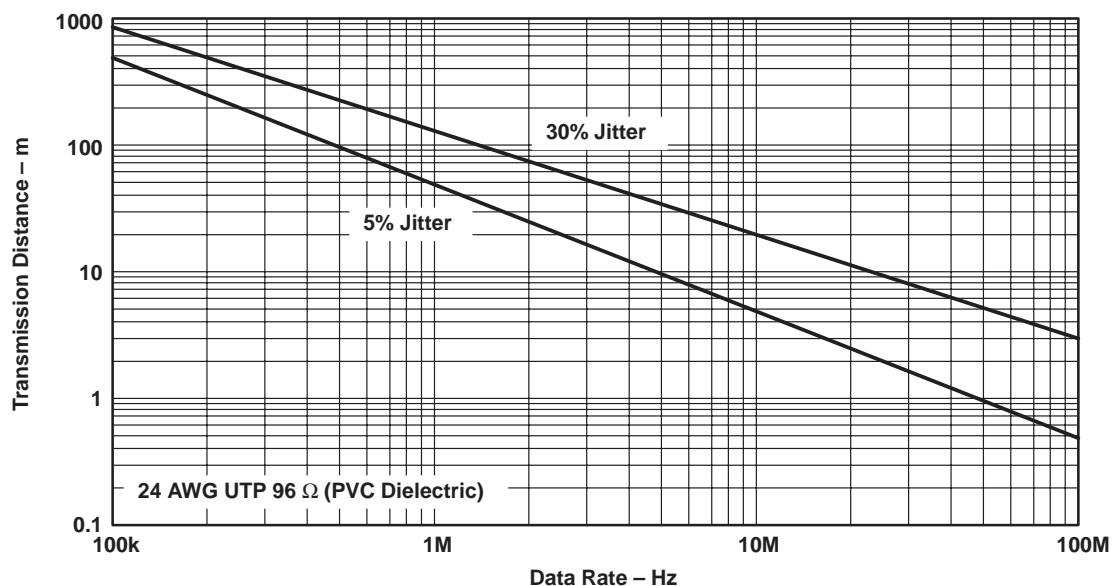


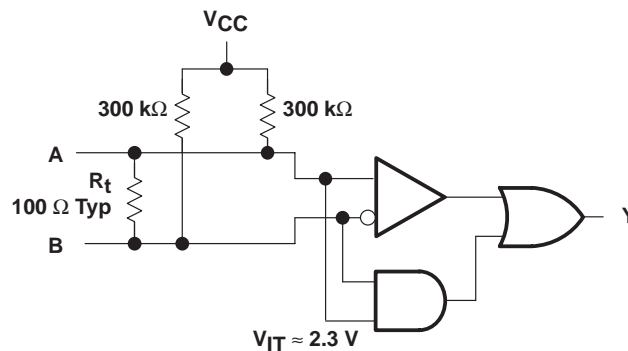
Figure 17. Data Transmission Distance Versus Rate

## APPLICATION INFORMATION

### fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between  $-100\text{ mV}$  and  $100\text{ mV}$  and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near  $V_{CC}$  through  $300\text{-k}\Omega$  resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about  $2.3\text{ V}$  to detect this condition and force the output to a high-level, regardless of the differential input voltage.



**Figure 18. Open-Circuit Fail Safe of the LVDS Receiver**

It is only under these conditions that the output of the receiver will be valid with less than a  $100\text{-mV}$  differential input voltage magnitude. The presence of the termination resistor,  $R_t$ , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

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## HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

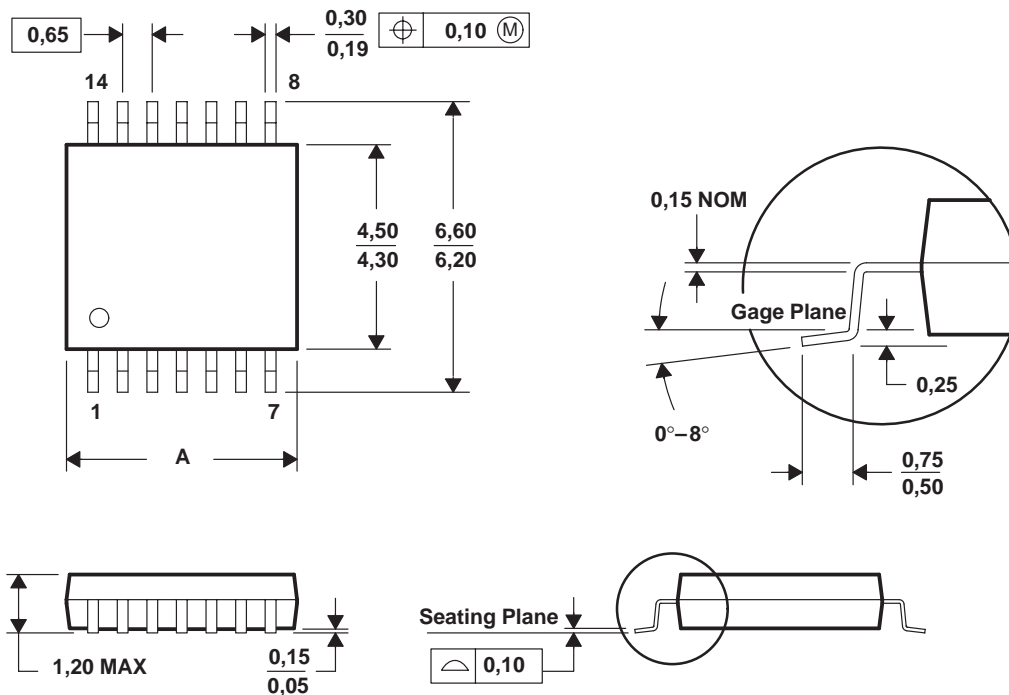
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### MECHANICAL DATA

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-153



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