

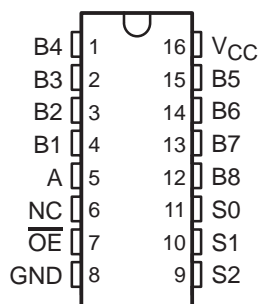
SN74CBTLV3251

LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

SCDS054I – MARCH 1998 – REVISED OCTOBER 2003

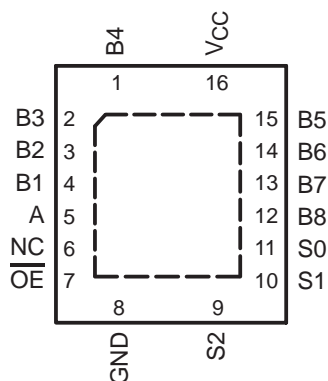
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

RGY PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The SN74CBTLV3251 device is a 1-of-8 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select inputs (S0, S1, S2) control the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable (\overline{OE}) input is high.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Tape and reel | SN74CBTLV3251RGYR | CL251 |
| | SOIC – D | Tube | SN74CBTLV3251D | CBTLV3251 |
| | | Tape and reel | SN74CBTLV3251DR | |
| | SSOP (QSOP) – DBQ | Tape and reel | SN74CBTLV3251DBQR | CL251 |
| | TSSOP – PW | Tape and reel | SN74CBTLV3251PWR | CL251 |
| | TVSOP – DGV | Tape and reel | SN74CBTLV3251DGV | CL251 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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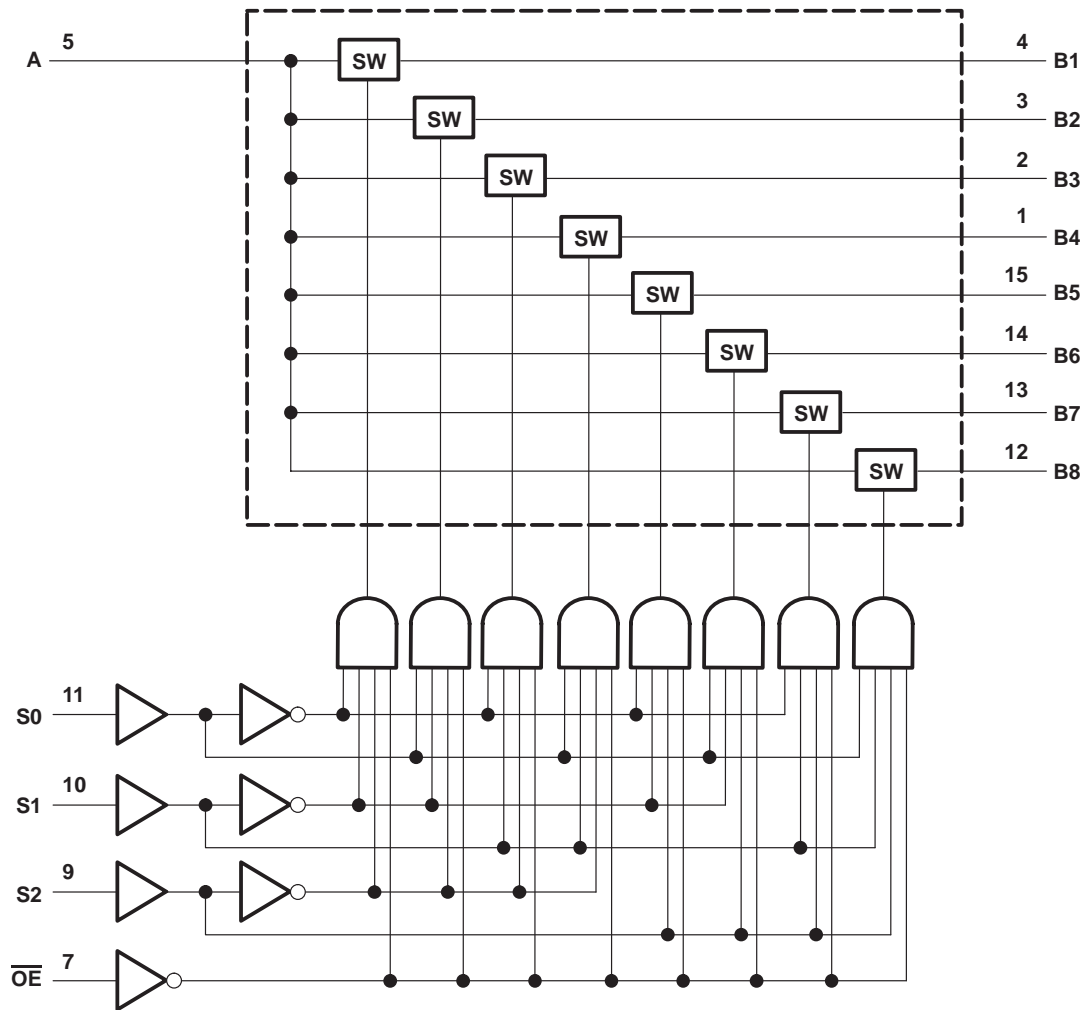
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SN74CBTLV3251
LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

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| FUNCTION TABLE | | | | |
|----------------|----|----|----|------------------|
| INPUTS | | | | FUNCTION |
| OE | S2 | S1 | S0 | |
| L | L | L | L | A port = B1 port |
| L | L | L | H | A port = B2 port |
| L | L | H | L | A port = B3 port |
| L | L | H | H | A port = B4 port |
| L | H | L | L | A port = B5 port |
| L | H | L | H | A port = B6 port |
| L | H | H | L | A port = B7 port |
| L | H | H | H | A port = B8 port |
| H | X | X | X | Disconnect |

logic diagram (positive logic)

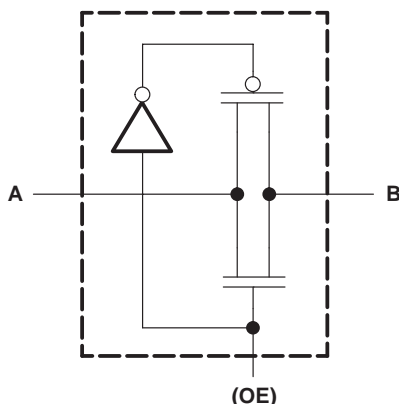


SN74CBTLV3251

LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

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simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|-----------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 4.6 V |
| Continuous channel current | 128 mA |
| Input clamp current, I_K ($V_{I/O} < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| (see Note 2): DBQ package | 90°C/W |
| (see Note 2): DGV package | 120°C/W |
| (see Note 2): PW package | 108°C/W |
| (see Note 3): RGY package | 39°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|----------|----------------------------------|--|-----|------|
| V_{CC} | Supply voltage | 2.3 | 3.6 | V |
| V_{IH} | High-level control input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2 | |
| V_{IL} | Low-level control input voltage | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ | 0.7 | V |
| | | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ | 0.8 | |
| T_A | Operating free-air temperature | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------------|---|--|---|-----|------|---------|---------------|
| V_{IK} | | $V_{CC} = 3\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| I_I | | $V_{CC} = 3.6\text{ V}$, | $V_I = V_{CC}$ or GND | | | ± 1 | μA |
| I_{off} | | $V_{CC} = 0$, | V_I or $V_O = 0$ to 3.6 V | | | 20 | μA |
| I_{CC} | | $V_{CC} = 3.6\text{ V}$, | $I_O = 0$, $V_I = V_{CC}$ or GND | | | 10 | μA |
| ΔI_{CC}^\ddagger | Control inputs | $V_{CC} = 3.6\text{ V}$, | One input at 3 V , Other inputs at V_{CC} or GND | | | 300 | μA |
| C_i | Control inputs | $V_I = 3\text{ V}$ or 0 | | | | 3 | pF |
| $C_{io}(\text{OFF})$ | A port | $V_O = 3\text{ V}$ or 0 , $\overline{OE} = V_{CC}$ | | | | 40.5 | pF |
| | B port | | | | | 6 | |
| r_{on}^\S | $V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$ | $V_I = 0$ | $I_I = 64\text{ mA}$ | | | 5 | Ω |
| | | | $I_I = 24\text{ mA}$ | | | 5 | |
| | | $V_I = 1.7\text{ V}$, | $I_I = 15\text{ mA}$ | | | 27 | |
| | $V_{CC} = 3\text{ V}$ | $V_I = 0$ | $I_I = 64\text{ mA}$ | | | 5 | |
| | | | $I_I = 24\text{ mA}$ | | | 5 | |
| | | $V_I = 2.4\text{ V}$, | $I_I = 15\text{ mA}$ | | | 10 | |

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|-----------|---------------------|----------------|---|------|---|------|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B [¶] | B or A | | 0.15 | | 0.25 | ns |
| | S | A | 1 | 6.1 | 1 | 5.3 | |
| t_{en} | S | B | 1 | 4.1 | 1 | 3.6 | ns |
| t_{dis} | S | B | 1 | 3.5 | 1 | 3.3 | ns |
| t_{en} | \overline{OE} | A or B | 1 | 5.2 | 1 | 4.5 | ns |
| t_{dis} | \overline{OE} | A or B | 1 | 6.7 | 1 | 7.2 | ns |

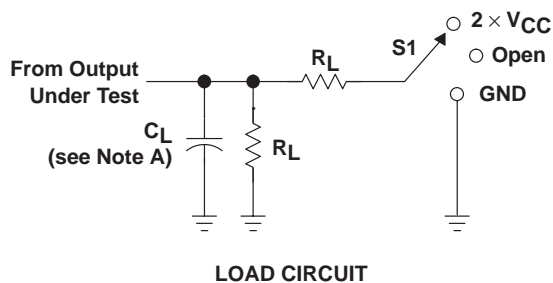
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

SN74CBTLV3251

LOW-VOLTAGE 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

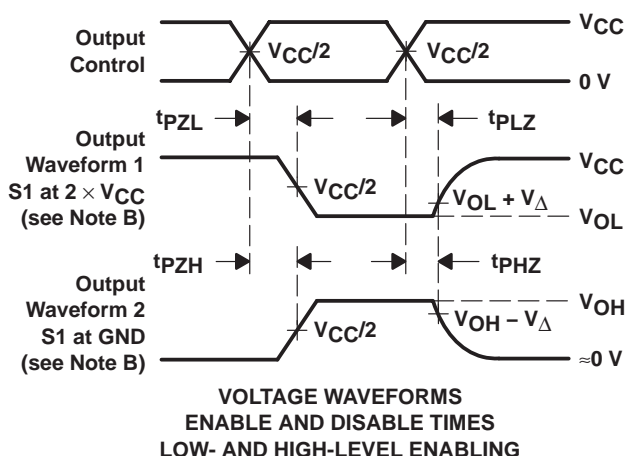
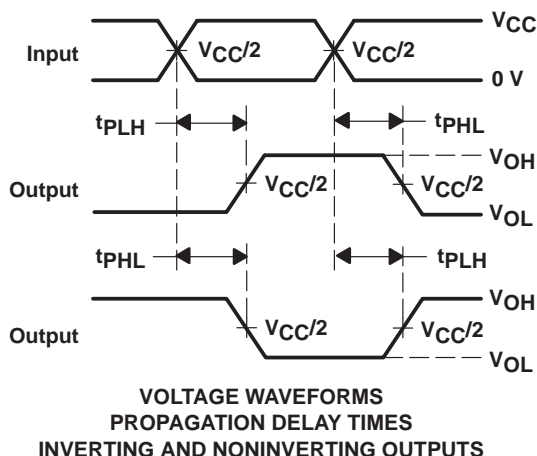
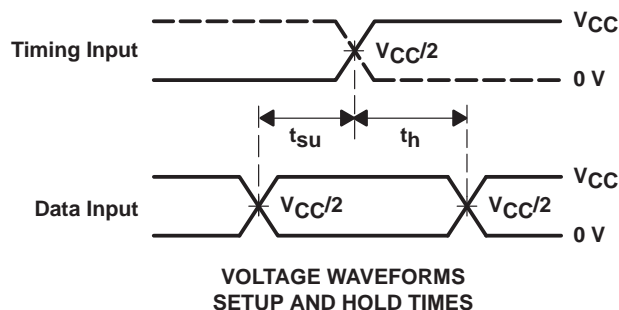
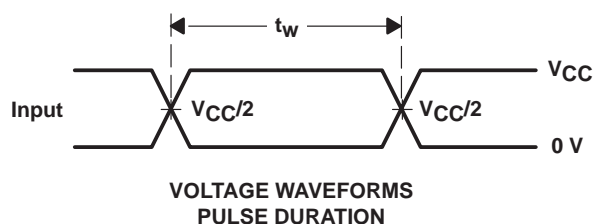
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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | C_L | R_L | V_{Δ} |
|-----------------------------------|-------|--------------|--------------|
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|---------------|-----------------|------|-------------|----------------------------|------------------|------------------------------|
| 74CBTLV3251DBQRE4 | ACTIVE | SSOP/ QSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| 74CBTLV3251DGVRE4 | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74CBTLV3251PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74CBTLV3251RGYRG4 | ACTIVE | QFN | RGY | 16 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74CBTLV3251D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBTLV3251DBQR | ACTIVE | SSOP/ QSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74CBTLV3251DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBTLV3251DGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBTLV3251DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBTLV3251DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBTLV3251PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74CBTLV3251RGYR | ACTIVE | QFN | RGY | 16 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

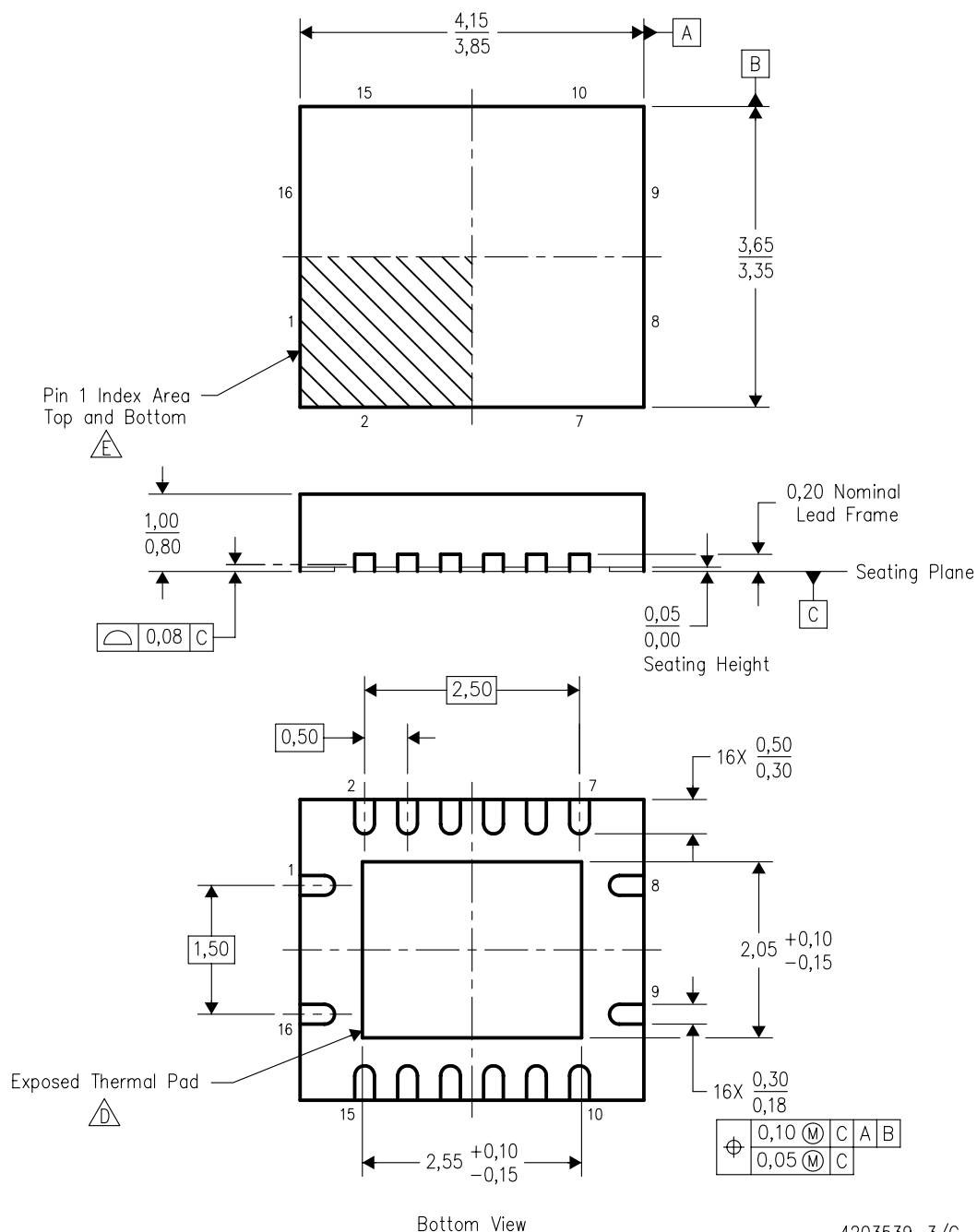
PLASTIC SMALL-OUTLINE PACKAGE





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RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK

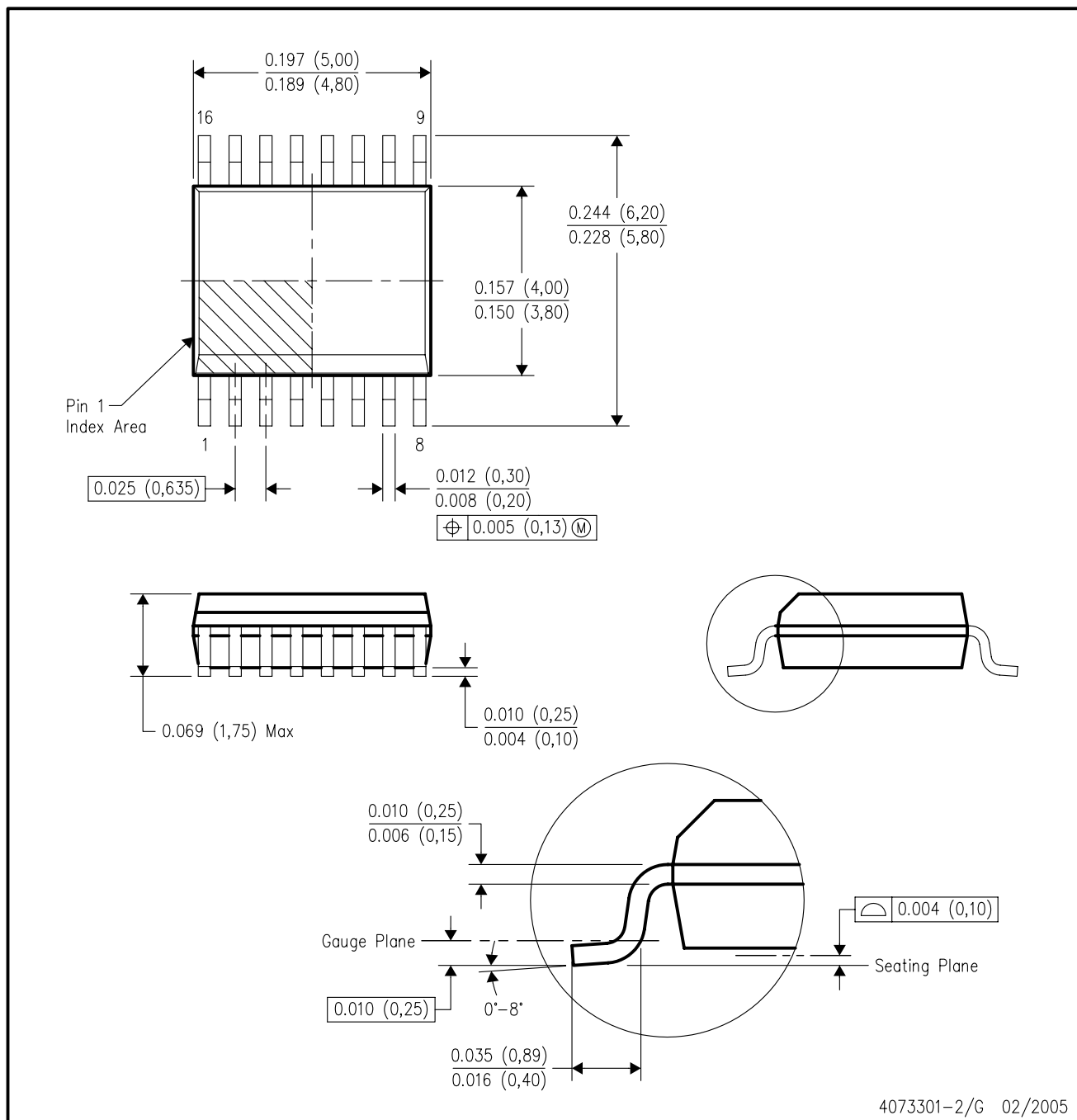


4203539-3/G 04/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 -  E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BB.

DBQ (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - Falls within JEDEC MO-137 variation AB.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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