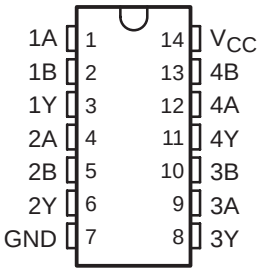
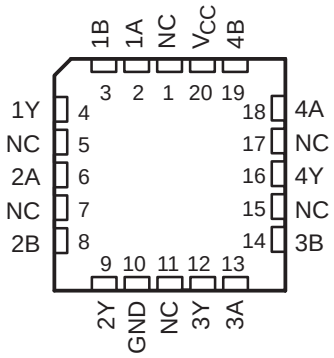
- **2-V to 5.5-V $V_{CC}$ Operation**
- **Max $t_{pd}$ of 9 ns at 5 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**SN54LV132A . . . J OR W PACKAGE**
**SN74LV132A . . . D, DB, DGV, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54LV132A . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

The ’LV132A devices are quadruple positive-NAND gates designed for 2-V to 5.5-V $V_{CC}$ operation.

The ’LV132A devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

**ORDERING INFORMATION**

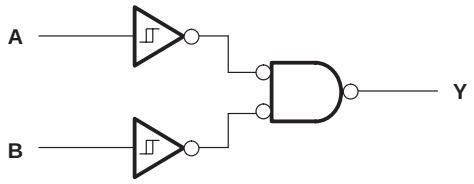
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SOIC − D | Tube of 25 | SN74LV132AD | LV132A |
| | | Reel of 2500 | SN74LV132ADR | |
| | SOP − NS | Reel of 2000 | SN74LV132ANSR | 74LV132A |
| | SSOP − DB | Reel of 2000 | SN74LV132ADBR | LV132A |
| | TSSOP − PW | Tube of 90 | SN74LV132APW | LV132A |
| | | Reel of 2000 | SN74LV132APWR | |
| | | Reel of 250 | SN74LV132APWT | |
| | TVSOP − DGV | Reel of 2000 | SN74LV132ADGVR | LV132A |
| −55°C to 125°C | CDIP − J | Tube of 25 | SNJ54LV132AJ | SNJ54LV132AJ |
| | CFP − W | Tube of 150 | SNJ54LV132AW | SNJ54LV132AW |
| | LCCC - FK | Tube of 55 | SNJ54LV132AFK | SNJ54LV132AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each gate)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance
or power-off state, $V_O$ (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . −50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
DGV package . . . . . 127°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | SN54LV132A | | SN74LV132A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | −50 | | −50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | −2 | | −2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | −6 | | −6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | −12 | | −12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | | 12 | |
| $T_A$ | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN54LV132A | | | SN74LV132A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{T+}$ Positive-going input threshold voltage | | 2.5 V | | | 1.75 | | | 1.75 | V |
| | | 3.3 V | | | 2.31 | | | 2.31 | |
| | | 5 V | | | 3.5 | | | 3.5 | |
| $V_{T−}$ Negative-going input threshold voltage | | 2.5 V | 0.75 | | | 0.75 | | | V |
| | | 3.3 V | 0.99 | | | 0.99 | | | |
| | | 5 V | 1.5 | | | 1.5 | | | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T−}$) | | 2.5 V | 0.25 | | 1 | 0.25 | | 1 | V |
| | | 3.3 V | 0.33 | | 1.32 | 0.33 | | 1.32 | |
| | | 5 V | 0.5 | | 2 | 0.5 | | 2 | |
| $V_{OH}$ | $I_{OH}$ = −50 μA | 2 V to 5.5 V | $V_{CC}$ − 0.1 | | | $V_{CC}$ − 0.1 | | | V |
| | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | 2 | | | |
| | $I_{OH}$ = −6 mA | 3 V | 2.48 | | | 2.48 | | | |
| | $I_{OH}$ = −12 mA | 4.5 V | 3.8 | | | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.44 | |
| | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | μA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | 0 | | | 5 | | | 5 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 1.9 | | | 1.9 | | pF |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV132A | | SN74LV132A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | $C_L$ = 15 pF | | 7.9* | 16.5* | 1* | 18.5* | 1 | 18.5 | ns |
| $t_{pd}$ | A or B | Y | $C_L$ = 50 pF | | 10.8 | 20.2 | 1 | 23 | 1 | 23 | ns |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV132A | | SN74LV132A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | $C_L$ = 15 pF | | 5.6* | 11.9* | 1* | 14* | 1 | 14 | ns |
| $t_{pd}$ | A or B | Y | $C_L$ = 50 pF | | 7.6 | 15.4 | 1 | 17.5 | 1 | 17.5 | ns |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54LV132A | | SN74LV132A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | $C_L$ = 15 pF | | 3.9* | 7.7* | 1* | 9* | 1 | 9 | ns |
| $t_{pd}$ | A or B | Y | $C_L$ = 50 pF | | 5.3 | 9.7 | 1 | 11 | 1 | 11 | ns |



* On products compliant to MIL-PRF-38535, this parameter is not production tested.

### noise characteristics, $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 5)

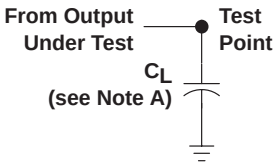
| PARAMETER | | SN74LV132A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.21 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | −0.09 | −0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 3.12 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

NOTE 5: Characteristics are for surface-mount packages only.

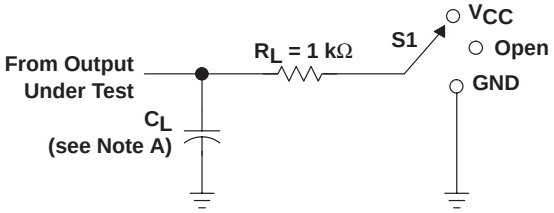
### operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 10 MHz | 3.3 V | 7.5 | pF |
| | | | 5 V | 11.2 | |

## PARAMETER MEASUREMENT INFORMATION

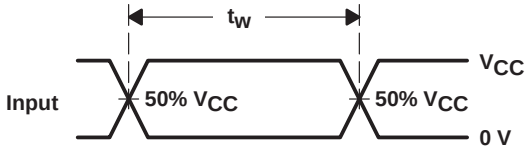



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

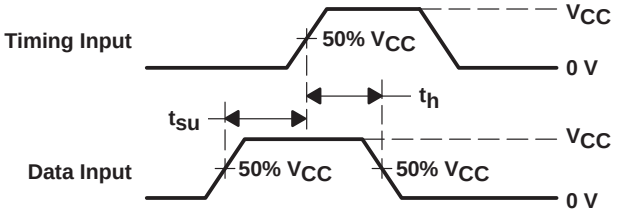



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

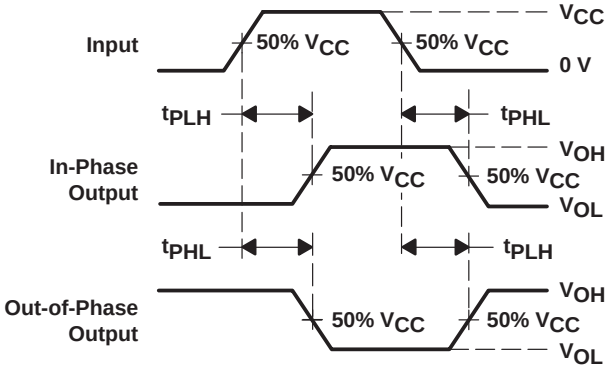
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



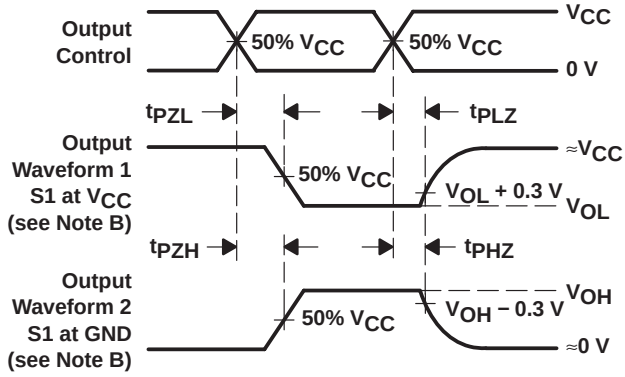

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



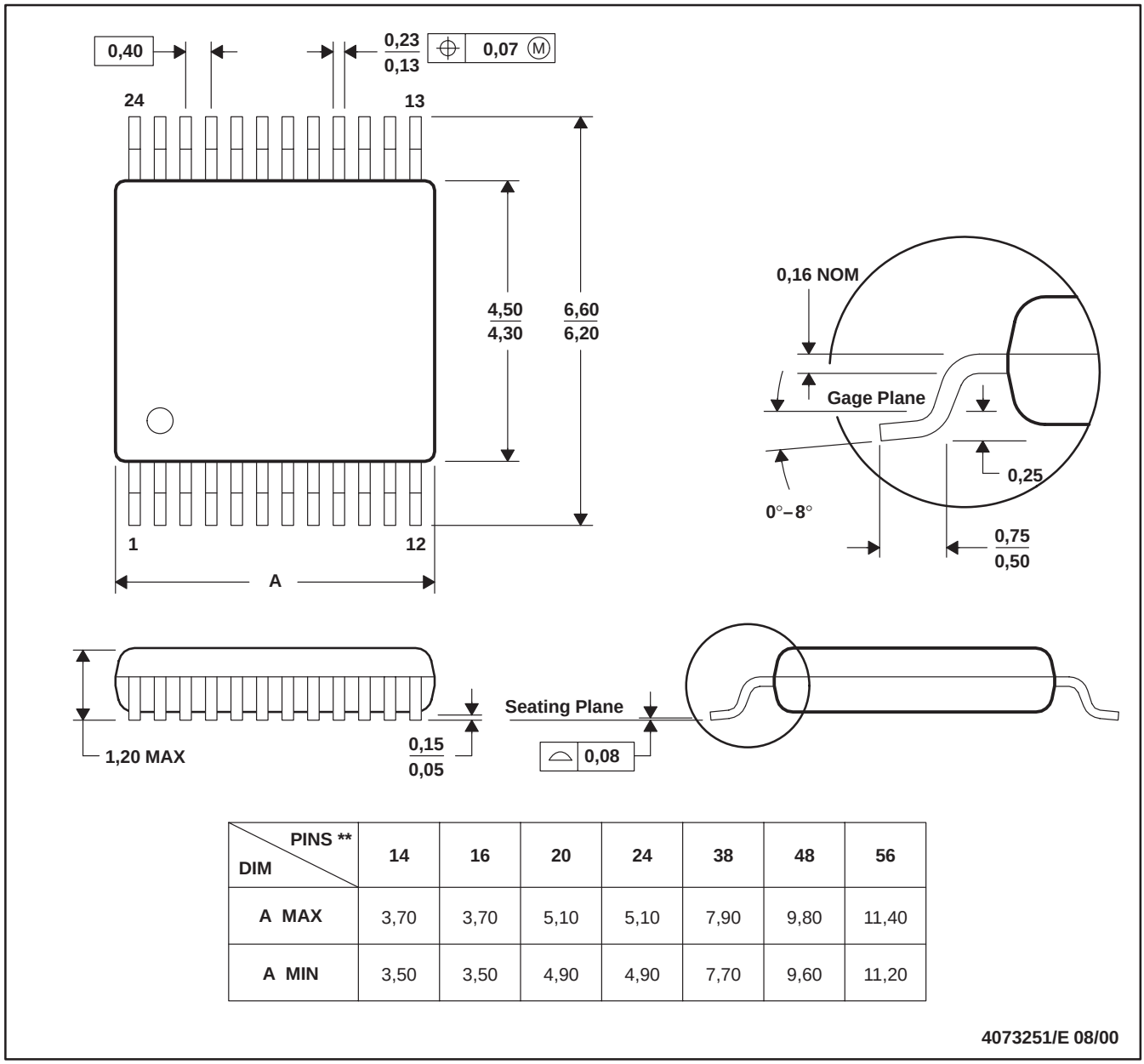

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

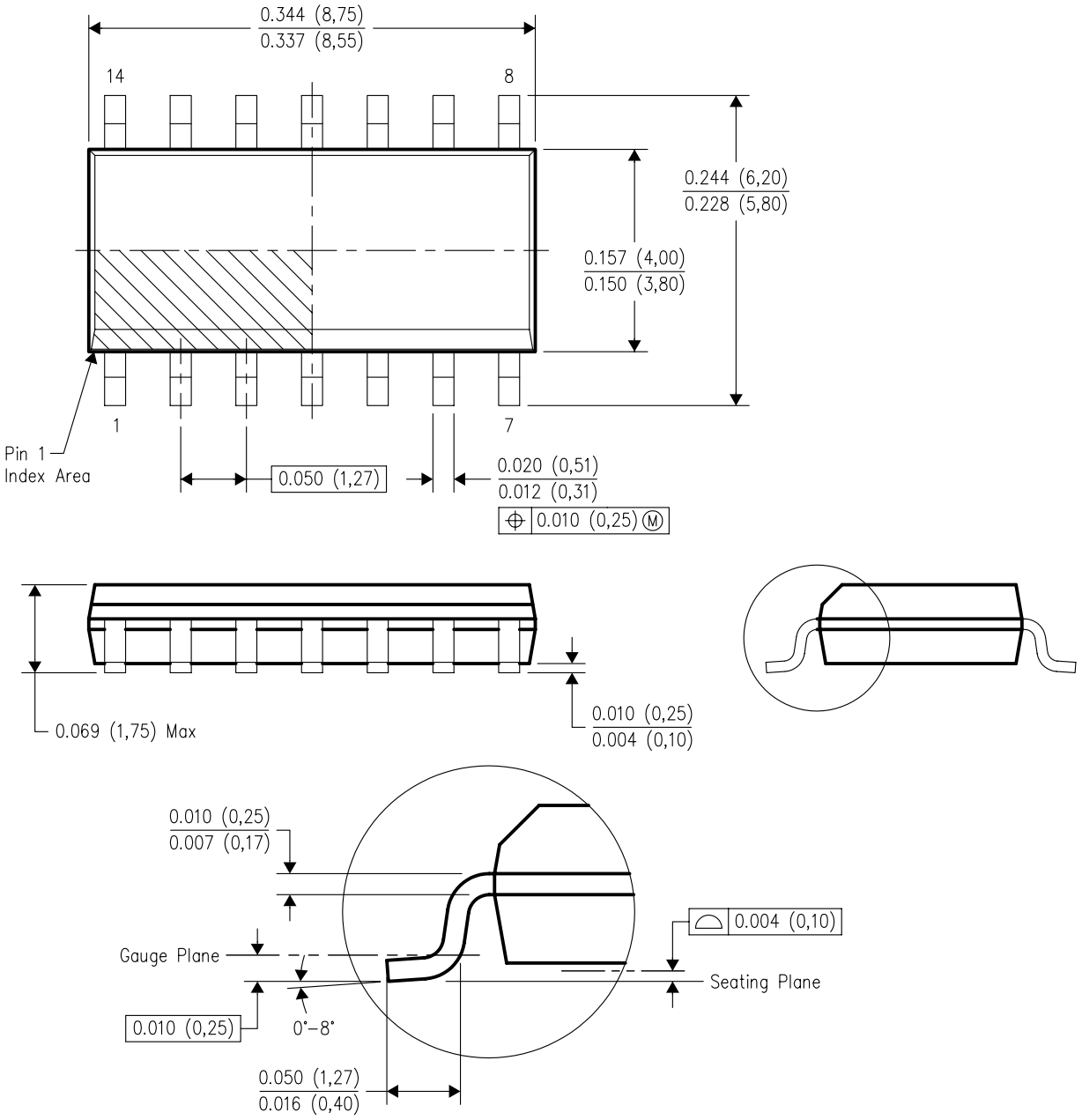



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

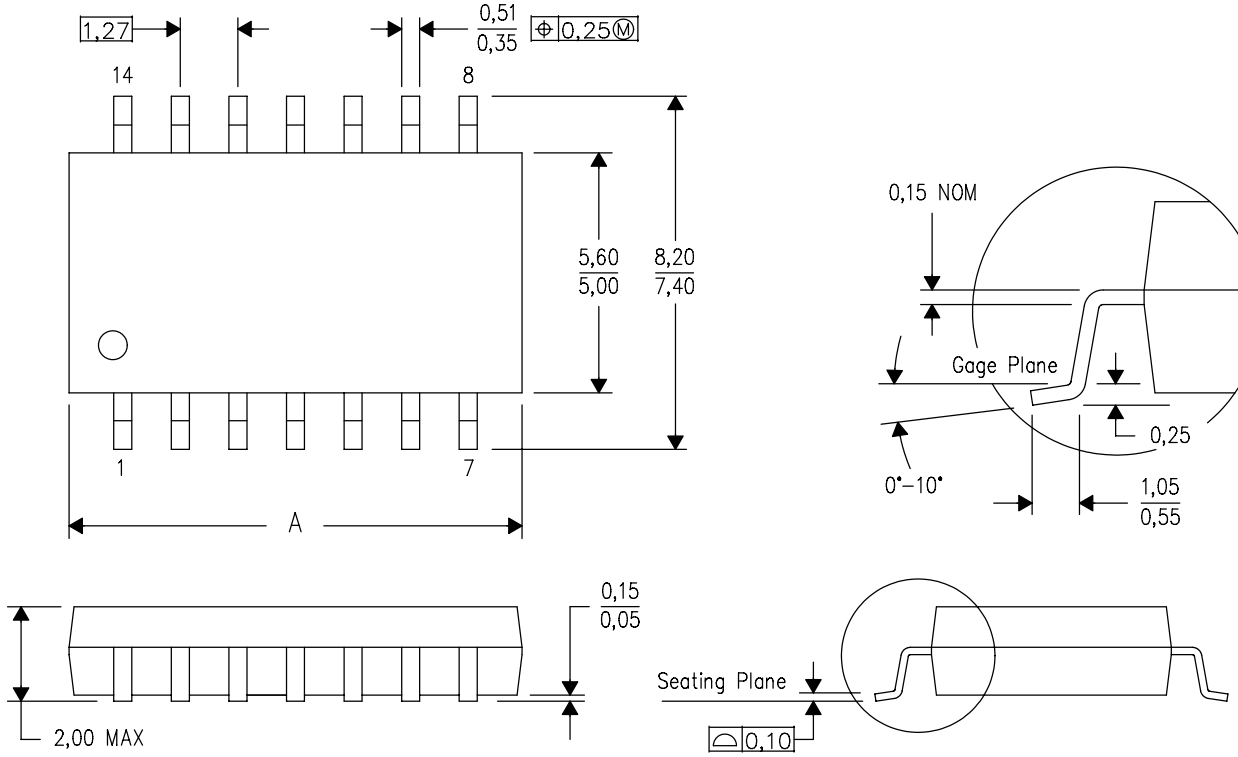



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

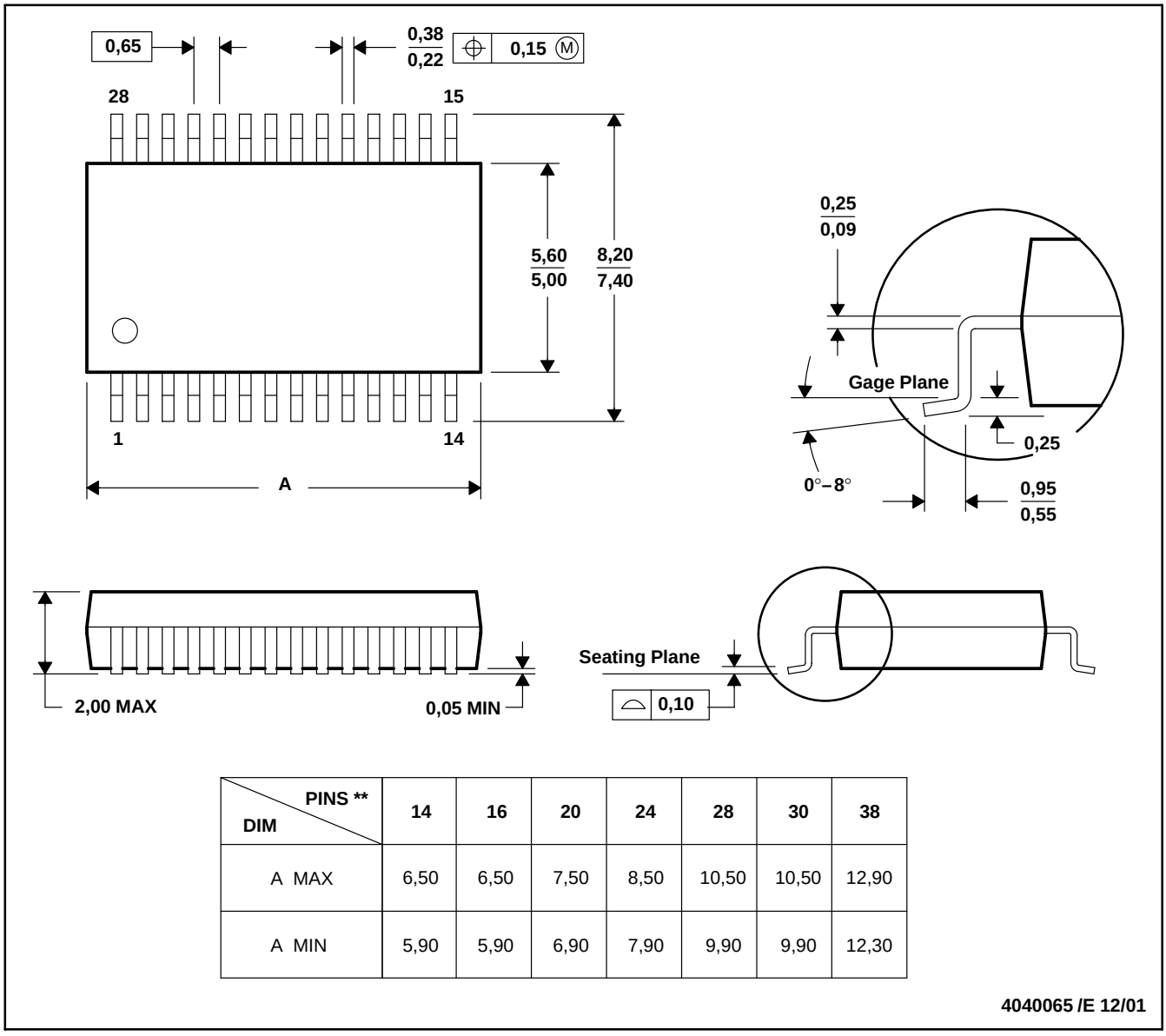
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



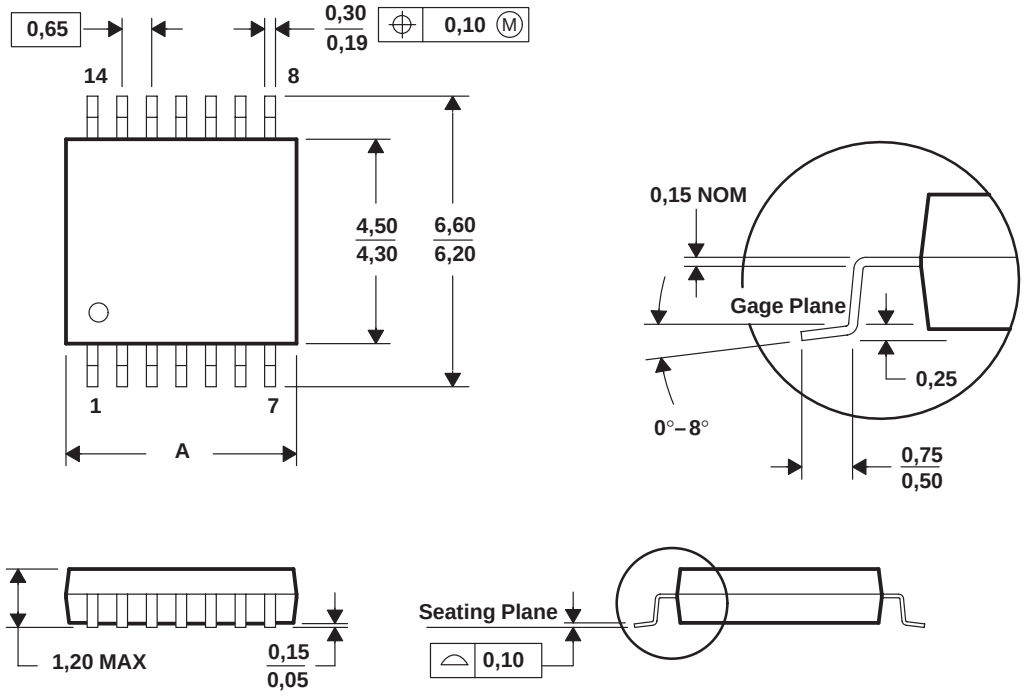

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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