

N-Channel 60-V (D-S) MOSFET

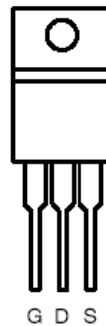
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, and cordless telephones.

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
60	16.5 @ $V_{GS} = 10V$	90 ^a
	21 @ $V_{GS} = 4.5V$	

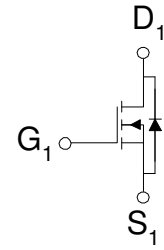
- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TO-220 saves board space
- Fast switching speed
- High performance trench technology

TO-220AB



Top View

DRAIN connected to TAB



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25^\circ\text{C}$	I_D	90	A
Pulsed Drain Current ^b		I_{DM}	240	
Continuous Source Current (Diode Conduction) ^a		I_S	90	A
Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	300	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	0.5	$^\circ\text{C/W}$

Notes

- Package Limited
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			25	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$			16.5	mΩ
		$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$			21	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 2 \text{ A}$		30		S
Diode Forward Voltage	V_{SD}	$I_S = 2 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 2 \text{ A}$		26		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			13		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 \text{ V}, R_L = 25 \text{ } \Omega \text{ , } I_D = 2 \text{ A},$ $V_{GEN} = 10 \text{ V}$		6		nS
Rise Time	t_r			6		
Turn-Off Delay Time	$t_{d(off)}$			58		
Fall-Time	t_f			20		

Notes

- Pulse test: $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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