



SCCS016 - May 1994 - Revised February 2000

# CY74FCT191T

## 4-Bit Up/Down Binary Counter

### Features

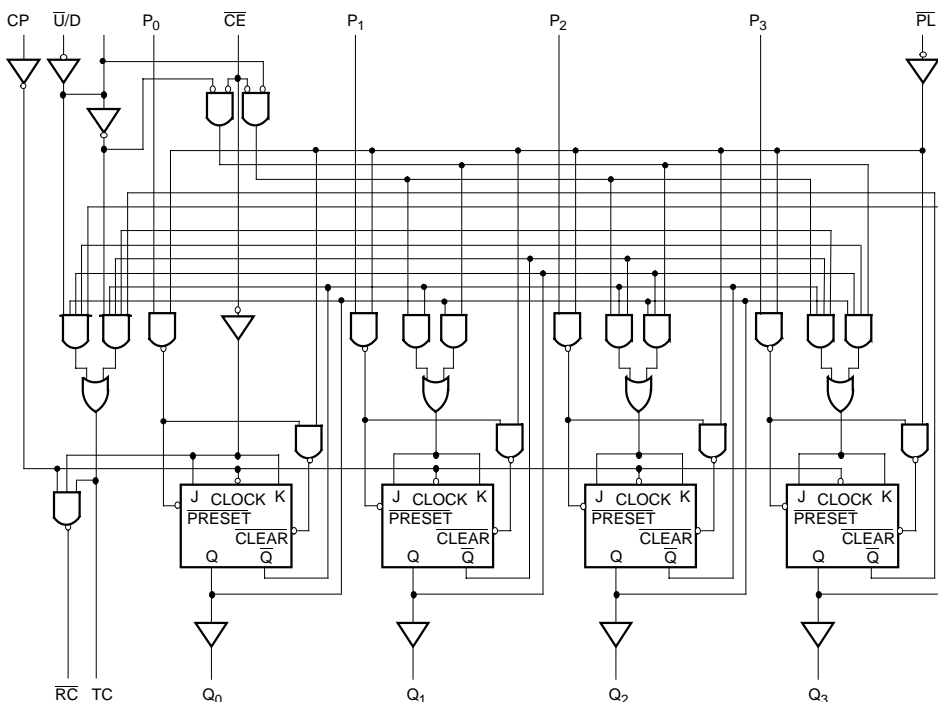
- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 6.2 ns max,  
FCT-A speed at 7.8 ns max.
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable permits live insertion
- ESD > 2000V
- Matched rise and fall times
- Sink current 64 mA  
Source current 32 mA

### Functional Description

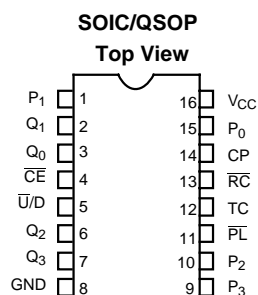
The FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple clock output make possible a variety of methods of implementing multusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

### Logic Block Diagram



### Pin Configurations



### Pin Description

Name	Description
CE	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P	Parallel Data Inputs
PL	Asynchronous Parallel Load Input (Active LOW)
U/D	Up/Down Count Control Input
Q	Flip-Flop Outputs
RC	Ripple Clock Output (Active LOW)
TC	Terminal Count Output



### RC Function Table<sup>[1]</sup>

Inputs		Outputs	
CE	CP	T <sup>[2]</sup>	RC
L	⌋	H	⌋
H	X	X	H
X	X	L	H



**RC Function Table<sup>[1]</sup>**

Inputs		Outputs	
CE	CP	T <sup>[2]</sup>	RC

**Notes:**

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care,  
 = LOW-to-HIGH clock transition.  = Low Pulse.
- TC is generated internally.

**Mode Select<sup>[1]</sup>**

Inputs				Mode
PL	CE	U/D	CP	
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

**Maximum Ratings<sup>[3, 4]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0			V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs		0.2		V
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>			5	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V			±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V			±1	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V	-60	-120	-225	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V			±1	μA

**Capacitance<sup>[6]</sup>**

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Notes:**

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

Ambient Temperature with  
 Power Applied..... -65°C to +135°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Input Voltage ..... -0.5V to +7.0V  
 DC Output Voltage..... -0.5V to +7.0V  
 DC Output Current (Maximum Sink Current/Pin) ..... 120 mA  
 Power Dissipation ..... 0.5W  
 Static Discharge Voltage..... >2001V  
 (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	-40°C to +85°C	5V ± 5%

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}, V_{IN} \leq 0.2V,$ $V_{IN} \geq V_{CC}-0.2V$	0.1	0.2	mA
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}, V_{IN}=3.4V,$ <sup>[8]</sup> $f_1=0, \text{Outputs Open}$	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[9]</sup>	$V_{CC}=\text{Max.}, \text{One Bit Toggling, Preset Mode,}$ 50% Duty Cycle, Outputs Open, $MR=V_{CC}=\overline{SR},$ $PL=\overline{CE}=\overline{U/D}=CP=GND,$ $V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC}-0.2V$	0.06	0.12	mA/MHz
$I_C$	Total Power Supply Current <sup>[10]</sup>	$V_{CC}=\text{Max.}, \text{Preset Mode,}$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5 \text{ MHz},$ $PL=\overline{CE}=\overline{U/D}=CP=GND,$ $V_{IN}=V_{CC}, V_{IN}=GND$	0.4	0.8	mA
		$V_{CC}=\text{Max.}, \text{Preset Mode,}$ 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5 \text{ MHz},$ $V_{IN}=3.4V \text{ or } V_{IN}=GND$	0.7	1.8	mA
		$V_{CC}=\text{Max.}, \text{Preset Mode,}$ 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1=5 \text{ MHz},$ $PL=\overline{CE}=\overline{U/D}=CP=GND,$ $V_{IN}=V_{CC}, V_{IN}=GND$	1.3	2.6 <sup>[11]</sup>	mA
		$V_{CC}=\text{Max.}, \text{Preset Mode,}$ 50% Duty Cycle, Outputs Open, Four Bits Toggling at $f_1=5 \text{ MHz},$ $PL=\overline{CE}=\overline{U/D}=CP=GND,$ $V_{IN}=3.4V \text{ or } V_{IN}=GND$	2.3	6.6 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range

Parameter	Description	CY74FCT191AT		CY74FCT191CT		Unit	Fig. No. <sup>[13]</sup>
		Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	1.5	7.8	1.5	6.2	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to TC	1.5	11.8	1.5	9.4	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to RC	1.5	8.5	1.5	6.8	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CE to RC	1.5	7.2	1.5	6.0	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay U/D to RC	1.5	13.0	1.5	11.0	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay U/D to TC	1.5	7.2	1.5	6.1	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>n</sub> to Q <sub>n</sub>	1.5	9.1	1.5	7.7	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay PL to Q <sub>n</sub>	2.0	8.5	2.0	7.2	ns	1, 5
t <sub>SU</sub>	Set-Up Time HIGH or LOW P <sub>n</sub> to PL	4.0		3.5		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW P <sub>n</sub> to PL	1.5		1.0		ns	4
t <sub>SU</sub>	Set-Up Time LOW CE to CP	9.0		7.2		ns	4
t <sub>H</sub>	Hold Time LOW CE to CP	0		0		ns	4
t <sub>SU</sub>	Set-Up Time HIGH or LOW U/D to CP	10.0		8.0		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW U/D to CP	0		0		ns	4
t <sub>W</sub>	PL Pulse Width LOW	5.5		5.0		ns	5
t <sub>W</sub>	Clock Pulse Width <sup>[6]</sup> HIGH or LOW	4.0		4.0		ns	5
t <sub>REM</sub>	Recovery Time PL to CP	5.0		4.5		ns	6

**Notes:**

12. Minimum limits are specified but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.

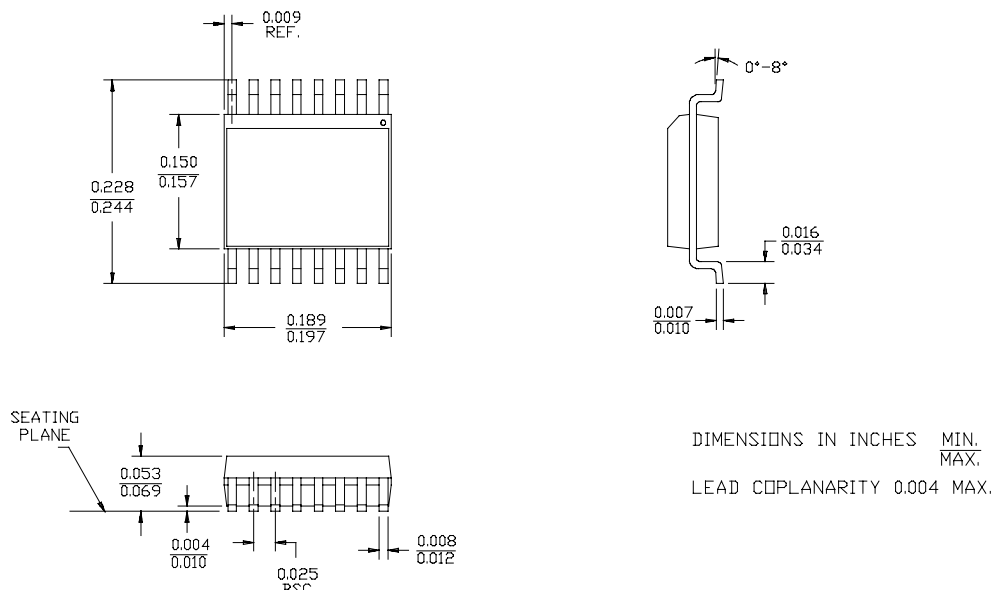
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.2	CY74FCT191CTQCT	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY74FCT191CTSOC/SOCT	S1	16-Lead (300-Mil) Molded SOIC	
7.8	CY74FCT191ATSOC/SOCT	S1	16-Lead (300-Mil) Molded SOIC	Commercial

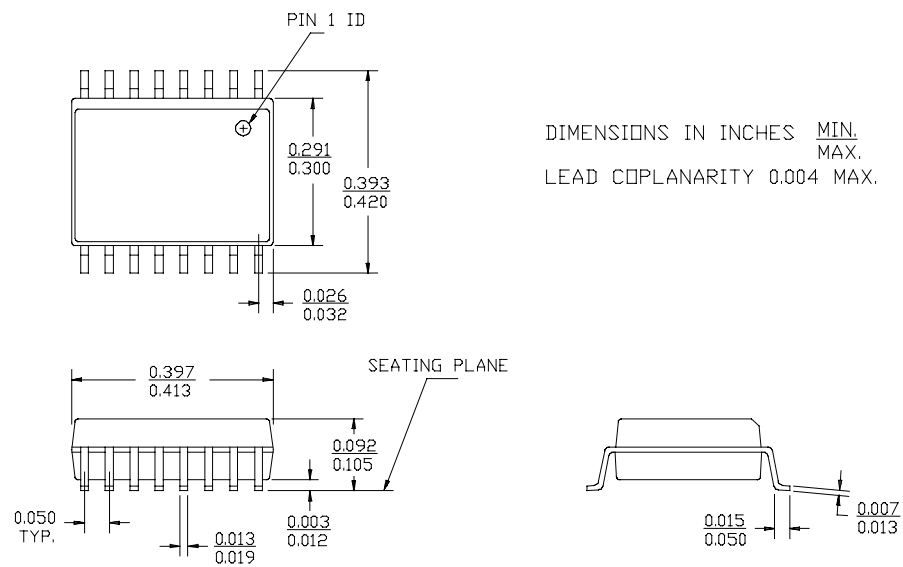
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**Package Diagrams**

**16-Lead Quarter Size Outline Q1**



**16-Lead Molded SOIC S1**



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