

R1LV0808ASB – 5SI, 7SI

8Mb Advanced LPSRAM (1024k word x 8bit)

REJ03C0394-0100

Rev.1.00

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Description

The R1LV0808ASB is a family of low voltage 8-Mbit static RAMs organized as 1,048,576-words by 8-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1LV0808ASB is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The R1LV0808ASB is packaged in a 44pin thin small outline mount device [11.76mm×18.41mm 44-pin plastic TSOP (II)]. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

Features

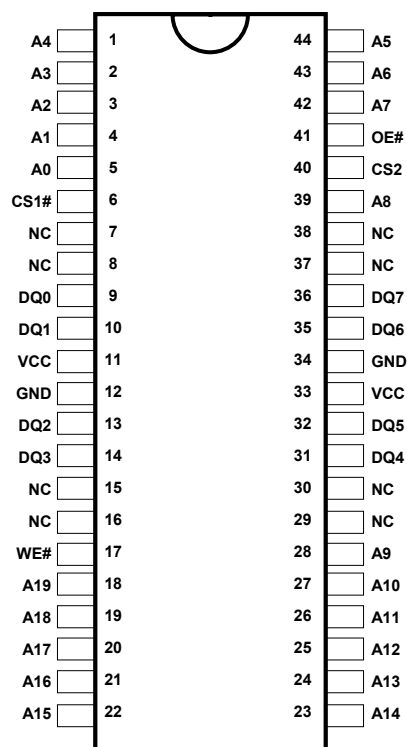
- Single 2.4-3.6V power supply
- Small stand-by current: 1.2μA (Vcc=3.0V, typ.)
- No clocks, No refresh
- All inputs and outputs are TTL compatible
- Easy memory expansion by CS1# and CS2
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Operation temperature: -40 ~ +85°C
-

Ordering information

Type No.	Power supply	Access time	Temperature Range	Package
R1LV0808ASB-5SI	2.7V to 3.6V	55 ns	-40 ~ +85°C	11.76mm×18.41mm 44-pin plastic TSOP (II) (normal-bend type) (44P3F)
	2.4V to 2.7V	70 ns		
R1LV0808ASB-7SI	2.4V to 3.6V	70 ns		

Pin Arrangement

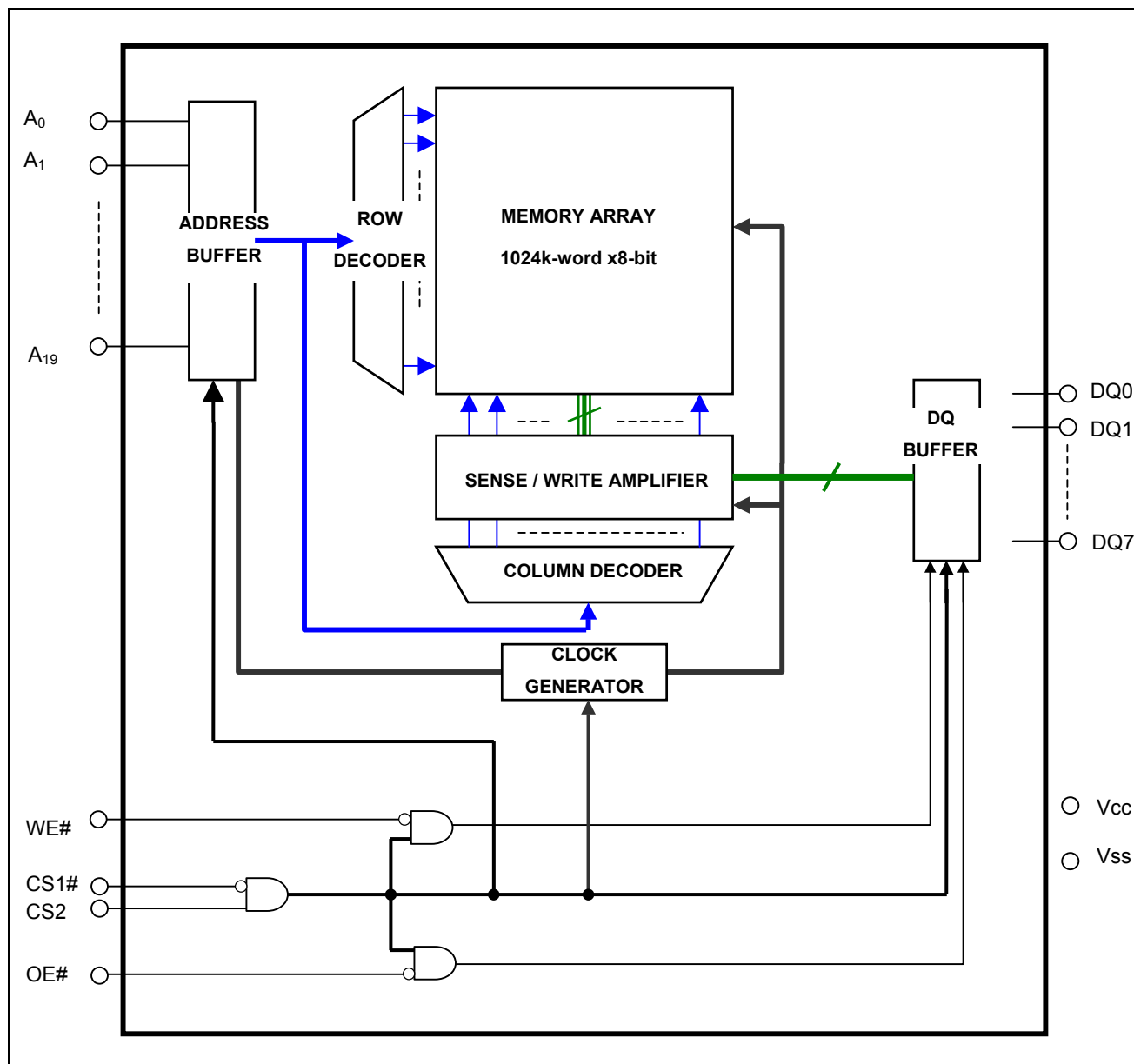
44-pin TSOP (II)



Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A19	Address input (word mode)
DQ0 to DQ7	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
NC	Non connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	DQ0~7	Operation
X	L	X	X	High-Z	Stand-by
H	X	X	X	High-Z	Stand-by
L	H	L	X	Din	Write
L	H	H	L	Dout	Read
L	H	H	H	High-Z	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Terminal voltage on any pin relative to Vss	V_T	-0.5^{*1} to $V_{cc}+0.3^{*2}$	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 1. -3.0V in case of AC (Pulse width ≤ 30 ns)

2. Maximum voltage is +4.6V

Recommend Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Supply voltage	V _{CC}	2.4	3.0	3.6	V	-	
	V _{SS}	0	0	0	V	-	
Input high voltage	V _{IH}	2.0	-	V _{CC} +0.2	V	V _{CC} =2.4V to 2.7V	
		2.2	-	V _{CC} +0.2	V	V _{CC} =2.7V to 3.6V	
Input low voltage	V _{IL}	-0.2	-	0.4	V	V _{CC} =2.4V to 2.7V	1
		-0.2	-	0.6	V	V _{CC} =2.7V to 3.6V	1
Ambient temperature range	T _a	-40	-	+85	°C	-	

Note 1. -3.0V in case of AC (Pulse width ≤30ns)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I _{LI}	-	-	1	μA	Vin = Vss to Vcc	
Output leakage current	I _{LO}	-	-	1	μA	CS1# =V _{IH} or CS2 =V _{IL} or OE# =V _{IH} or WE# =V _{IL} , VI/O =Vss to Vcc	
Average operating current	I _{CC1}	-	20 ^{*1}	35	mA	Min. cycle, duty =100%, II/O = 0mA CS1# =V _{IL} , CS2 =V _{IH} , Others = V _{IH} /V _{IL}	
	I _{CC2}	-	2 ^{*1}	5	mA	Cycle =1μs, duty =100%, II/O = 0mA CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V, V _{IH} ≥ V _{CC} -0.2V, V _{IL} ≤ 0.2V	
Standby current	I _{SB}	-	-	1	mA	CS2 =V _{IL}	
Standby current	I _{SB1}	-	1.2 ^{*1}	4	μA	~+25°C	Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V
		-	3 ^{*2}	6	μA	~+40°C	
		-	-	15	μA	~+70°C	
		-	-	20	μA	~+85°C	
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -1mA Vcc≥2.7V	
	V _{OH2}	2.0	-	-	V	I _{OH} = -0.1mA	
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA Vcc≥2.7V	
	V _{OL2}	-	-	0.4	V	I _{OL} = 0.1mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V(T_a=+25°C), and not 100% tested.

2. Typical parameter indicates the value for the center of distribution at 3.0V(T_a=+40°C), and not 100% tested.

Capacitance

(Ta =25°C, f =1MHz)

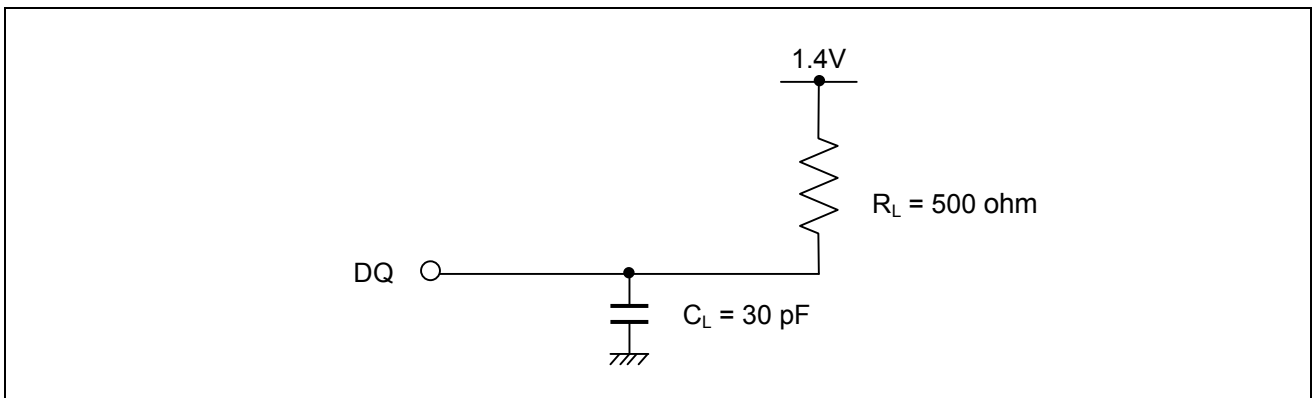
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C _{in}	-	-	10	pF	V _{in} =0V	1
Input / output capacitance	C _{I/O}	-	-	10	pF	V _{I/O} =0V	1

Note 1. Typical parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (V_{cc} = 2.4V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels: V_{IL} = 0.4V, V_{IH} = 2.4V (V_{cc} = 2.7V ~ 3.6 V)
V_{IL} = 0.4V, V_{IH} = 2.2V (V_{cc} = 2.4V ~ 2.7 V)
- Input rise and fall times: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read cycle

Parameter	Symbol	R1LV0808ASB-5SI (Note 0)		R1LV0808ASB-7SI		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	55	-	70	-	ns	
Address access time	t_{AA}	-	55	-	70	ns	
Chip select access time	t_{ACS1}	-	55	-	70	ns	
	t_{ACS2}	-	55	-	70	ns	
Output enable to output valid	t_{OE}	-	30	-	35	ns	
Output hold from address change	t_{OH}	10	-	10	-	ns	
Chip select to output in low-Z	t_{CLZ1}	10	-	10	-	ns	2,3
	t_{CLZ2}	10	-	10	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1,2,3
	t_{CHZ2}	0	20	0	25	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2,3

Write Cycle

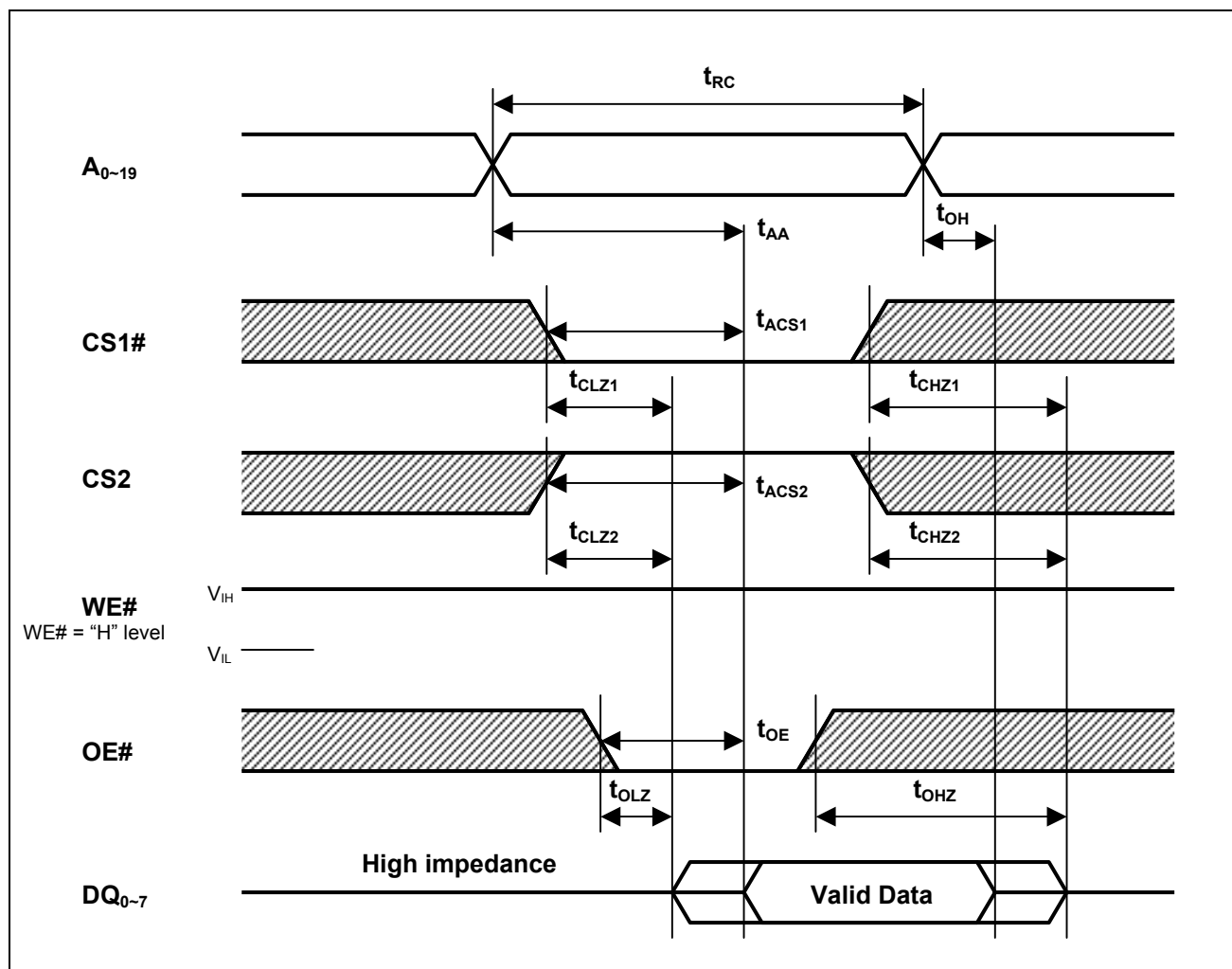
Parameter	Symbol	R1LV0808ASB-5SI (Note 0)		R1LV0808ASB-7SI		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	55	-	70	-	ns	
Address valid to end of write	t_{AW}	50	-	65	-	ns	
Chip select to end of write	t_{CW}	50	-	65	-	ns	5
Write pulse width	t_{WP}	40	-	55	-	ns	4
Address setup time	t_{AS}	0	-	0	-	ns	6
Write recovery time	t_{WR}	0	-	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	35	-	ns	
Data hold from write time	t_{DH}	0	-	0	-	ns	
Output enable from end of write	t_{OW}	5	-	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1,2

Note 0. If Vcc is 2.4-2.7V, parameters of R1LV0808ASB-7SI (70ns) are applied.

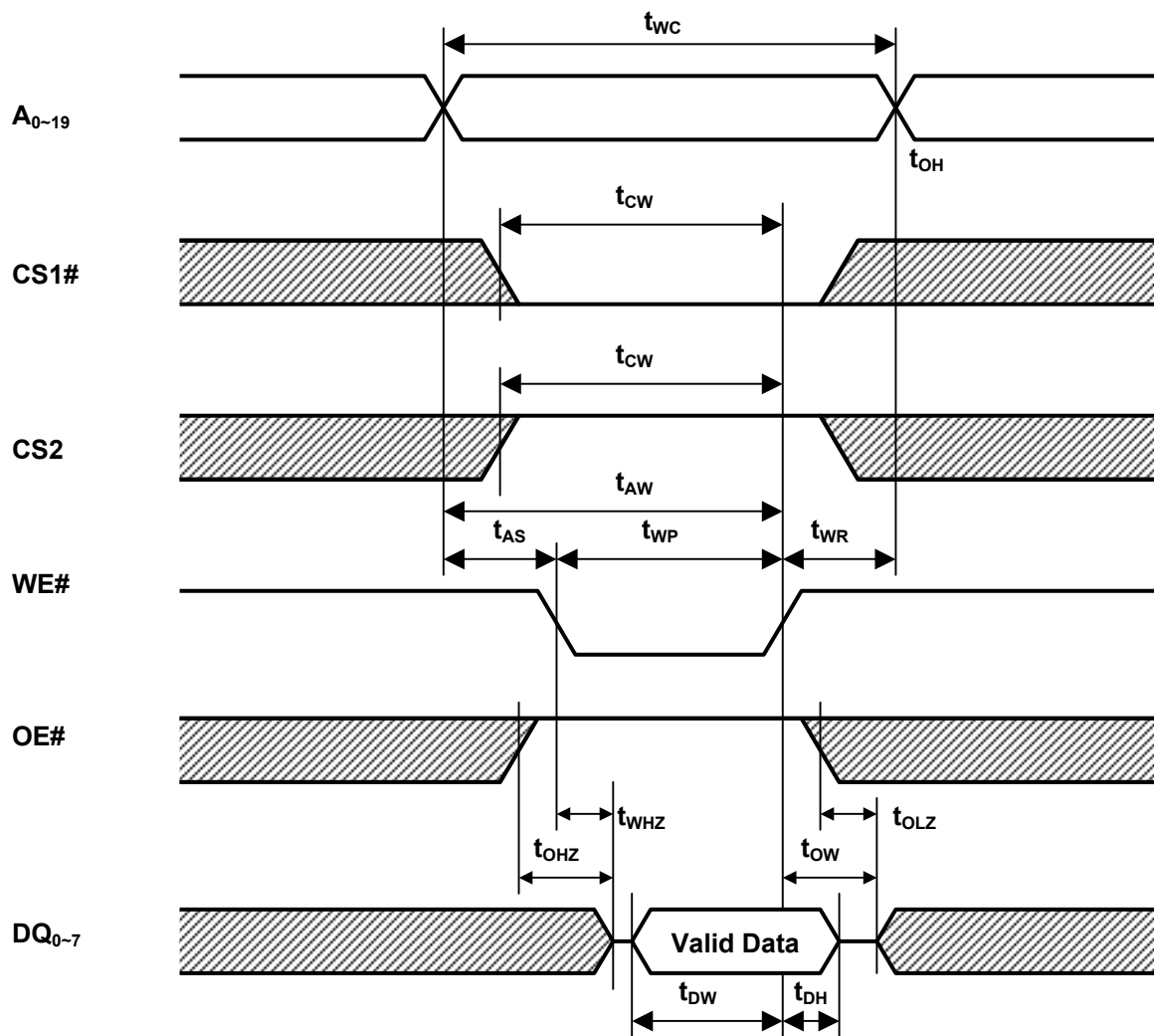
1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. Typical parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# .
A write begins at the latest transitions among CS1# going low, CS2 going high and WE# going low.
A write ends at the earliest transitions among CS1# going high, CS2 going low and WE# going high.
 t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.
6. t_{AS} is measured the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle

Timing Waveforms

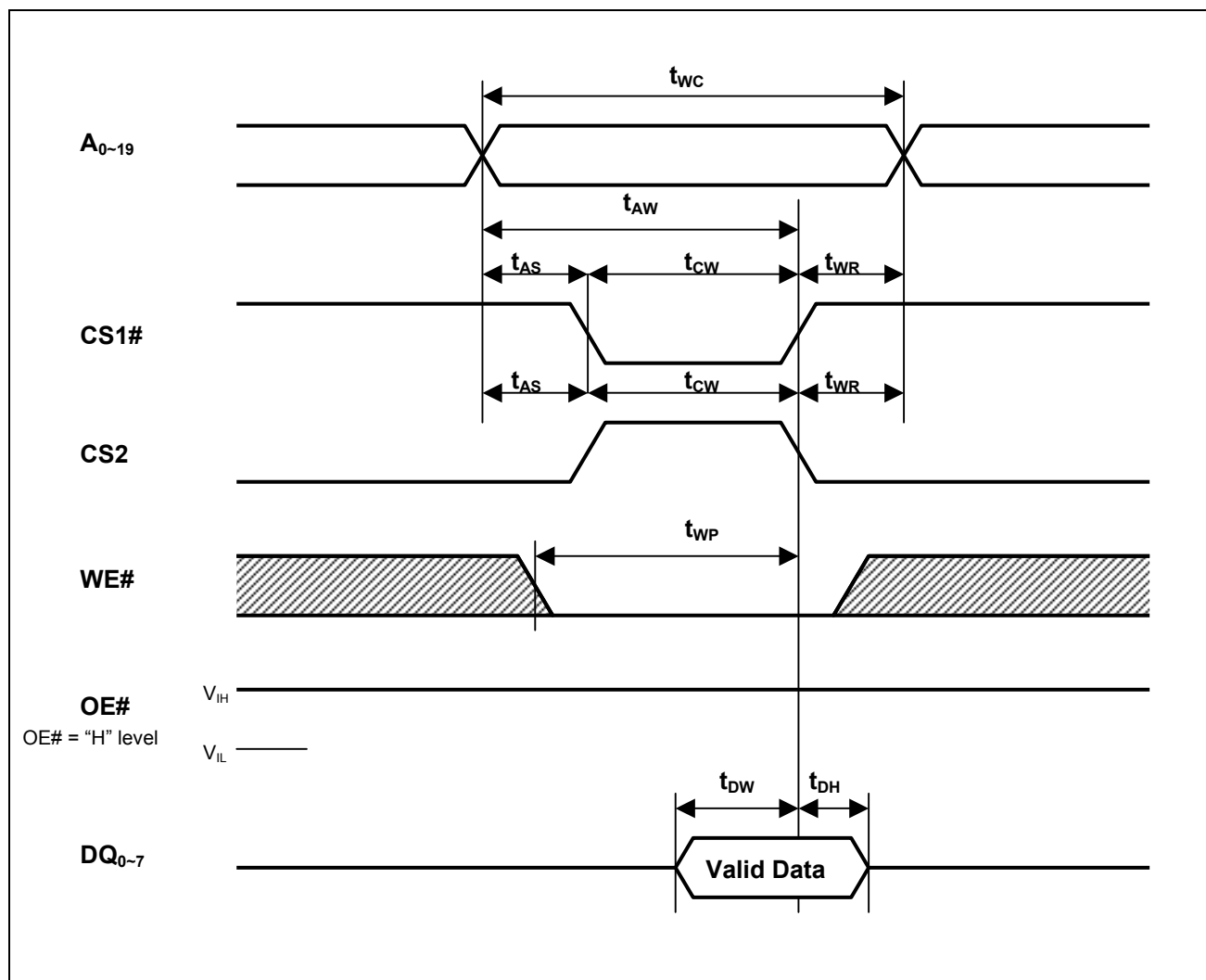
Read Cycle



Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS1#, CS2 CLOCK)



Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*3}	
V _{CC} for data retention	V _{DR}	1.5	-	3.6	V	Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V	
Data retention current	I _{CCDR}	-	1.2 ^{*1}	4	μA	~+25°C	Vcc=3.0V, Vin ≥ 0V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V
		-	3 ^{*2}	6	μA	~+40°C	
		-	-	15	μA	~+70°C	
		-	-	20	μA	~+85°C	
Chip select to data retention time	t _{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t _R	5	-	-	ms		

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V($T_a = +25^{\circ}C$), and not 100% tested.

2. Typical parameter indicates the value for the center of distribution at 3.0V($T_a = +40^{\circ}C$), and not 100% tested.

3. CS2 controls address buffer, WE# buffer, CS1# Buffer, OE# buffer and Din buffer.

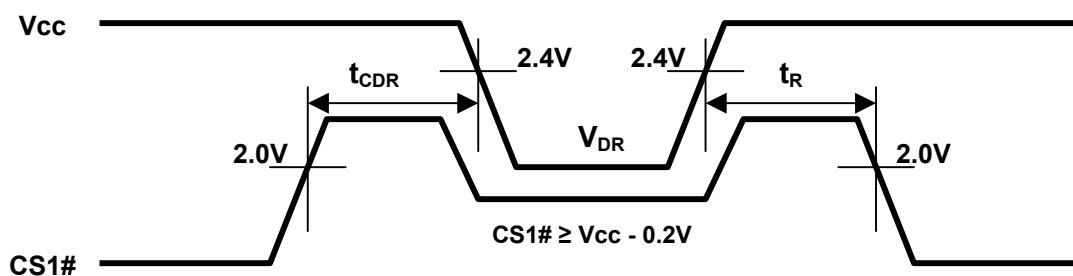
If CS2 controls data retention mode, Vin levels (address, WE#, OE #, DQ) can be in the high impedance state.

If CS1# controls data retention mode, CS2 must be $CS2 \geq V_{CC}-0.2V$ or $0V \leq CS2 \leq 0.2V$.

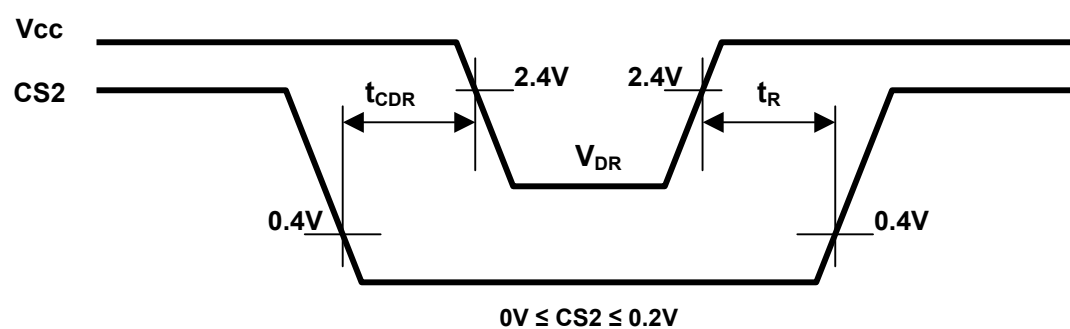
The other inputs levels (address, WE#, OE#, DQ) can be in the high impedance state.

Data Retention Timing Waveforms

(1) CS# controlled



(2) CS2 controlled



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April 1st, 2010
Renesas Electronics Corporation

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