



**Advanced
Micro
Devices**

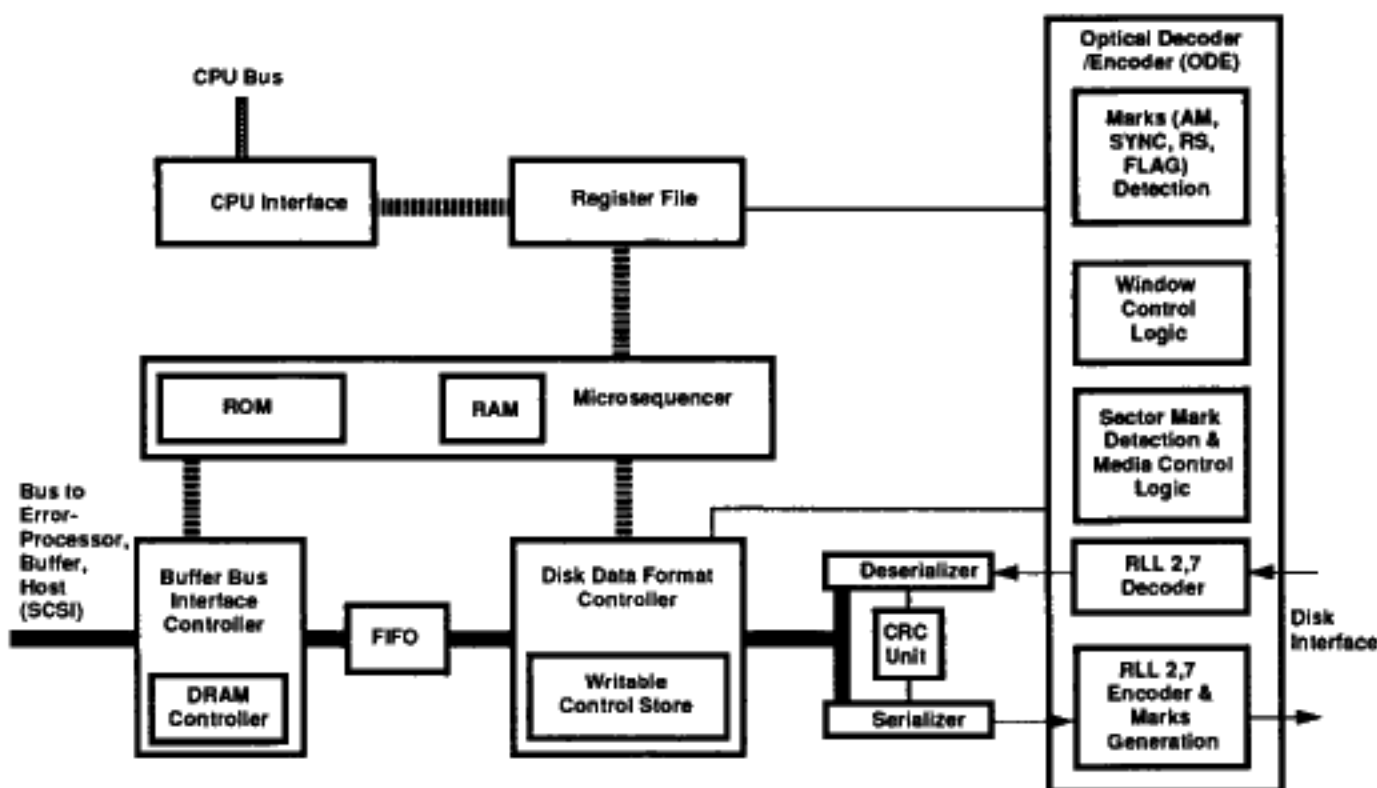
Am95C98

Integrated Optical Disk Controller

DISTINCTIVE CHARACTERISTICS

- Supports X3B11 (1990) Continuous Composite Servo WORM/Erasable Optical Formats for both 90 mm and 130 mm drives
- 2,7 RLL Encoder/Decoder
- User programmable disk format functions
- High Level Command Set
- Supports Intelligent SCSI-type Interfaces
- On-chip Buffer Management with direct support of up to 4 MBytes of DRAM
- Performs sector, address, sync marks and resync bytes detection and generation
- Supports zone bit recording
- High-speed Operation up to 25 Mbits/s NRZ data rate (50 Mbits/s RLL)
- 20 MHz System Clock
- Employs data recovery schemes for corrupted data
- Supports drives with ODF (Mirror Mark) and Written Flag
- Handles error correction in conjunction with the Am95C94 Advanced Burst Error Processor (ABEP)

INTERNAL BLOCK DIAGRAM



15940B-014A

GENERAL DESCRIPTION

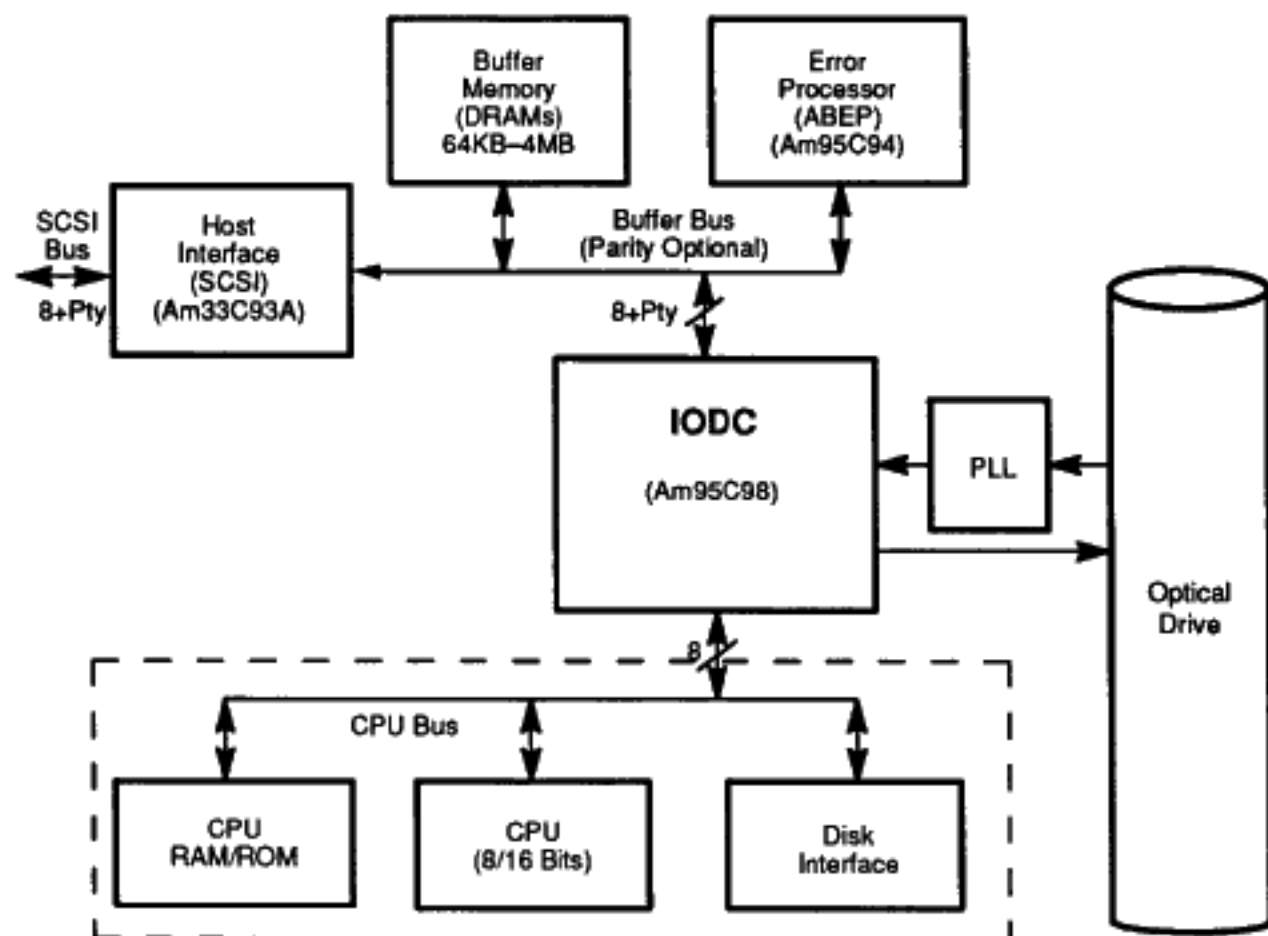
The Integrated Optical Disk Data Controller (IODC) is a highly programmable optical disk data format controller designed for use in ISO/ANSI X3B11 standard applications. The device has been optimized for applications utilizing an embedded SCSI disk data manager, but it easily supports other intelligent proprietary interfaces as well.

As an embedded controller, the IODC translates data between the RLL and NRZ domains, and monitors the special marks or patterns specified by the X3B11 standard. IODC can tolerate or recover from situations involving media defects. It also handles the timing of all disk read/write control signals, the transfer of data between the disk and buffer RAM, and the transfer of data between a parallel host interface and buffer RAM. The IODC performs all buffer management and arbitration associated with this transfer of data while maintaining data integrity by using a dedicated interface to AMD's Am95C94 an external, high-performance Advanced Burst Error Processor (ABEP). In addition, the IODC can perform advanced data mapping operations during data transfer, simplifying the task of cache management. The IODC can handle up to 4 MB of data buffer Dynamic RAM directly, including address multiplexing and refresh, with no external logic.

The IODC acts as an intelligent peripheral to a microprocessor or microcontroller. In an embedded SCSI disk controller application, the control CPU (referred to in this document as simply the *CPU*), interprets all SCSI commands and controls disk head positioning and head selection, while the IODC handles all data transfers. The CPU sets up and initiates IODC operation by modifying as few as six IODC registers. IODC registers are directly addressable, and can be read or written directly with either an iAPX-multiplexed address/data bus, or a Motorola 68xxx-type non-multiplexed bus interface.

A dedicated interface to an external error processor permits the IODC to cope with the high error rates associated with optical media. Through this interface, the IODC, in combination with the ABEP chip can correct an error in as little as 10 μ s. The ABEP supports 5- or 10-way interleaving with optional overlay CRC capability. The ABEP can correct up to 80 errors in a single sector in less than a millisecond. With this error-correction capability, the IODC and ABEP can perform on-the-fly error correction without missing a sector. In spiral formatted media, this avoids the need for the head to seek back in order to access a missed sector.

SYSTEM DIAGRAM

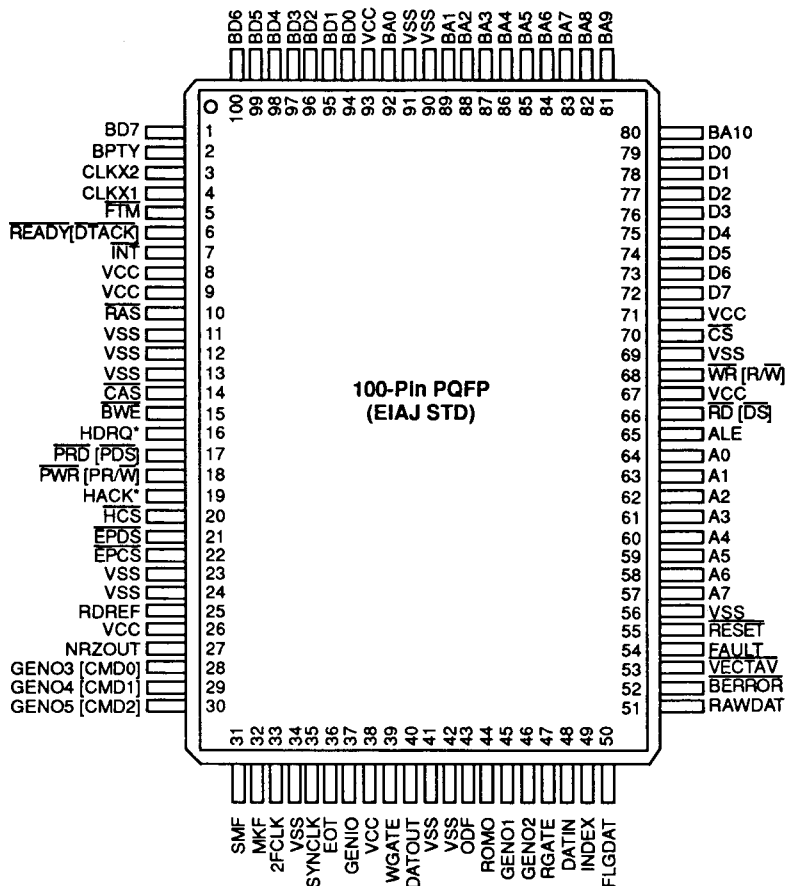


15940B-001C

RELATED AMD PRODUCTS

Part Number	Description
Am33C93A	SCSI Controller
Am53C80	SCSI Controller
Am53C94	SCSI Controller
Am53C96	SCSI Controller
Am80188	Microprocessor
Am80C188	Microprocessor
Am80C186	Microprocessor
Am80286	Microprocessor
Am80C286	Microprocessor
Am95C94	Advanced Burst Error Processor
Am95C96	Optical Disk Controller

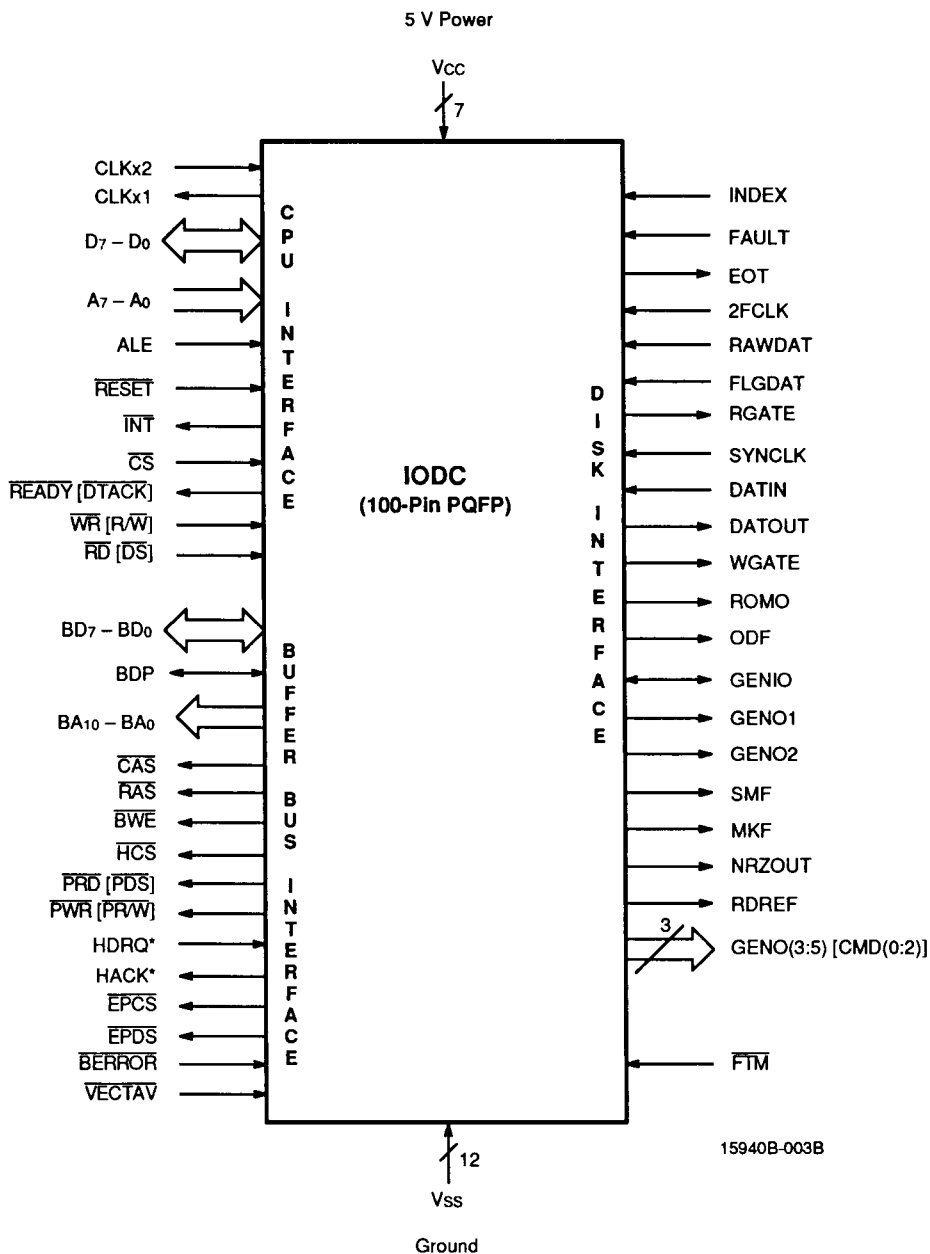
CONNECTION DIAGRAM



*These pins have programmable polarity.

15940B-002B

LOGIC SYMBOL

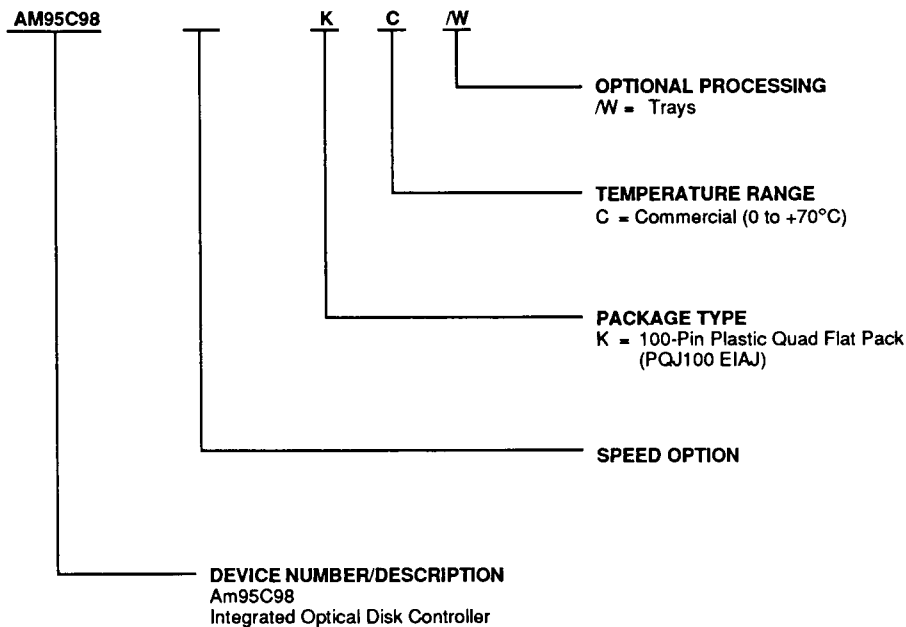


15940B-003B

*These pins have programmable polarity.

ORDERING INFORMATION**Standard Products**

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM95C98	KC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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