

MMBTA55LT1, MMBTA56LT1

MMBTA56LT1 is a Preferred Device

Driver Transistors

PNP Silicon

Features

- Pb-Free Package is Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage MMBTA55 MMBTA56	V_{CEO}	–60 –80	Vdc
Collector–Base Voltage MMBTA55 MMBTA56	V_{CBO}	–60 –80	Vdc
Emitter–Base Voltage	V_{EBO}	–4.0	Vdc
Collector Current – Continuous	I_C	–500	mAdc

THERMAL CHARACTERISTICS

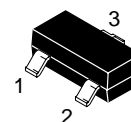
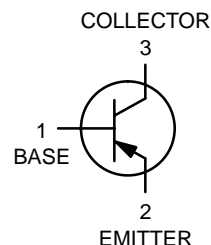
Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board (Note 1) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	$^\circ\text{C}$

- FR–5 = $1.0 \times 0.75 \times 0.062$ in.
- Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.



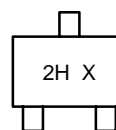
ON Semiconductor®

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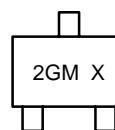


SOT–23
CASE 318
STYLE 6

MARKING DIAGRAMS



MMBTA55LT1



MMBTA56LT1

2H, 2GM = Specific Device Code
X = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
MMBTA55LT1	SOT–23	3000/Tape & Reel
MMBTA55LT3	SOT–23	10,000/Tape & Reel
MMBTA56LT1	SOT–23	3000/Tape & Reel
MMBTA56LT1G	SOT–23 (Pb–Free)	3000/Tape & Reel
MMBTA56LT3	SOT–23	10,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

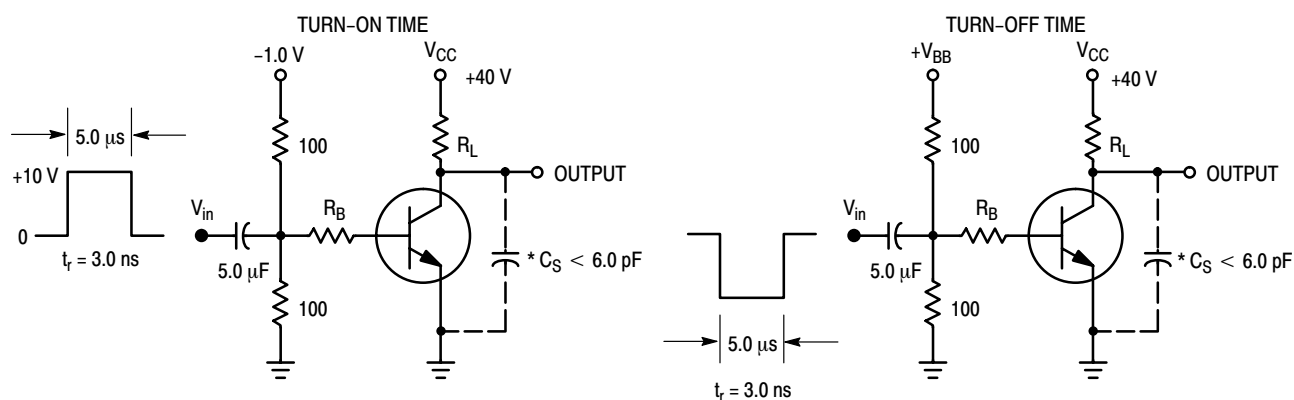
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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (Note 3) ($I_C = -1.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	-60 -80	– –	Vdc
Emitter–Base Breakdown Voltage ($I_E = -100\text{ }\mu\text{A}$, $I_C = 0$)	$V_{(BR)EBO}$	-4.0	–	Vdc
Collector Cutoff Current ($V_{CE} = -60\text{ Vdc}$, $I_B = 0$)	I_{CES}	–	-0.1	μA dc
Collector Cutoff Current ($V_{CB} = -60\text{ Vdc}$, $I_E = 0$) ($V_{CB} = -80\text{ Vdc}$, $I_E = 0$)	I_{CBO}	– –	-0.1 -0.1	μA dc
ON CHARACTERISTICS				
DC Current Gain ($I_C = -10\text{ mA}$, $V_{CE} = -1.0\text{ Vdc}$) ($I_C = -100\text{ mA}$, $V_{CE} = -1.0\text{ Vdc}$)	h_{FE}	100 100	– –	–
Collector–Emitter Saturation Voltage ($I_C = -100\text{ mA}$, $I_B = -10\text{ mA}$)	$V_{CE(sat)}$	–	-0.25	Vdc
Base–Emitter On Voltage ($I_C = -100\text{ mA}$, $V_{CE} = -1.0\text{ Vdc}$)	$V_{BE(on)}$	–	-1.2	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Current–Gain – Bandwidth Product (Note 4) ($I_C = -100\text{ mA}$, $V_{CE} = -1.0\text{ Vdc}$, $f = 100\text{ MHz}$)	f_T	50	–	MHz

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

4. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.



*Total Shunt Capacitance of Test Jig and Connectors
For PNP Test Circuits, Reverse All Voltage Polarities

Figure 1. Switching Time Test Circuits

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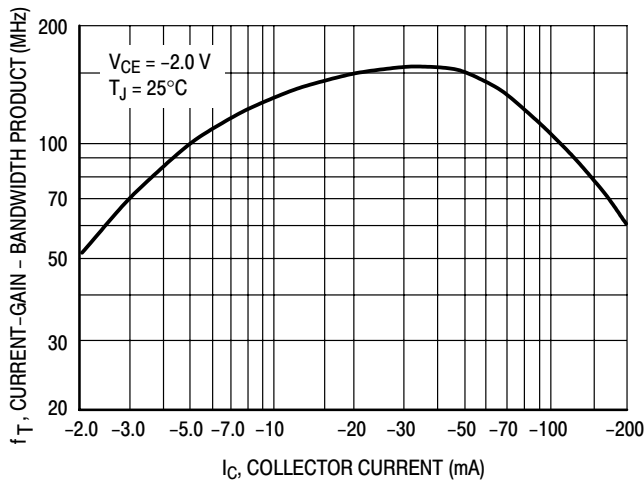


Figure 2. Current-Gain — Bandwidth Product

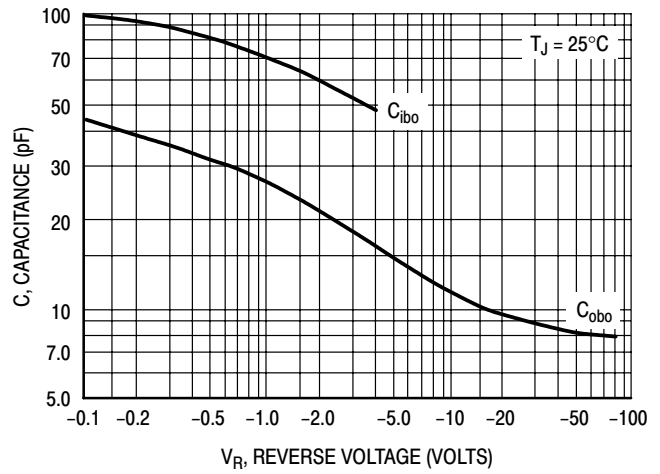


Figure 3. Capacitance

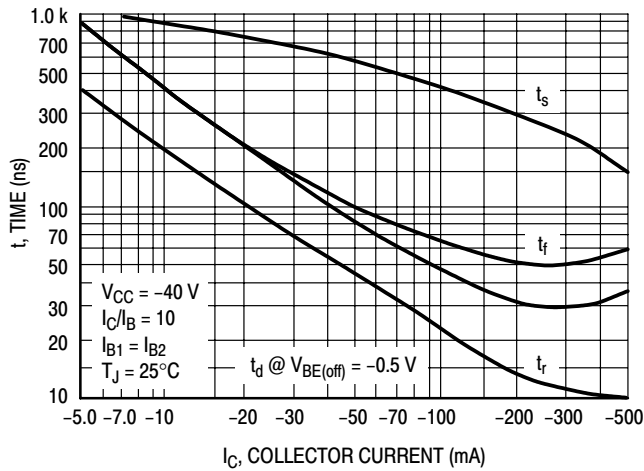


Figure 4. Switching Time

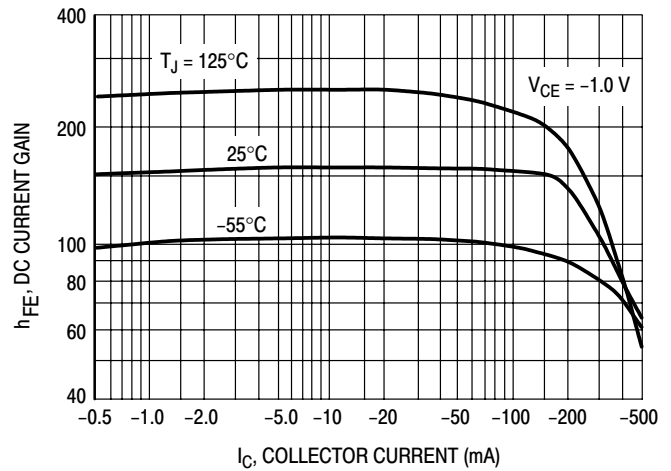


Figure 5. DC Current Gain

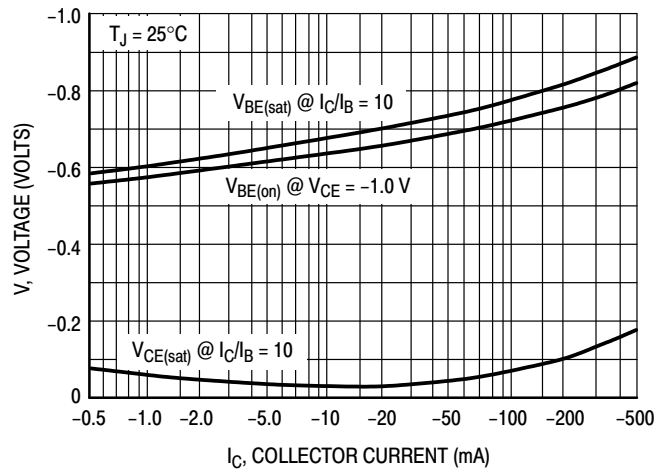


Figure 6. "ON" Voltages

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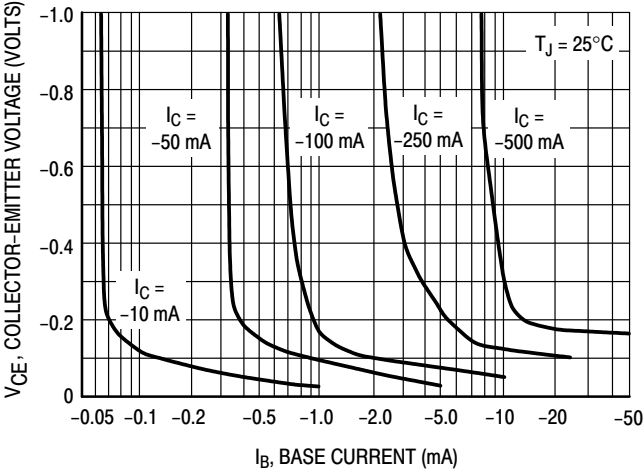


Figure 7. Collector Saturation Region

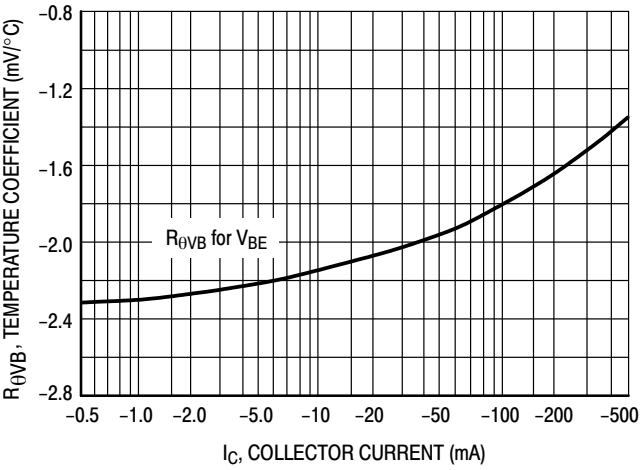


Figure 8. Base-Emitter Temperature Coefficient

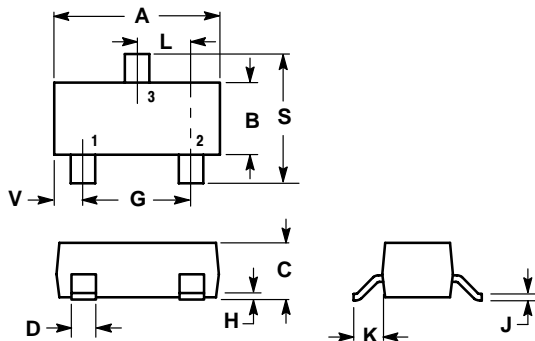
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PACKAGE DIMENSIONS

SOT-23 (TO-236)

CASE 318-08

ISSUE AH



NOTES:

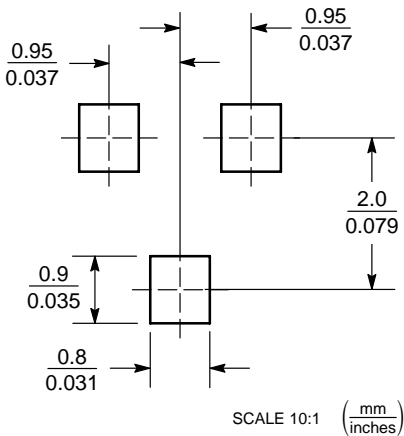
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-03 AND -07 OBSOLETE, NEW STANDARD 318-08.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:

- PIN 1. BASE
- EMITTER
- COLLECTOR

SOLDERING FOOTPRINT*



SOT-23

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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