

# Load Share Controller

## FEATURES

- Fully Differential High Impedance Voltage Sensing
- Accurate Current Amplifier for Precise Current Sharing
- Opto Coupler Driving Capability
- 1.25% Trimmed Reference
- Master Status Indication
- 4.5V TO 35V Operation

## DESCRIPTION

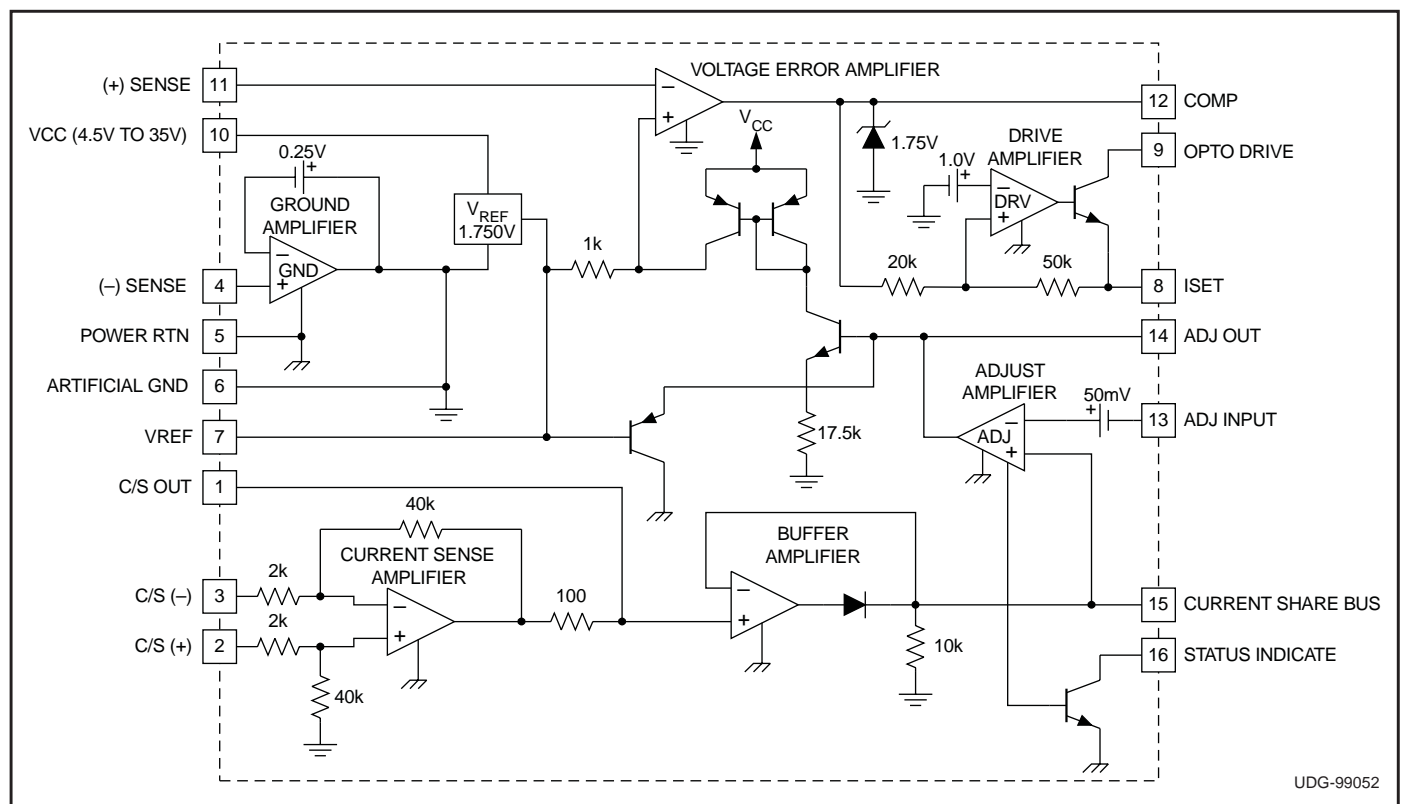
The UC3907 family of Load Share Controller ICs provides all the necessary features to allow multiple independent power modules to be paralleled such that each module supplies only its proportionate share to total load current.

This sharing is accomplished by controlling each module's power stage with a command generated from a voltage feedback amplifier whose reference can be independently adjusted in response to a common share bus voltage. By monitoring the current from each module, the current share bus circuitry determines which paralleled module would normally have the highest output current and, with the designation of this unit as the master, adjusts all the other modules to increase their output current to within 2.5% of that of the master.

The current share bus signal interconnecting all the paralleled modules is a low-impedance, noise-insensitive line which will not interfere with allowing each module to act independently should the bus become open or shorted to ground. The UC3907 controller will reside on the output side of each power module and its overall function is to supply a voltage feedback loop. The specific architecture of the power stage is unimportant. Either switching or linear designs may be utilized and the control signal may be either directly coupled or isolated though the use of an opto coupler or other isolated medium.

Other features of the UC3907 include 1.25% accurate reference: a low-loss, fixed gain current sense amplifier, a fully differential, high-impedance voltage sensing capability, and a status indicator to designate which module is performing as master.

## BLOCK DIAGRAM

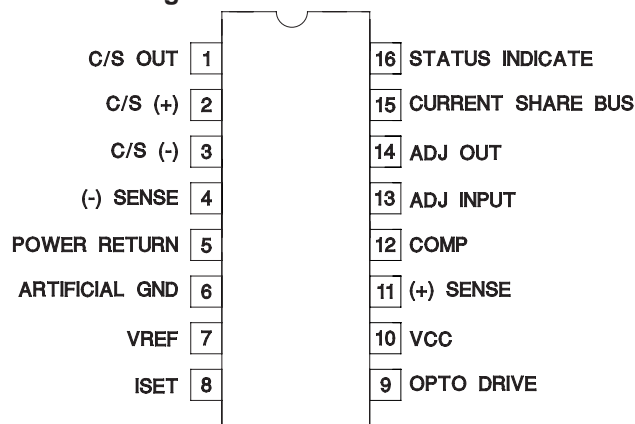


## ABSOLUTE MAXIMUM RATINGS

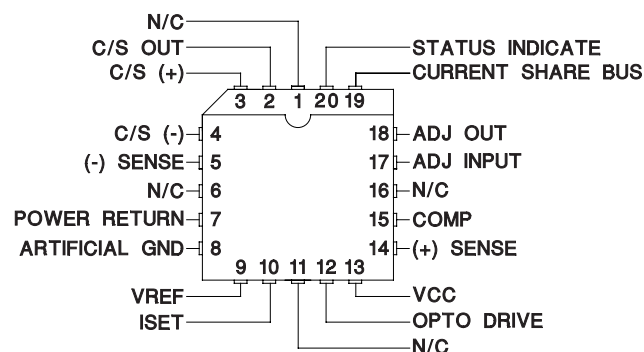
Supply Voltage ..... +35V  
 Opto Out Voltage ..... +35V  
 Opto Out Current ..... +20mA  
 Status Indicate Sink Current ..... +20mA  
 C/S Input Voltage ..... +35V  
 Share Bus Voltage ..... - 0.3V to +35V  
 Other Analog Inputs and Outputs (Zener clamped)  
   Maximum Forced Voltage ..... - 0.3V to +10V  
   Maximum Forced Current .....  $\pm 10$ mA  
 Ground Amp Sink Current ..... +50mA  
 Pins 1, 9, 12, 15 Sink Current ..... +20mA  
 Storage Temperature Range ..... - 65°C to +150°C  
 Junction Temperature ..... - 55°C to +150°C  
 Lead Temperature (Solder 10 Seconds) ..... +300°C  
*Pin Nos. refer to 16 Pin DIL Package*  
*Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.*

## CONNECTION DIAGRAMS

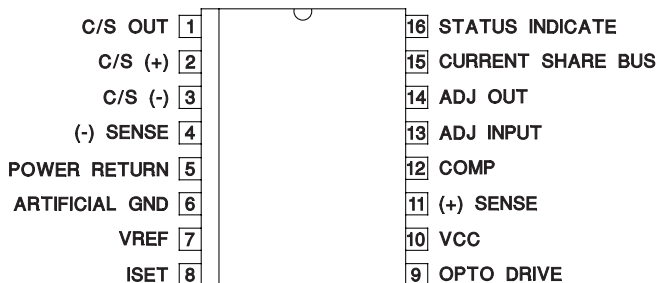
**DIL-16 (Top View)**  
**J or N Package**



**PLCC-20, LCC-20 (Top View)**  
**Q PACKAGE, L PACKAGE**



**SOIC-16 (Top View)**  
**DW Package**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for UC1907;  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for UC2907; and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for UC3907;  $V_{IN} = 15\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Voltage Amp Section</b>					
Input Voltage	COMP = 1V, $T_A = 25^\circ\text{C}$	1.975	2.000	2.025	V
	COMP = 1V, Over Temp	1.960	2.000	2.040	V
Line Regulation	$V_{IN} = 4.5\text{V}$ to 35V			15	mV
Load Regulation	$I_L$ Reference = 0.0mA to - 10mA			10	mV
Long Term Stability	$T_A = 125^\circ\text{C}$ , 1000hrs (Note 2)		5	25	mV
Total Output Variation	Line, Load, Temp	1.960		2.040	
Input Adjust Range	ADJ OUT from max high to max low	85	100	115	mV
Input Bias Current		-1			$\mu\text{A}$
Open Loop Gain	COMP = 0.75V to 1.5V	65			dB
Unity Gain Bandwidth	$T_A = 25^\circ\text{C}$ (Note 2)	700			kHz
Output Sink Current	(+) SENSE = 2.2V, COMP = 1V	6	15		mA
Output Source Current	(+) SENSE = 1.8V, COMP = 1V	400	600		$\mu\text{A}$
$V_{OUT}$ High	(+) SENSE = 1.8V, $I_L = - 400\mu\text{A}$	1.85	2		V
$V_{OUT}$ Low	(+) SENSE = 2.2V, $I_L = +1\text{mA}$		0.15	0.40	V

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference Section</b>					
Output Voltage	$T_A = 25^{\circ}\text{C}$	1.970	2.000	2.030	V
	Over Operating Temp	1.955	2.000	2.045	V
Short Circuit Current	$V_{REF} = 0.0\text{V}$	- 15	- 30	- 60	mA
<b>Ground Amp Section</b>					
Output Voltage		200	250	300	mV
Common Mode Variation	(-) SENSE from 0.0V to 2V			5	mV
Load Regulation	$I_L = 0.0\text{mA}$ to $20\text{mA}$ , $T_A = 25^{\circ}\text{C}$			10	mV
	$I_L = 0.0\text{mA}$ to $20\text{mA}$ , Over Temp			15	mV
<b>Adjust Amp Section</b>					
Input Offset Voltage	ADJ OUT = 1.5V, $V_{cm} = 0.0\text{V}$	40	50	60	mV
Input Bias Current		- 2			$\mu\text{A}$
Open Loop Gain	$1.5\text{V} \leq \text{ADJ OUT} \leq 2.25\text{V}$	65			dB
Unity Gain Bandwidth	$T_A = 25^{\circ}\text{C}$ , $C_{OUT} = 1\mu\text{F}$ (Note 2)		500		Hz
Transconductance	$I_{OUT} = -10\mu\text{A}$ to $+10\mu\text{A}$ , $V_{OUT} = 1.5\text{V}$	1.7	3	4.5	ms
Output Sink Current	$V_{id} = 0.0\text{V}$ , ADJ OUT = 1.5V	55	135	225	$\mu\text{A}$
Output Source Current	$V_{id} = 250\text{mV}$ , ADJ OUT = 1.5V	110	200	350	$\mu\text{A}$
$V_{OUT}$ High	$V_{id} = 250\text{mV}$ , $I_{OUT} = -50\mu\text{A}$	2.20	2.70	2.90	V
$V_{OUT}$ Low	$V_{id} = 0.0\text{V}$ , $I_{OUT} = 50\mu\text{A}$		0.75	1.15	V
Common Mode Rejection Ratio	$V_{cm} = 0.0$ to $10\text{V}$	70			dB
Output Gain to V/A	$V_{OUT}$ ADJ OUT = 1.5V to 2V	50	57	64	mV/V
	$\Delta(+)$ SENSE/ $\Delta$ ADJ OUT				
<b>Current Amp Section</b>					
Gain	$V_{cm} = 0.0\text{V}$ , $V_{id} = 50\text{mV}$ to $100\text{mV}$	19.2	19.6	20.1	V/V
Output Voltage	$V_{c/s (+)} = V_{c/s (-)} = 0.0\text{V}$ , $T_A = 25^{\circ}\text{C}$	210	250	290	mV
	$V_{c/s (+)} = V_{c/s (-)} = 0.0\text{V}$ , Over Temp	180	250	330	mV
Input Offset Change with Common Mode Input	$V_{cm} = 0\text{V}$ to $13\text{V}$			600	$\mu\text{V/V}$
$V_{OUT}$ High	$V_{id} = 1\text{V}$	10	14.5		V
$V_{OUT}$ Low	$V_{id} = -1\text{V}$ , $I_L = 1\text{mA}$		350	450	mV
Power Supply Rejection Ratio	$V_{IN} = 4.5\text{V}$ to $35\text{V}$ , $V_{cm} = 0.0\text{V}$	60			dB
Slew Rate			0.4		V/ $\mu\text{s}$
<b>Drive Amp Section Rset = 500<math>\Omega</math> to Artificial Gnd, Opto Drive = 15V</b>					
Voltage Gain	COMP = 0.5V to 1V	2.3	2.5	2.6	V/V
ISET $V_{OUT}$ High	(+) SENSE = 2.2V	3.8	4.1	4.4	V
ISET $V_{OUT}$ Low	(+) SENSE = 1.8V		270	300	mV
Opto out Voltage Range		4		35	V
Zero Current Input Threshold		1.55	1.65	1.75	V
<b>Buffer Amp Section</b>					
Input Offset Voltage	Input = 1V			5	mV
Output Off Impedance	Input = 1V, Output = 1.5V to 2V	5	10	20	k $\Omega$
Output Source Current	Input = 1V, Output = 0.5V	6	15		mA
Common Mode Rejection Ratio	$V_{cm} = 0.3\text{V}$ to $10\text{V}$	70			dB
Power Supply Rejection Ratio	$V_{IN} = 4.5\text{V}$ to $35\text{V}$	70			dB

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Under Voltage Lockout Section</b>					
Startup Threshold			3.7	4.4	V
Threshold Hysteresis			20		mV
<b>Status Indicate Section</b>					
$V_{OUT}$ Low	ADJ OUT = Current Share Bus		0.2	0.5	V
Output Leakage	ADJ OUT = 1V, $V_{OUT} = 35\text{V}$		0.1	5	$\mu\text{A}$
<b>Total Stand by Current Section</b>					
Startup Current	$V_{IN} = UVLO - 0.2\text{V}$		3	5	mA
Operating Current	$V_{IN} = 35\text{V}$		6	10	mA

Note 1: Unless otherwise specified all voltages are with respect to (–) SENSE. Currents are positive into, negative out of the specified terminal.

Note 2: Guaranteed by design. Not 100% tested in production.

## PIN/BLOCK DESCRIPTIONS

**(–) SENSE** (Pin 4) - This is a high-impedance pin intended to allow remote sensing of the system ground, bypassing any voltage drops which might appear in the power return line. **This point should be considered as the “true” ground. Unless otherwise stated, all voltages are with respect to this point.**

**ARTIFICIAL GROUND** (Pin 6) - This is a low impedance circuit ground which is exactly 250 millivolts above the (–) SENSE terminal. This offset allows the Ground Buffer Amplifier negative headroom to return all the control bias and operating currents while maintaining a high impedance at the (–) SENSE input.

**POWER RTN** (Pin 5) - This should be the most negative voltage available and can range from zero to 5V below the (–) SENSE terminal. It should be connected as close to the power source as possible so that voltage drops across the return line and current sensing impedances lie between this terminal and the (–) SENSE point.

**VREF** (Pin 7) - The internal Voltage Reference is a band-gap circuit set at 2.0 Volts with respect to the (–) SENSE input (1.75V above the ARTIFICIAL GROUND), and an accuracy of  $\pm 1.5\%$ . This circuit, as well as all the other chip functions, will work over a supply voltage range of 4.5V to 35V allowing operation from unregulated DC, an auxiliary voltage, or the same output voltage that it is controlling. Under voltage lockout has been included to insure proper startup by disabling internal bias currents until the reference rises into regulation.

**VOLTAGE AMPLIFIER** (Pins 11, 12) - This circuit is the feedback control gain stage for the power module's output voltage regulation, and overall loop compensation will normally be applied around this amplifier. Its output will swing from slightly above the ground return to an internal

clamp of 2.0 Volts. The reference trimming is performed closed loop, and measured at pin 11, (+) SENSE. The value is trimmed to  $2\text{V} \pm 1.25\%$ .

**DRIVE AMPLIFIER** (Pins 8, 9, 12) - This amplifier is used as an inverting buffer between the Voltage Amplifier's output and the medium used to couple the feedback signal to the power controller. It has a fixed voltage gain of 2.5 and is usually configured with a current-setting resistor to ground. This establishes a current - sinking output optimized to drive optical couplers biased at any voltage from 4.5V to 35V, with current levels up to 20mA. The polarity of this stage is such that an increasing voltage at the Voltage Amplifier's sense input (as, for example, at turn on) will increase the opto's current. In a nonisolated application, a voltage signal ranging from 0.25V to 4.1V may be taken from the current-setting output but it should be noted that this voltage will also increase with increasing sense voltage and an external inverter may be required to obtain the correct feedback polarity.

**CURRENT AMPLIFIER** (Pins 1, 2, 3) - This amplifier has differential sensing capability for use with an external shunt in the power return line. The common-mode range of its input will accommodate the full range between the Power Return point and  $V_{CC}-2\text{V}$  which will allow undefined line impedances on either side of the current shunt. The gain is internally set at 20 giving the user the ability to establish the maximum voltage drop across the current sense resistor at any value between 50 and 500 millivolts. While the bandwidth of this amplifier may be reduced with the addition of an external output capacitor to ground, in most cases this is not required as the compensation of the Adjust Amplifier will typically form the dominant pole in the adjust loop.



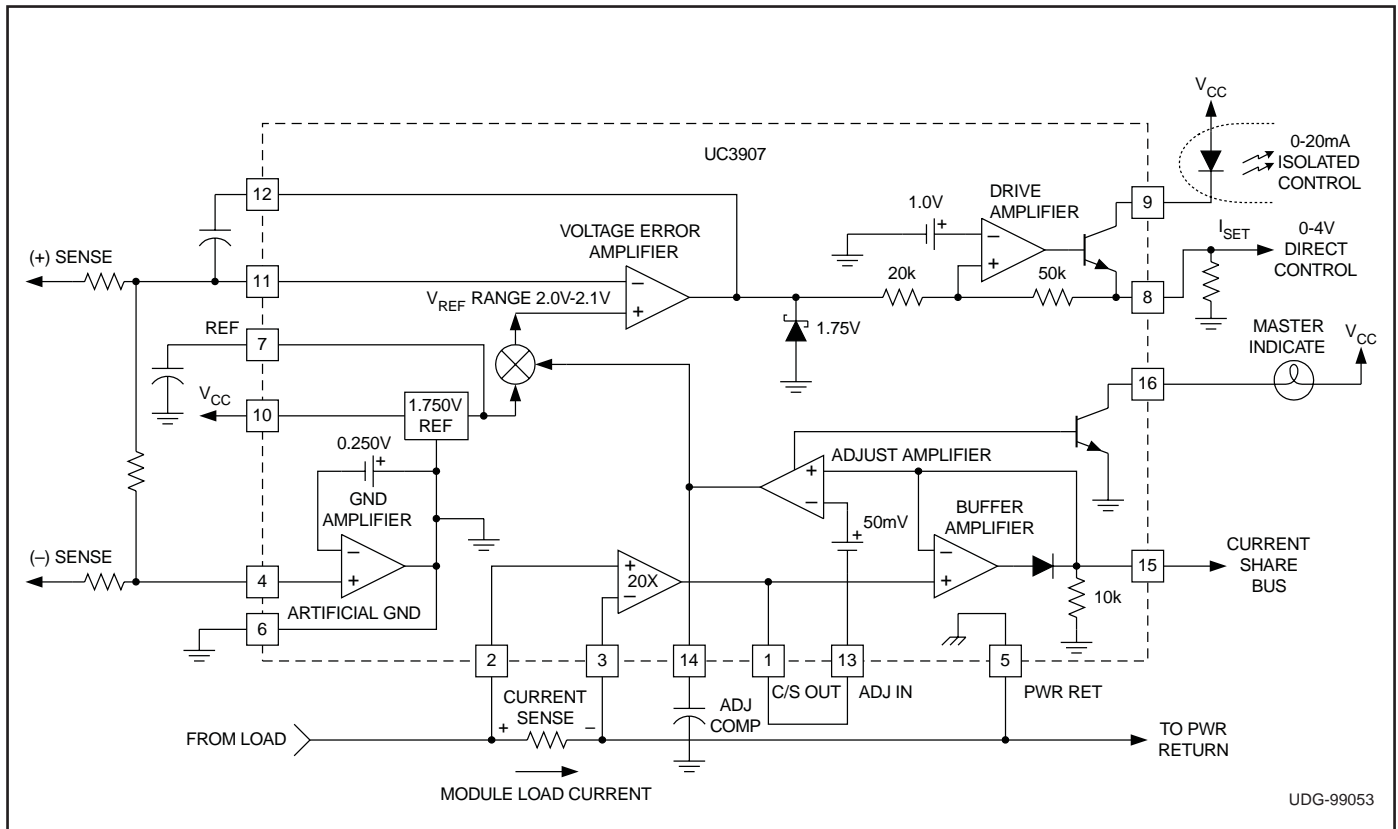


Figure 2. Load share connection diagram.

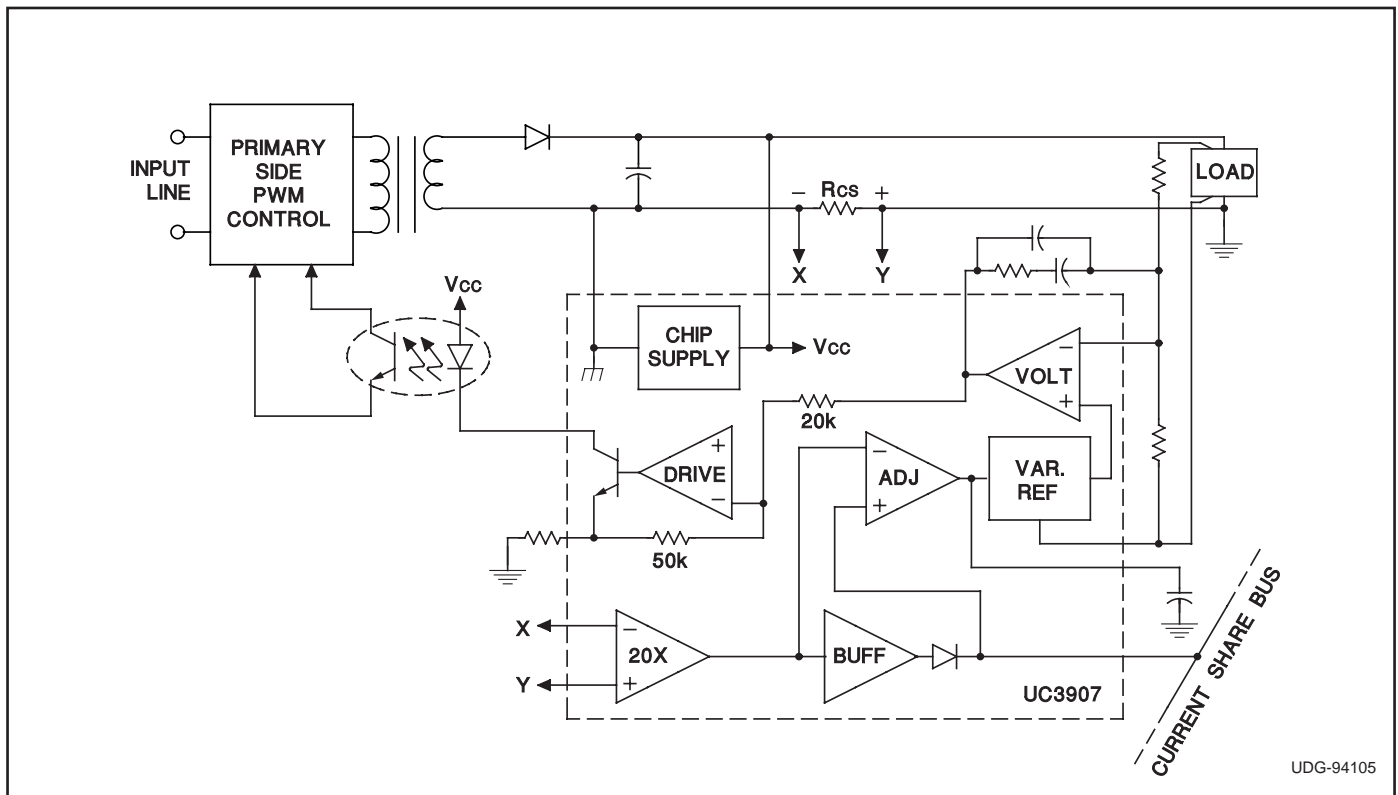


Figure 3. UC3907 In a load-sharing feedback loop for an off-line isolated supply.

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