- **3-Channel CMOS ADC**
- **5-V Single-Supply Operation or 5-V Analog Supply with Digital Supply from 2.7 V to 5.25 V**
- **8-Bit Resolution**
- **Differential Linearity Error . . . ±0.5 LSB Max**
- **Linearity Error . . . ±0.75 LSB Max**
- **Maximum Conversion Rate**
  20 Megasamples per Second (MSPS) Min
- **Analog Input Voltage Range**
  2 $V_{I(PP)}$ Min
- **64-Pin Shrink QFP Package**
- **Analog Input Bandwidth . . . >14 MHz**
- **Suitable for YUV or RGB Applications**
- **Digital Clamp Optimized for NTSC or PAL YUV Component**
- **High-Precision Clamp . . . ±1 LSB**
- **Automatic Clamp Pulse Generator**
- **Output-Data Format Multiplexer**
- **Low Power Consumption**

description

The TLC5733A is a 3-channel 8-bit semiflash analog-to-digital converter (ADC) that operates from a single 5-V power supply. It converts a wide-band analog signal (such as a video signal) to digital data at sampling rates up to 20 MSPS minimum. The TLC5733A contains a feed-back type high-precision clamp circuit for each ADC channel for video (YUV) applications and a clamp pulse generator that detects COMPOSITE SYNC† pulses automatically. A clamp pulse can also be supplied externally. The output-data format multiplexer selects a ratio of Y:U:V of 4:4:4, 4:1:1, or 4:2:2. For RGB applications, the 4:4:4 output format without clamp function can be used. The TLC5733A is characterized for operation from –20°C to 75°C.

AVAILABLE OPTIONS

T_A	PACKAGE
	QUAD FLATPACK
–20°C to 75°C	TLC5733AIPM

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† COMPOSITE SYNC refers to the externally generated synchronizing signal that is a combination of vertical and horizontal sync information used in display and TV systems.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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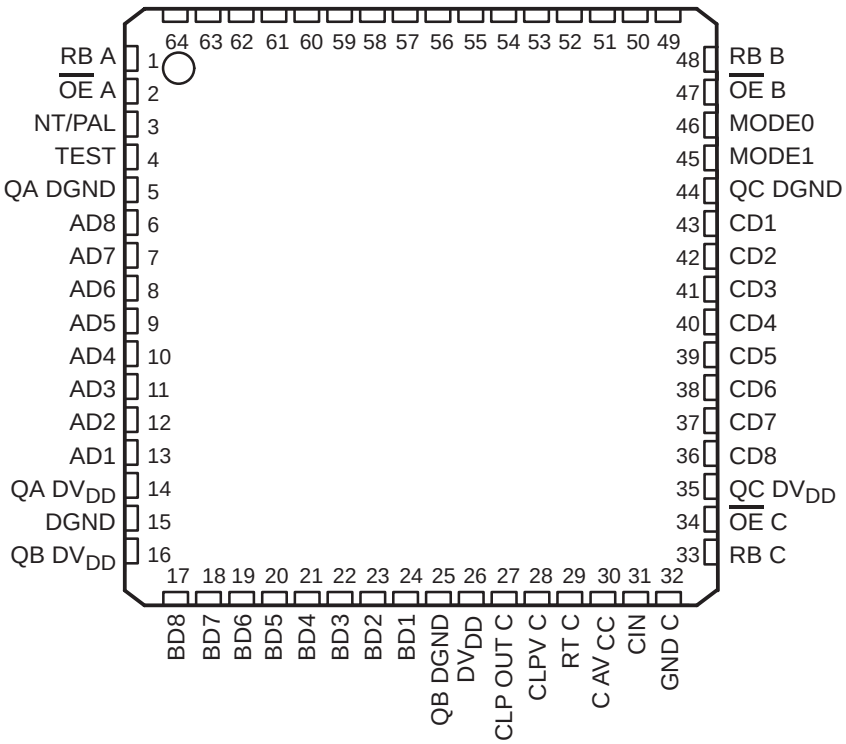
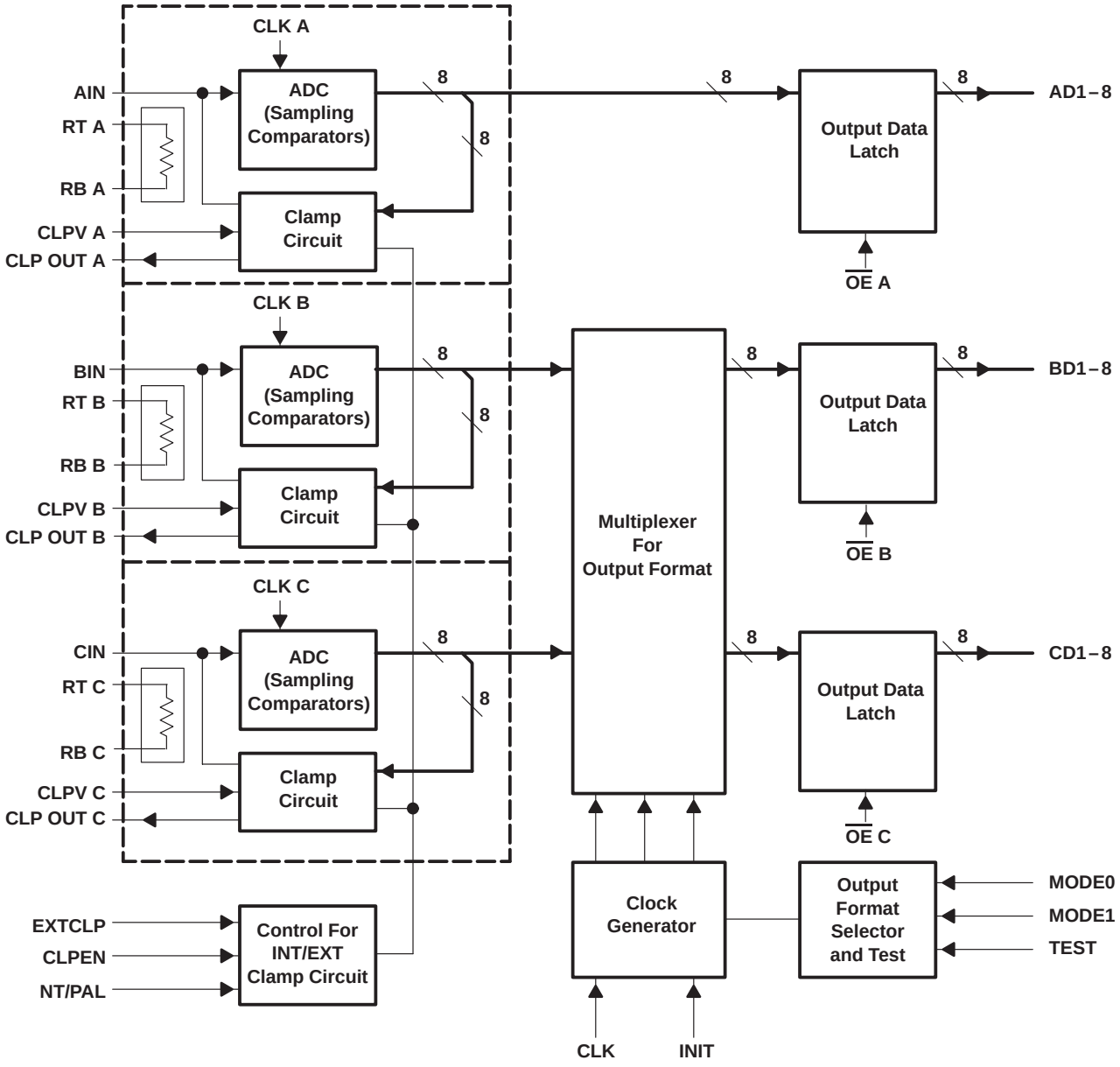
PM PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A AV_{CC}	62	I	Analog supply voltage of ADC A
AD8–AD1	6–13	O	Data output of ADC A (LSB: AD1, MSB:AD8)
AIN	63	I	Analog input of ADC A
B AV_{CC}	51	I	Analog supply voltage of ADC B
BD8–BD1	17–24	O	Data output of ADC B (LSB: BD1, MSB:BD8)
BIN	50	I	Analog input of ADC B
C AV_{CC}	30	I	Analog supply voltage of ADC C
CD8–CD1	36–43	O	Data output of ADC C (LSB:CD1, MSB: CD8) When MODE0 = L, MODE1 = L, CD8 outputs MSB flag of BD8–BD5 When MODE0 = L, MODE1 = L, CD7 outputs MSB flag of BD8–BD5 When MODE0 = L, MODE1 = H, CD8 outputs B channel flag of CD8–BD1 When MODE0 = L, MODE1 = H, CD8 outputs B channel flag of CD8–BD1
CIN	31	I	Analog input of ADC C
CLK	56	I	Clock input. The clock frequency is normally 4 × the frequency subcarrier (fsc) for most video systems (see Table 3). The nominal clock frequency is 14.31818 MHz for National Television System Committee (NTSC) and 17.745 MHz for phase alteration line (PAL).
CLPEN	57	I	Clamp enable. When using an internal clamp pulse, CLPEN should be high. When using an external clamp pulse, CLPEN should be low.
CLP OUT A	59	O	Clamping bias current of ADC A. A resistor-capacitor combination that sets the clamp timing.
CLP OUT B	54	O	Clamping bias current of ADC B. A resistor-capacitor combination that sets the clamp timing.
CLP OUT C	27	O	Clamping bias current of ADC C. A resistor-capacitor combination that sets the clamp timing.
CLPV A	60	O	Clamping level of ADC A. A capacitor is connected to CLPV A to set the clamp timing. The clamp level at CLPV A is connected to an output code of 16 (0010000).
CLPV B	53	O	Clamping level of ADC B. A capacitor is connected to CLPV B to set the clamp timing. The clamp level at CLPV B is connected to an output code of 128 (1000000).
CLPV C	28	O	Clamping level of ADC C. A capacitor is connected to CLPV C to set the clamp timing. The clamp level at CLPV C is connected to an output code of 128 (1000000).
DGND	15	I	Digital ground
DV_{DD}	26	I	Digital supply voltage
EXTCLP	55	I	External clamp pulse input. When EXTCLP and CLPEN are low, the internal clamp circuit cannot be used. The external clamp pulse when used is active high.
GND A	64	I	Ground of ADC A
GND B	49	I	Ground of ADC B
GND C	32	I	Ground of ADC C
INIT	58	I	Output initialized. The output data is synchronous when INIT is taken high from low. INIT is a control terminal that allows the external system to initialize the TLC5733A data conversion cycle. INIT is usually used at power up or system reset.
MODE0	46	I	Output format mode selector 0. When MODE1 is low and MODE0 is low, output data format1 is selected. When MODE1 is low and MODE0 is high, output data format2 is selected. When MODE1 is high and MODE0 is low, output data format3 is selected. A high level on MODE1 and a high level on MODE0 is not used.
MODE1	45	I	Output format mode selector 1. When MODE1 is low and MODE0 is low, output data format1 is selected. When MODE1 is low and MODE0 is high, output data format2 is selected. When MODE1 is high and MODE0 is low, output data format3 is selected. A high level on MODE1 and a high level on MODE0 is not used.
NT/PAL	3	I	NTSC/PAL control. NTSC/PAL should be low for NTSC and high for PAL.
$\overline{OE}$ A	2	I	Output enable A. $\overline{OE}$ A enables the output of ADC A.
$\overline{OE}$ B	47	I	Output enable B. $\overline{OE}$ B enables the output of ADC B.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{OE}$ C	34	I	Output enable C. $\overline{OE}$ C enables the output of ADC C.
QA DGND	5	I	Digital ground for output of ADC A
QA DV_{DD}	14	I	Digital supply voltage for output of ADC A
QB DGND	25	I	Digital ground for output of ADC B
QB DV_{DD}	16	I	Digital supply voltage for output of ADC B
QC DGND	44	I	Digital ground for output of ADC C
QC DV_{DD}	35	I	Digital supply voltage for output of ADC C
RB A	1	I	Bottom reference voltage of ADC A. The nominal externally applied dc voltage between RT A and RB A is 2 V for video signals.
RB B	48	I	Bottom reference voltage of ADC B. The nominal externally applied dc voltage between RT B and RB B is 2 V for video signals.
RB C	33	I	Bottom reference voltage of ADC C. The nominal externally applied dc voltage between RT C and RB C is 2 V for video signals.
RT A	61	I	Top reference voltage of ADC A. The nominal externally applied dc voltage between RT A and RB A is 2 V for video signals.
RT B	52	I	Top reference voltage of ADC B. The nominal externally applied dc voltage between RT B and RB B is 2 V for video signals.
RT C	29		Top reference voltage of ADC C. The nominal externally applied dc voltage between RT C and RB C is 2 V for video signals.
TEST	4	I	Test. TEST should be tied low when using this device.

absolute maximum ratings†

Supply voltage, V_{CC}, V_{DD} . . . . . 7 V
Reference voltage input range, $V_{ref(RT\ A)}$, $V_{ref(RT\ B)}$, $V_{ref(RT\ C)}$, $V_{ref(RB\ A)}$, $V_{ref(RB\ B)}$, $V_{ref(RB\ C)}$ . . . . . AGND to V_{CC}
Analog input voltage range . . . . . AGND to V_{CC}
Digital input voltage range, V_I . . . . . DGND to V_{DD}
Digital output voltage range, V_O . . . . . DGND to V_{DD}
Operating free-air temperature range, T_A . . . . . –20°C to 75°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage‡	V_{CC} – AGND	4.75	5	5.25	V
	V_{DD} – DGND	2.7	5	5.25	
	AGND – DGND	–100	0	100	mV
Reference input voltage, $V_{ref(RT\ A)}$, $V_{ref(RT\ B)}$, $V_{ref(RT\ C)}$		$V_{ref(RB)}$+2		V_{CC}	V
Reference input voltage, $V_{ref(RB\ A)}$, $V_{ref(RB\ B)}$, $V_{ref(RB\ C)}$		0		$V_{ref(RT)}$–2	V
Analog input voltage, V_I		0		$V_{ref(RT)}$	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level pulse duration, $t_{w(H)}$		25			ns
Low-level pulse duration, $t_{w(L)}$		25			ns
Setup time for INIT input, t_{su1}		5			ns
Operating free-air temperature range, T_A		–20		75	°C

‡ Within the electrical and operating characteristics table, when the term V_{DD} is used, all XDV_{DD} terminals are tied together, and when the term V_{CC} is used, all XAV_{CC} terminals are tied together.

electrical characteristics at V_{DD} = 2.7 V to 5.25 V, V_{CC} = 5 V, $V_{ref(RT)}$ = 2.5 V, $V_{ref(BB)}$ = 0.5 V, $f_{(CLK)}$ = 20 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Clamp level accuracy			±1		LSB
R_{ref}	Reference voltage resistor	Measured between RT and RB	160	220	350	Ω
C_i	Analog input capacitance	V_I = 1.5 V + 0.07 V_{rms}		16		pF
I_{IH}	High-level input current	V_{DD} = MAX†, V_{IH} = V_{DD}, V_{CC} = 5V			5	µA
I_{IL}	Low-level input current	V_{DD} = MAX†, V_{IL} = 0, V_{CC} = 5V			5	
V_{OH}	High-level output voltage	All DV_{DD} terminals = 2.7 V to 5.25 V, I_{OH} = –1 mA	DV_{DD} –0.7 V			V
V_{OL}	Low-level output voltage	All DV_{DD} terminals = 2.7 V to 5.25 V, I_{OL} = 2 mA			0.8	
$I_{OH(lkg)}$	High-level output leakage current	V_{DD} = MAX†, V_{OH} = V_{DD}, V_{CC} = 5V			16	µA
$I_{OL(lkg)}$	Low-level output leakage current	V_{DD} = MIN†, V_{OL} = 0, V_{CC} = 5V			16	
I_{CC}	Supply current	f_c = 20 MSPS, NTSC ramp wave input		50	75	mA

† Conditions marked MIN or MAX are as stated in recommended operating conditions.

operating characteristics at V_{DD} = 2.7 V to 5.25 V, V_{CC} = 5 V, $V_{ref(RT)}$ = 2.5 V, $V_{ref(RB)}$ = 0.5 V, $f_{(CLK)}$ = 20 MHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
E_{ZS}	Zero-scale error	V_{ref} = REFT – REFB = 2 V		–18	–43	–68	mV
E_{FS}	Full-scale error	V_{ref} = REFT – REFB = 2 V		–20	0	20	mV
E_L	Linearity error	$f_{(CLK)}$ = 20 MHz,	V_I = 0.5 V to 2.5 V		±0.4	±0.75	LSB
		$f_{(CLK)}$ = 20 MHz, T_A = –20°C to 75°C	V_I = 0.5 V to 2.5 V		±0.4	±1	
E_D	Linearity error, differential	$f_{(CLK)}$ = 20 MHz,	V_I = 0.5 V to 2.5 V		±0.3	±0.5	LSB
		$f_{(CLK)}$ = 20 MHz, T_A = –20°C to 75°C	V_I = 0.5 V to 2.5 V		±0.3	±0.75	
f_c	Maximum conversion rate	V_I = 0.5 V – 2.5 V,	f_I = 1-kHz ramp waveform	20			MSPS
BW	Analog input bandwidth	At – 1 dB			14		MHz
t_{pd}	Digital output delay time	C_L = 10 pF			18	30	ns
	Differential gain	NTSC 40 IRE‡ modulation wave,	f_c = 14.3 MSPS		1%		
	Differential phase	NTSC 40 IRE‡ modulation wave,	f_c = 14.3 MSPS		0.7		deg
	Aperture jitter time				30		ps
	Sampling delay time				4		ns

‡ Institute of Radio Engineers

detailed description

clamp function

The clamp function is optimized for a YUV video signal and has two clamp modes. The first mode uses the COMPOSITE SYNC signal as the input to the EXTCLP terminal to generate an internal clamp pulse and the second mode uses an externally generated clamp pulse as the input to the EXTCLP terminal.

In the first mode, the device detects false pulses in the COMPOSITE SYNC signal by monitoring the rising and falling edges of the COMPOSITE SYNC signal pulses. This monitoring prevents faulty operation caused by disturbances and missing pulses of the COMPOSITE SYNC signal input on EXTCLP and external spike noise. When fault pulses are detected, the device internally generates a train of clamp pulses at the proper positions (1H) by an internal 910-counter for NTSC and a 1136-counter for PAL. The device checks clamp pulses for 1H time and generates clamp pulses at correct positions when COMPOSITE SYNC pulses are in error in time.

The internal counter continually produces a horizontal sync period (1H) that is NTSC or PAL compatible as selected by the condition of the NT/PAL terminal.

clamp voltages and selection

Table 1 shows the clamping level during the clamp interval. Table 2 shows the selection of the internal or external clamp pulse. With either NTSC or PAL, the internal clamp pulse is always used.

Table 1. Clamp Level (Internal Connection Level)

CHANNEL OF ADC	OUTPUT CODE	APPLICATION
ADC A • $V_{I(A)}$	00010000	Y
ADC B • $V_{I(B)}$	10000000	(U, V)
ADC C • $V_{I(C)}$	10000000	(U, V)

Table 2. Clamp Level (Internal Connection Level)

CONDITION			FUNCTION (EACH ADC)	
CLPEN	EXTCLP	NT/PAL	INTERNAL CLAMP	CLAMP PULSE
L	⎍	Don't Care	Inactive	External clamp pulse
	L	Don't Care	Inactive	No clamping
H	COMPOSITE SYNC input	L	Active	Synchronous with NTSC
		H	Active	Synchronous with PAL

The clamp circuit is shown in Figure 6. The clamp voltage is stored on capacitor C2 during the back porch of the horizontal blanking period.

During the clamp pulse the input to channel A is clamped to:

$V_C(A) = (16/256) \times$ (voltage difference from terminal RT A to RB A)

$V_C(B) = (128/256) \times$ (voltage difference from terminal RT B to RB B)

$V_C(C) = (128/256) \times$ (voltage difference from terminal RT C to RB C)

COMPOSITE SYNC time monitoring

When CLPEN is high, COMPOSITE SYNC generates an internal clamp pulse on the horizontal blanking interval back porch. The TLC5733A has a timing window into which the horizontal sync tip must occur. There is a noise time window for the falling edge and one for the rising edge (see Figure 1, Figure 2, and Table 3).

correct COMPOSITE SYNC timing

The Noise Gate 1 signal provides the timing window for the COMPOSITE SYNC falling edge. After an interval A of 867 clocks for NTSC or 1075 for PAL from the last falling edge of COMPOSITE SYNC, Noise Gate 1 signal goes high for 43 clocks for NTSC or 61 clocks for PAL (interval B). The falling edge of the input signal to the EXTCLP terminal can occur at any time within this window to be a valid COMPOSITE SYNC falling edge.

The Noise Gate 2 signal provides the timing window for the COMPOSITE SYNC rising edge. On the falling edge of the horizontal sync tip, the internal logic generates Noise Gate 2 as a low signal for 58 clocks (interval C) for both NTSC and PAL and then returns to a high active state. At this time if the input to EXTCLP is still low, it is considered a valid COMPOSITE SYNC signal.

normal clamp pulse generation

On the rising edge of COMPOSITE SYNC, the internal logic generates an internal delay (interval D) and then generates the internal positive clamp pulse 54 clocks wide (interval F).

clamp operation with incorrect COMPOSITE SYNC timing

noise suppression

If the input to EXTCLP goes low prior to Noise Gate 1 going high (within 43 clocks for NTSC or 61 clocks for PAL of the normal 1H timing for the falling edge of COMPOSITE SYNC) then that input is not considered a valid COMPOSITE SYNC and is ignored.

If the input to EXTCLP is high when Noise Gate 2 goes to the high state, the input signal is considered noise and is ignored.

Therefore, the correct signal must be high for a maximum of 43 clocks for NTSC or 61 clocks for PAL, before the 1H timing, to be a valid sync signal. Also, the input to EXTCLP must be at least 58 clocks wide (interval C) to be valid.

This function of monitoring the timing eliminates spurious noise spikes from falsely synchronizing the system.

timing error of COMPOSITE SYNC

The internal counter resets to zero on the first falling edge of COMPOSITE SYNC. After that time, if there is a missing COMPOSITE SYNC signal, then the internal logic waits an interval of 76 clocks (interval E) for NTSC or 93 for PAL from the counter zero count and then generates an internal clamp pulse 54 clocks wide (interval F).

This function maintains the synchronization pattern when COMPOSITE SYNC is not present.

summary of device operation with COMPOSITE SYNC

This internal timing allows the TLC5733A to correctly position the clamp pulse when an external COMPOSITE SYNC input:

- Is delayed with respect to the horizontal sync period
- Is early with respect to the horizontal sync period
- Is nonexistent during the horizontal sync period
- Has falling edge noise spikes within the horizontal sync period

The device operation is summarized as follows for these improper external clamp conditions:

- Under all four conditions on EXTCLP, the internal clamp generation circuit generates a clamp pulse at the proper time after the horizontal sync period as shown in Figure 1.
- The TLC5733A internal clamp circuit generates an internal clamp pulse each 1H time for the entire time interval that the COMPOSITE SYNC input is missing.

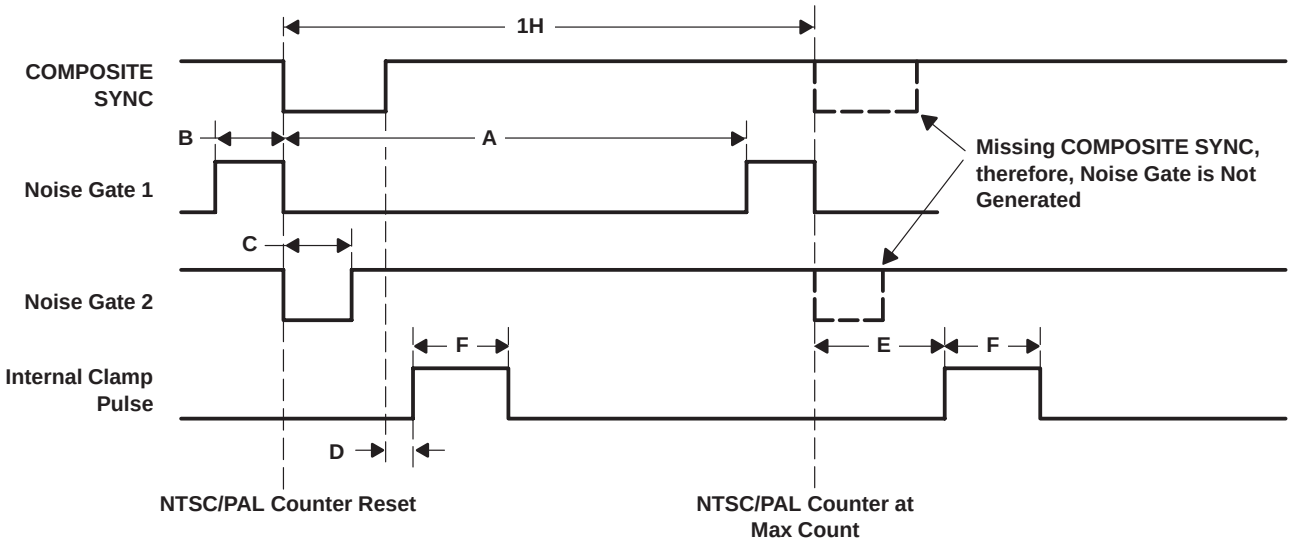


Figure 1. COMPOSITE SYNC and Internal Clamp Timing

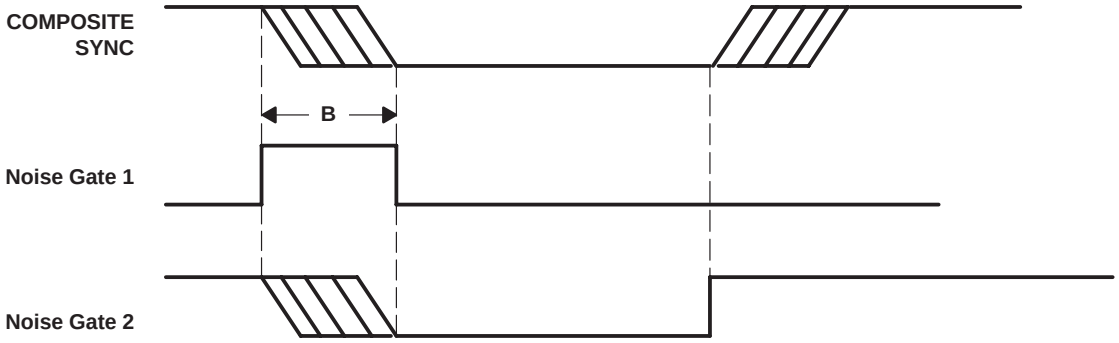


Figure 2. Proper COMPOSITE SYNC Timing

Table 3. Sync and Clamp Timing for NTSC and PAL with CLK = 4 fsc

TIME INTERVAL	NTSC fsc = 3.58 MHz		PAL fsc = 4.43 MHz	
	NO. OF CLOCKS	TIME (μs)	NO. OF CLOCKS	TIME (μs)
A	867	60.6	1075	60.7
B	43	3	61	3.5
C	58	4.05	58	3.27
D	6	0.42	6	0.34
E	76	5.3	93	5.25
F	54	3.77	84	4.74

using an external clamp pulse

When CLPEN is taken low, EXTCLP accepts an externally generated active-high clamp pulse. This pulse must occur within the horizontal-blanking interval back porch. CLPEN low inhibits the internal counters and no internal clamp pulse is generated.

output digital code (for each channel of ADC)

Table 4. Input Signal Versus Digital Output Code

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
$V_{ref(RT)}$	255	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
$V_{ref(RB)}$	0	0	0	0	0	0	0	0	0

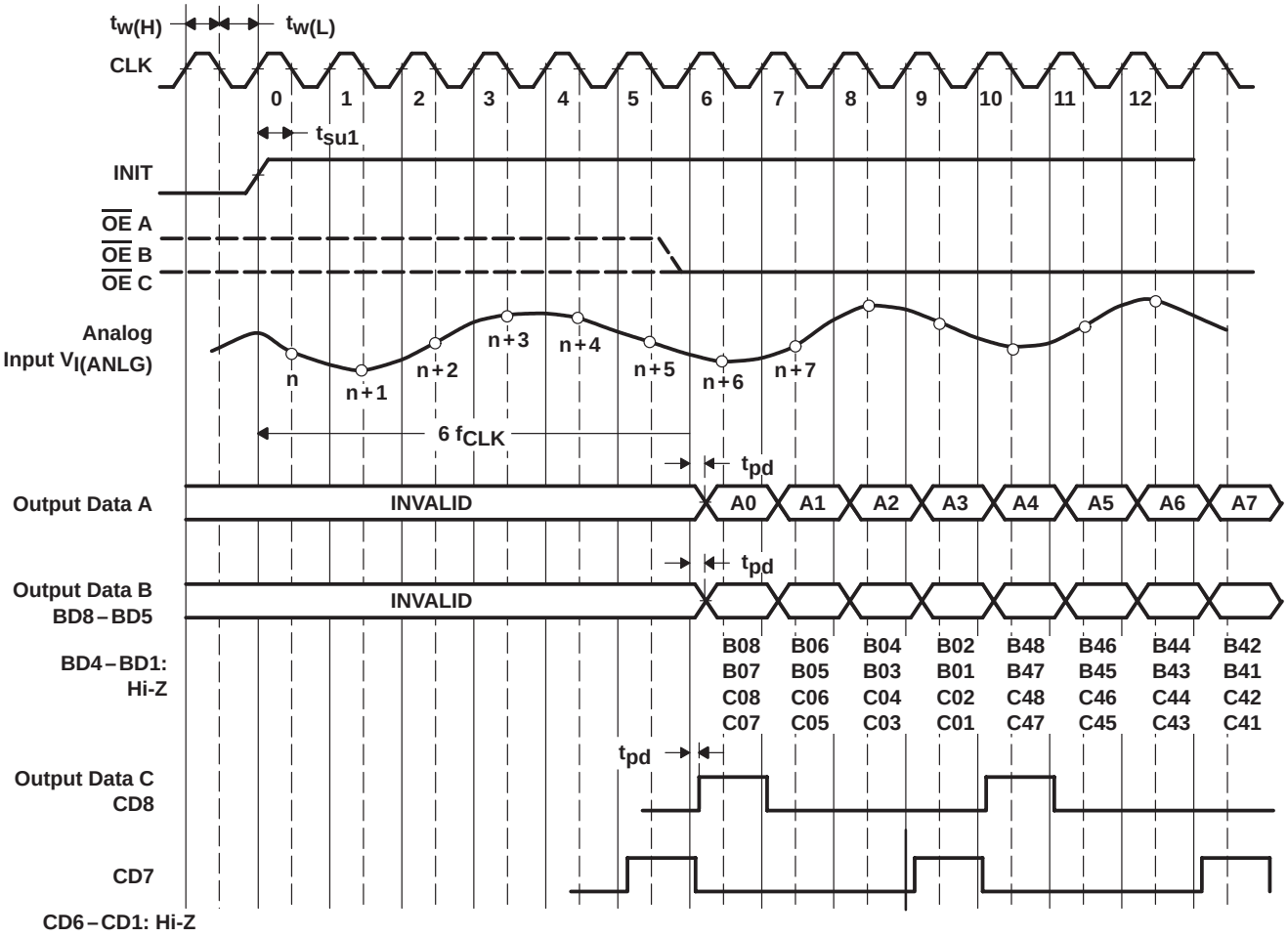
output data format

The TLC5733A can select three output data formats to various TV/VCR (video) data processing by the combination of MODE0 and MODE1. The output is synchronous when INIT is taken high.

Table 5. Output Data Format Selection

CONDITION		OUTPUT DATA	
MODE1	MODE0	OUTPUT DATA FORMAT	RATIO OF Y:U:V
L	L	Format 1	4:1:1
L	H	Format 2	4:4:4
H	L	Format 3	4:2:2
H	H	Not used	N/A

output data format (continued)



○ = Input signal sampling point

Figure 3. Format 1, 4:1:1

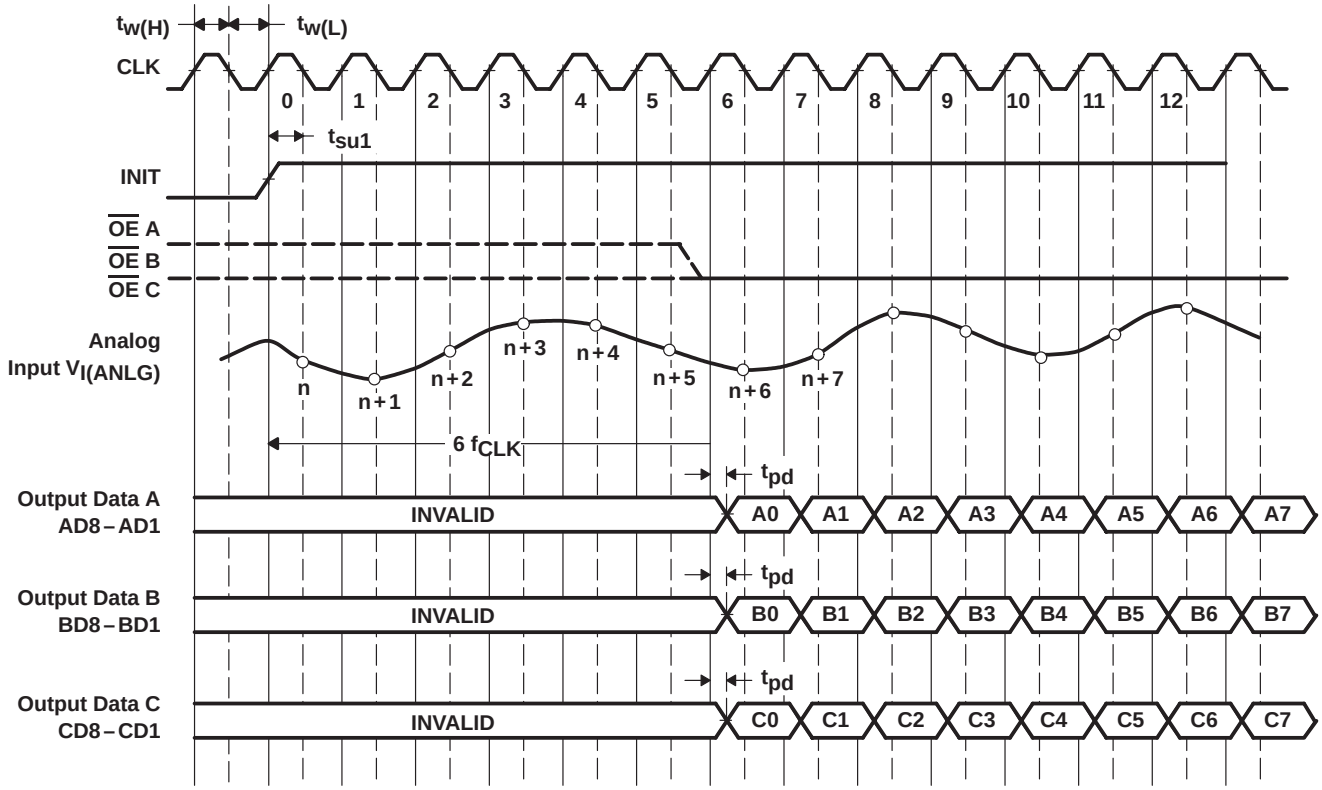
output data format (continued)

Table 6. Format 1

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK (see Note 1)							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B06	B04	B02	B48	B46	B44	B42
	BD7	B07	B05	B03	B01	B47	B45	B43	B41
	BD6	C08	C06	C04	C02	C48	C46	C44	C42
	BD5	C07	C05	C03	C01	C47	C45	C43	C41
	BD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	BD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
C	CD8	H	L	L	L	H	L	L	L
	CD7	L	L	L	H	L	L	L	H
	CD6	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD5	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

NOTES: 1. The value of the first sampling clock at A/D conversion is CLK 0.
2. A06 is an example of an entry in the table where A is the ADC channel, 0 is the sampling order, and 6 is the bit number.

output data format (continued)



○ = Input signal sampling point

Figure 4. Format 2, 4:4:4

output data format (continued)

Table 7. Format 2

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK (see Note 1)							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	B18	B28	B38	B48	B58	B68	B78
	BD7	B07	B17	B27	B37	B47	B57	B67	B77
	BD6	B06	B16	B26	B36	B46	B56	B66	B76
	BD5	B05	B15	B25	B35	B45	B55	B65	B75
	BD4	B04	B14	B24	B34	B44	B54	B64	B74
	BD3	B03	B13	B23	B33	B43	B53	B63	B73
	BD2	B02	B12	B22	B32	B42	B52	B62	B72
	BD1	B01	B11	B21	B31	B41	B51	B61	B71
C	CD8	C08	C18	C28	C38	C48	C58	C68	C78
	CD7	C07	C17	C27	C37	C47	C57	C67	C77
	CD6	C06	C16	C26	C36	C46	C56	C66	C76
	CD5	C05	C15	C25	C35	C45	C55	C65	C75
	CD4	C04	C14	C24	C34	C44	C54	C64	C74
	CD3	C03	C13	C23	C33	C43	C53	C63	C73
	CD2	C02	C12	C22	C32	C42	C52	C62	C72
	CD1	C01	C11	C21	C31	C41	C51	C61	C71

NOTES: 1. The value of the first sampling clock at A/D conversion is CLK 0.
2. A06 is an example of an entry in the table where A is the ADC channel, 0 is the sampling order, and 6 is the bit number.

output data format (continued)

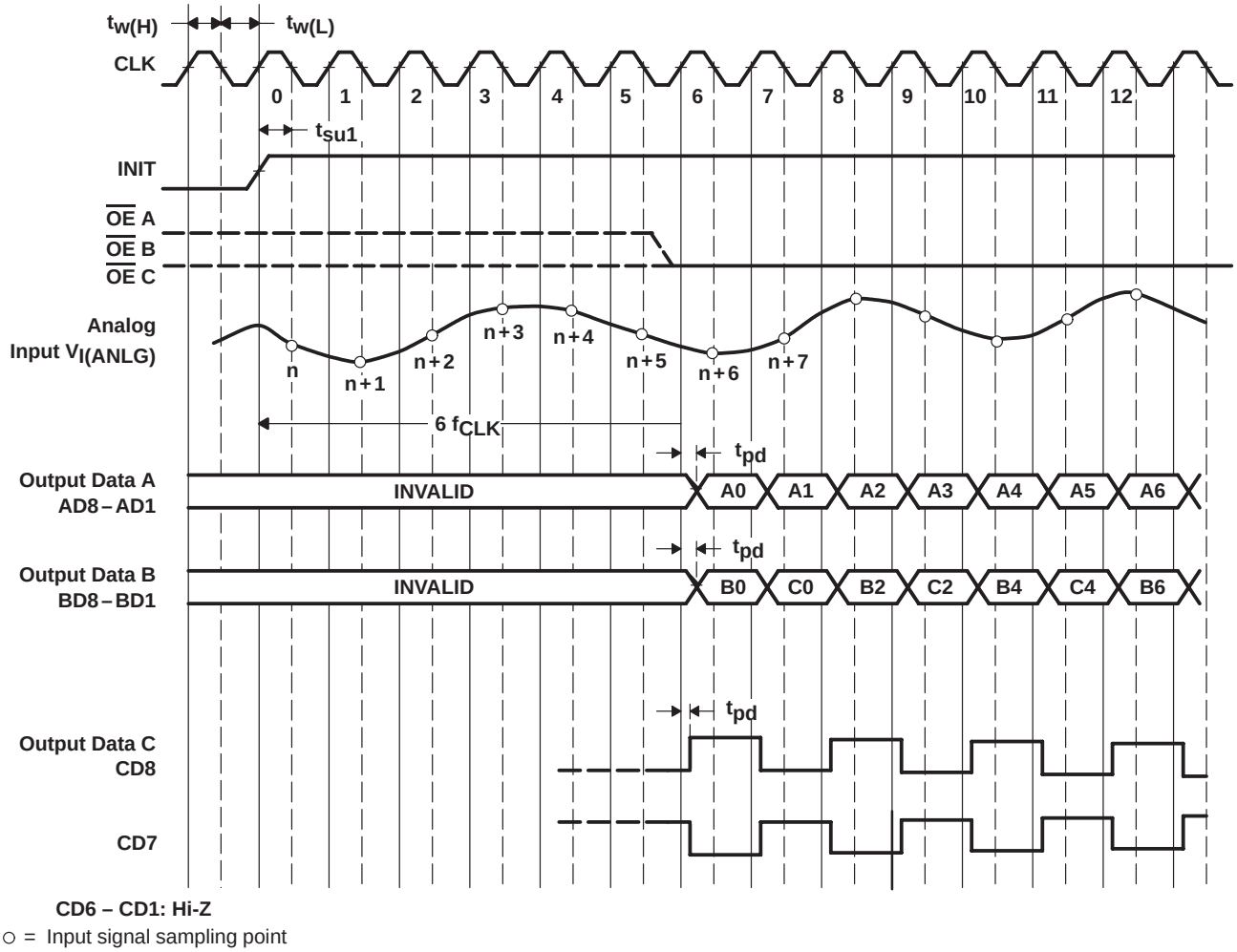


Figure 5. Format 3, 4:2:2

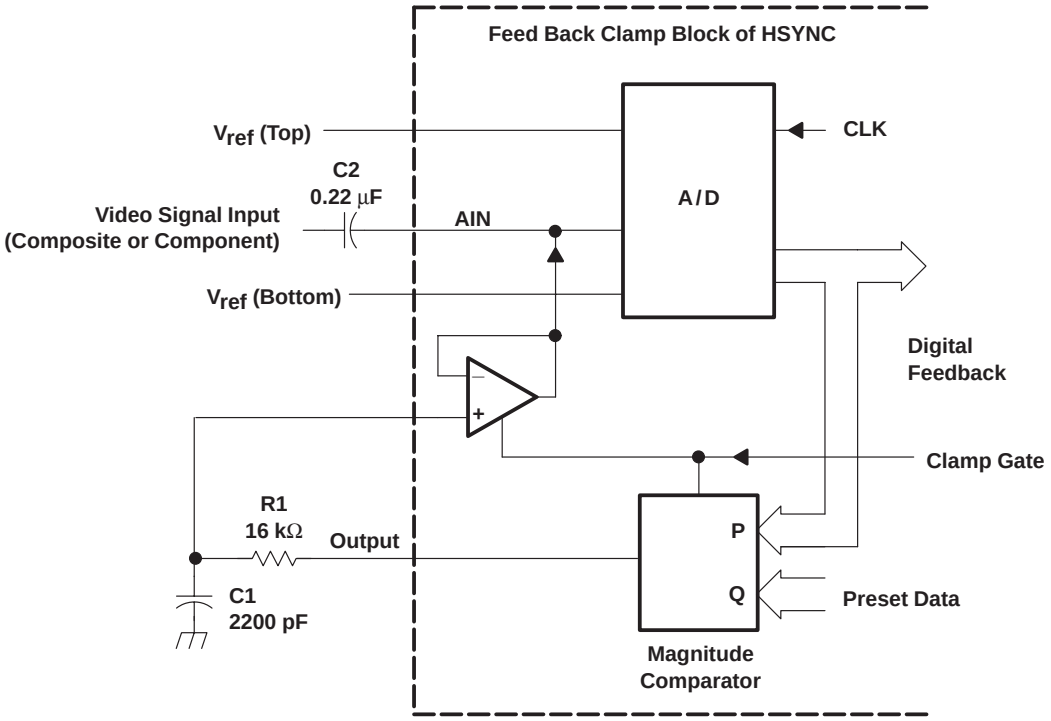
output data format (continued)

Table 8. Format 3

CHANNEL OF ADC	BIT	OUTPUT DATA							
		CLK (see Note 1)							
		6	7	8	9	10	11	12	13
A	AD8	A08	A18	A28	A38	A48	A58	A68	A78
	AD7	A07	A17	A27	A37	A47	A57	A67	A77
	AD6	A06	A16	A26	A36	A46	A56	A66	A76
	AD5	A05	A15	A25	A35	A45	A55	A65	A75
	AD4	A04	A14	A24	A34	A44	A54	A64	A74
	AD3	A03	A13	A23	A33	A43	A53	A63	A73
	AD2	A02	A12	A22	A32	A42	A52	A62	A72
	AD1	A01	A11	A21	A31	A41	A51	A61	A71
B	BD8	B08	C08	B28	C28	B48	C48	B68	C68
	BD7	B07	C07	B27	C27	B47	C47	B67	C67
	BD6	B06	C06	B26	C26	B46	C46	B66	C66
	BD5	B05	C05	B25	C25	B45	C45	B65	C65
	BD4	B04	C04	B24	C24	B44	C44	B64	C64
	BD3	B03	C03	B23	C23	B43	C43	B63	C63
	BD2	B02	C02	B22	C22	B42	C42	B62	C62
	BD1	B01	C01	B21	C21	B41	C41	B61	C61
C	CD8	H	L	H	L	H	L	H	L
	CD7	L	H	L	H	L	H	L	H
	CD6	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD5	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD4	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD3	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD2	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	CD1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

NOTES: 1. The value of the first sampling clock at A/D conversion is CLK 0.
2. A06 is an example of an entry in the table where A is the ADC channel, 0 is the sampling order, and 6 is the bit number.

APPLICATION INFORMATION



FEEDBACK CLAMP AND CHARGE PUMP ACTIVITY

INPUT DATA CONDITIONS	OUTPUT		CHARGE PUMP CONDITIONS
P < Q	Active	H	Charge
P = Q	Hold	Z	Hold
P > Q	Active	L	Discharge

Figure 6. Feedback Clamp Circuit

APPLICATION INFORMATION

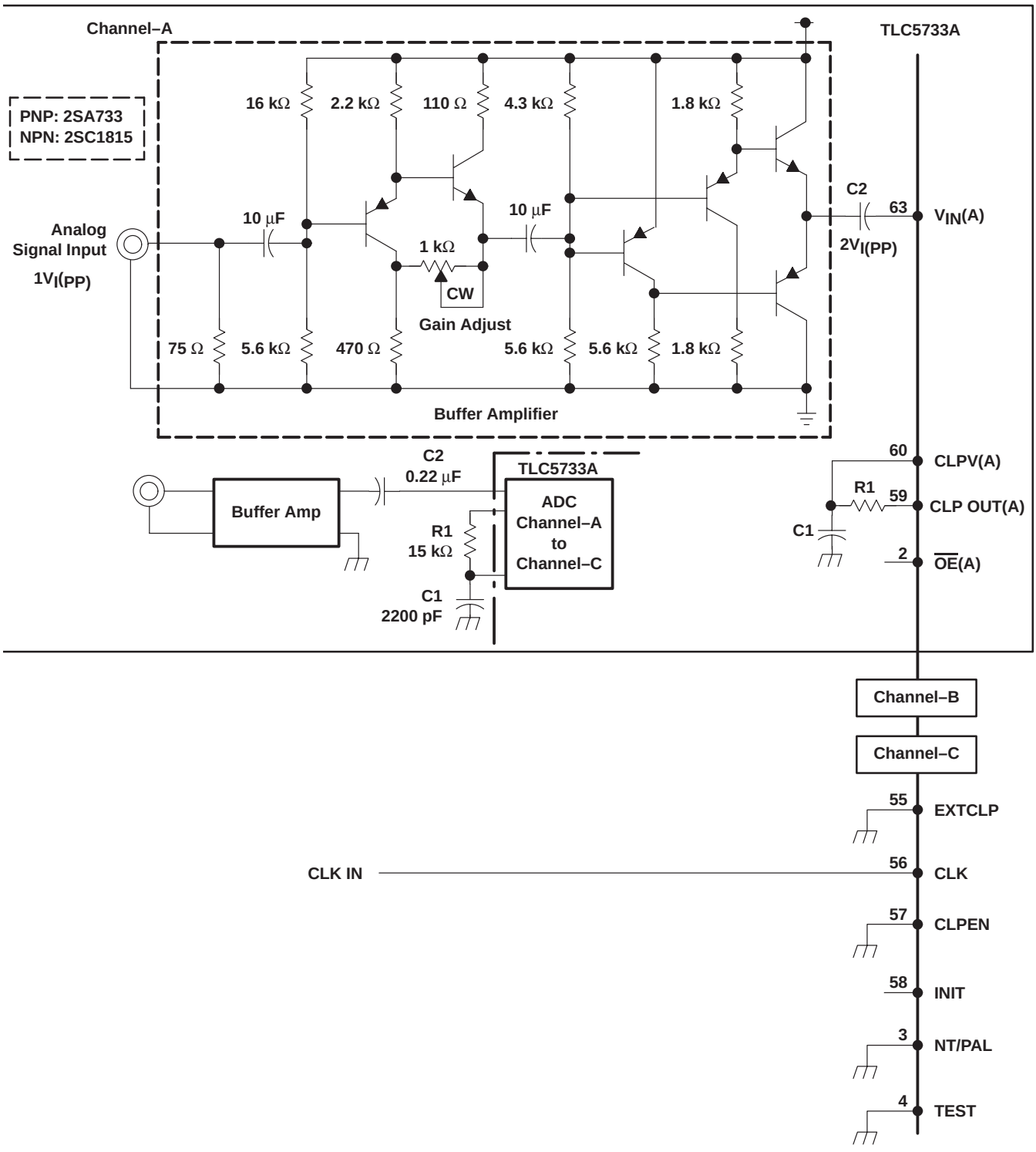


Figure 7. Interface Without Clamping

APPLICATION INFORMATION

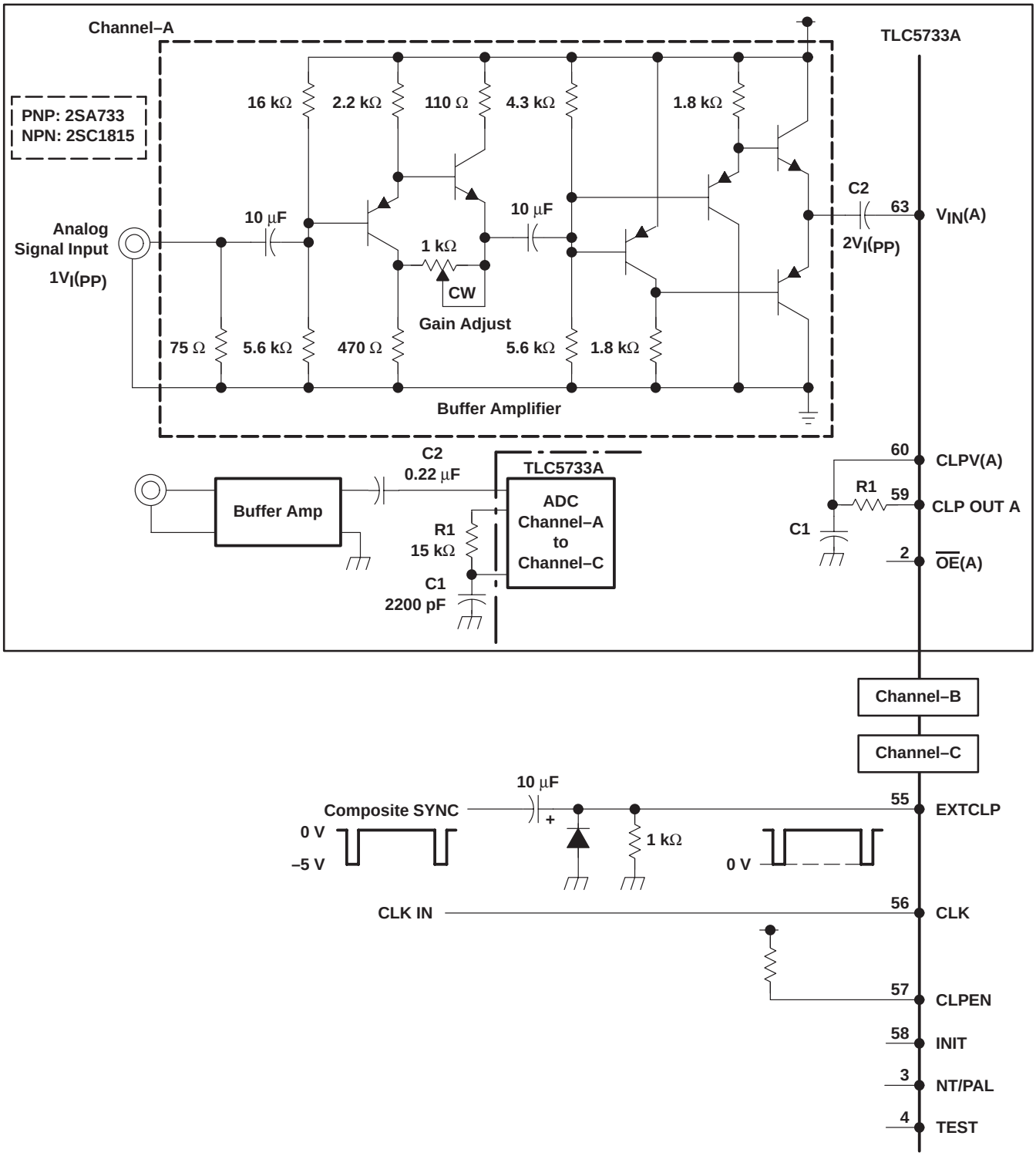


Figure 8. Interface Connection Using Composite Sync Signal

APPLICATION INFORMATION

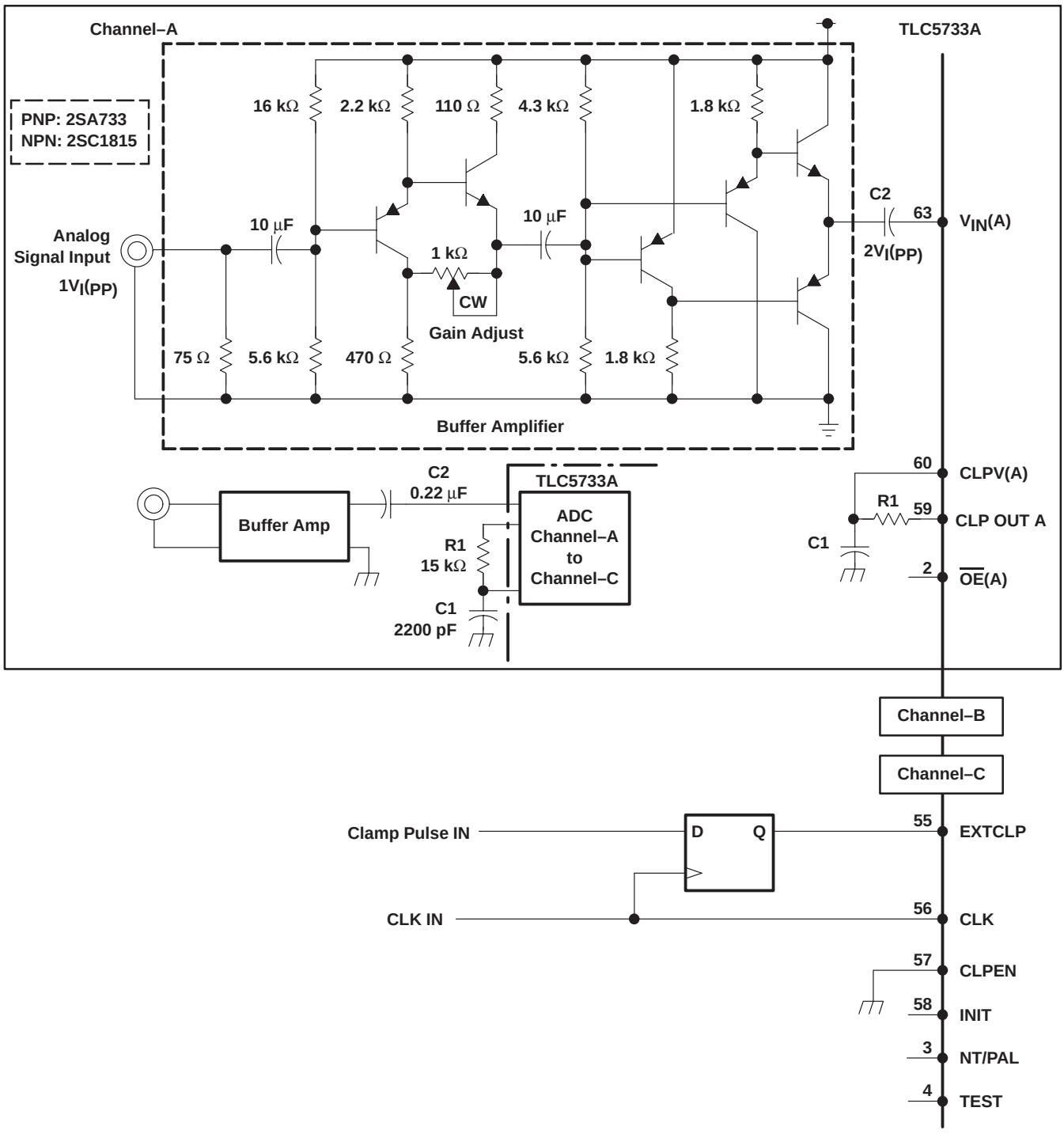


Figure 9. Interface Using External Clamp Pulse With Synchronization

APPLICATION INFORMATION

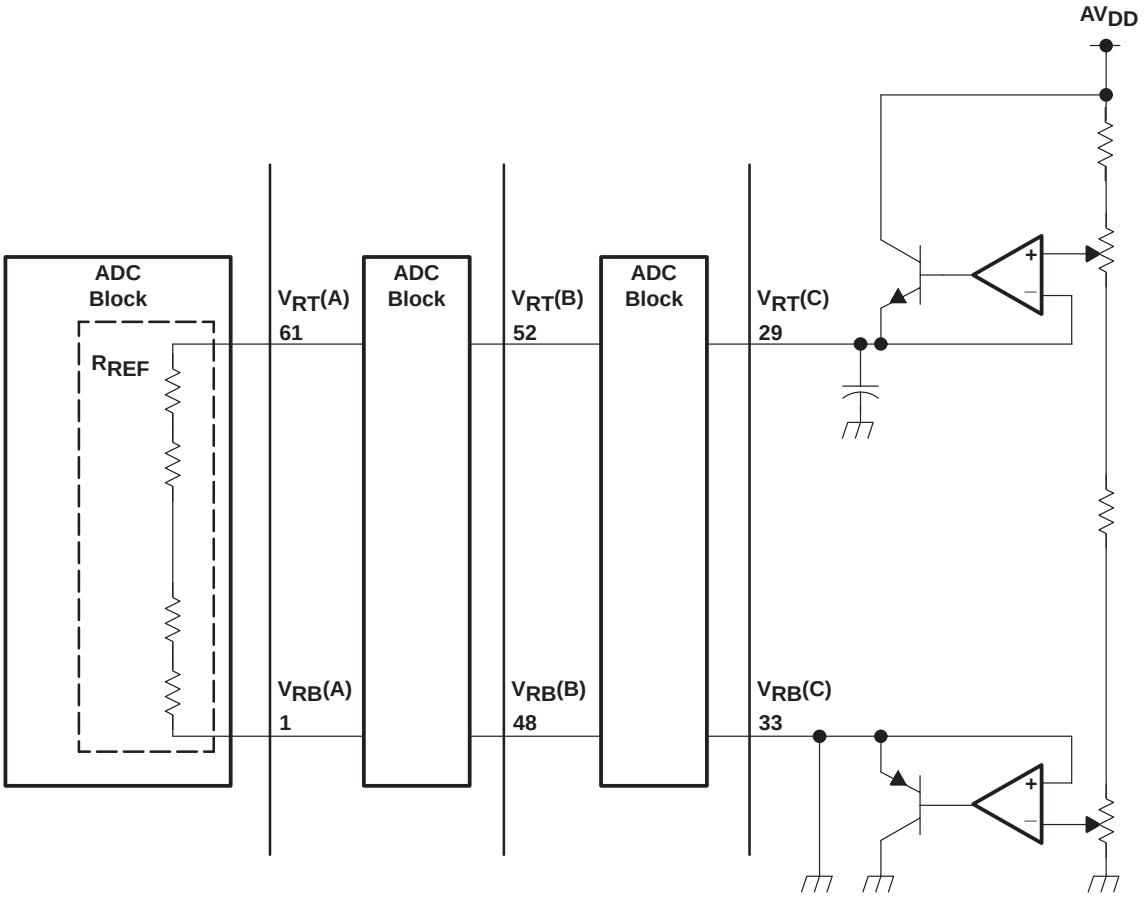
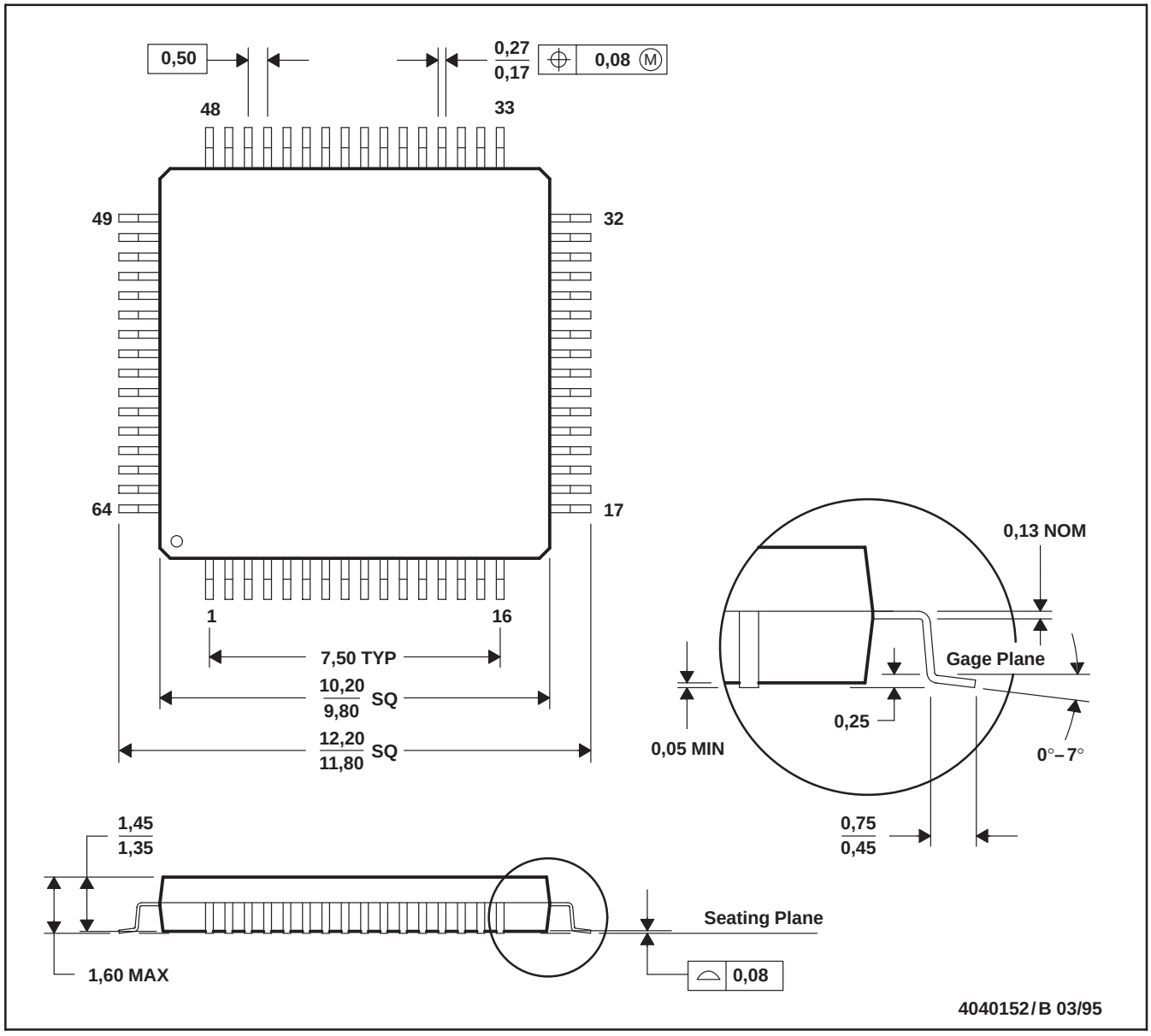


Figure 10. Adjustment Circuit For Top and Bottom Reference Voltages

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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