

# Positive Floating Hot Swap Power Manager

## FEATURES

- Manages Hot Swap of 15V and Above
- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable Overcurrent Limit
- Programmable Fault Time
- Internal Charge Pump to Control External NMOS Device
- Fault Output and Catastrophic Fault Indication
- Fault Mode Programmable to Latch or Retry
- Shutdown Control
- Undervoltage Lockout

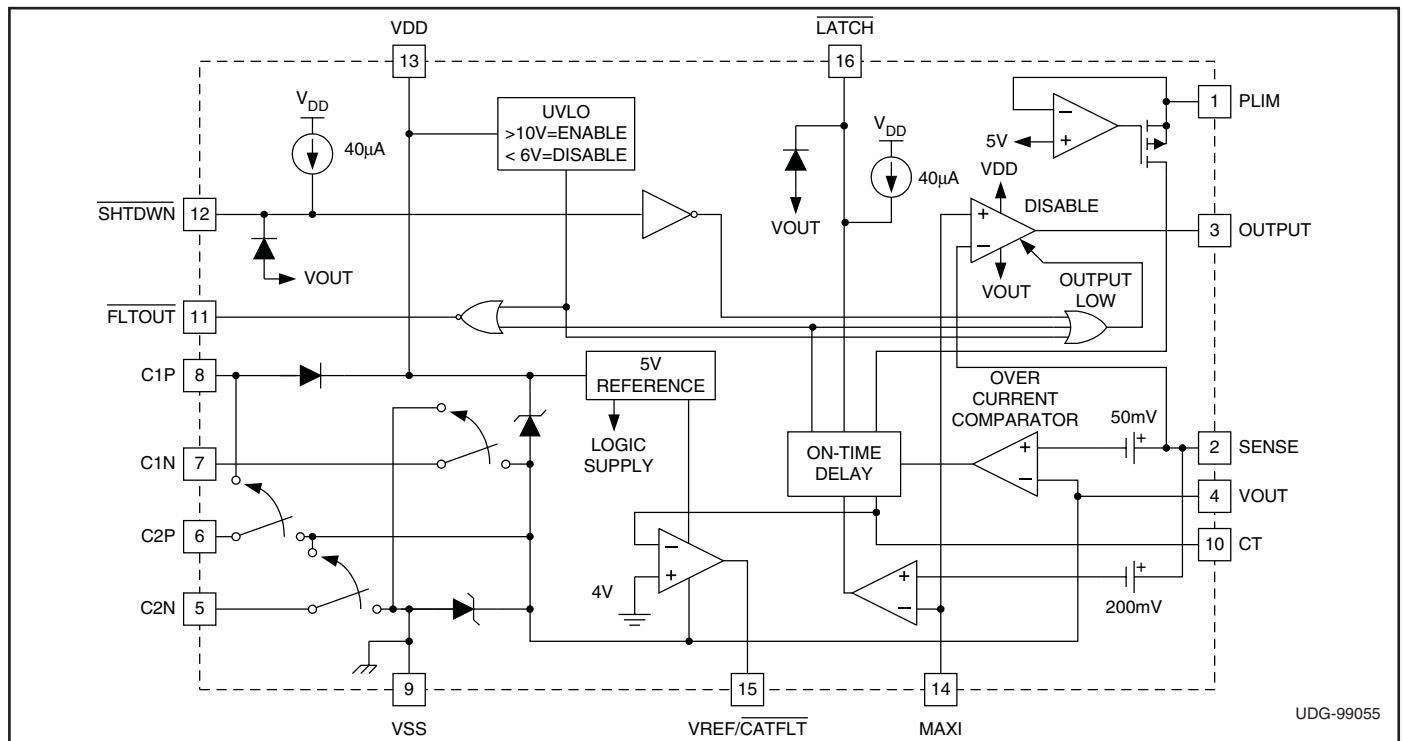
## DESCRIPTION

The UCC3917 family of positive floating hot swap managers provides complete power management, hot swap, and fault handling capability. The voltage limitation of the application is only restricted by the external component voltage limitations. The IC provides its own supply voltage via a charge pump off of VOUT. The onboard 10V shunt regulator protects the IC from excess voltage. The IC also has catastrophic fault indication to alert the user that the ability to shut off the output NMOS has been bypassed. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft start time, and average NMOS power limiting.

The fault level across the current sense amplifier is fixed at 50mV to minimize total drop out. Once 50mV is exceeded across the current sense resistor, the fault timer will start. The maximum allowable sourcing current is programmed with a voltage divider from the VREF/CATFLT pin to generate a fixed voltage on the MAXI pin. The current level at which the output appears as a current source is equal to VMAXI divided by the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on MAXI.

When the output current is below the fault level, the output device is switched on with full gate drive. When the output current exceeds the fault level, but is less than maximum allowable sourcing level programmed by MAXI, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and attempts either a retry sometime later or waits for the state on the LATCH pin to change if in latch mode. When the output current reaches the maximum sourcing current level, the output device appears as a current source.

## BLOCK DIAGRAM



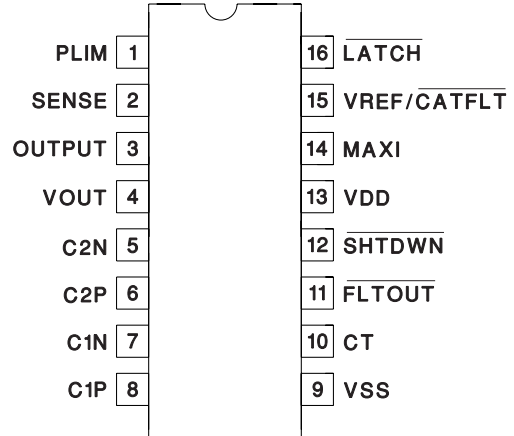
## ABSOLUTE MAXIMUM RATINGS

IDD	20mA
SHTDWN Current	−500μA
LATCH Current	−500μA
VREF Current	−500μA
PLIM Current	10mA
MAXI Input Voltage	VDD + 0.3V
Storage Temperature	−65°C to +150°C
Junction Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

*Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.*

## CONNECTION DIAGRAM

**DIL-16, SOIC-16 (Top View)  
J or N Package, D Package**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for the UCC3917,  $-40^\circ\text{C}$  to  $85^\circ$  for the UCC2917 and  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for the UCC1917,  $C_T = 4.7\text{nF}$ .  $T_A = T_J$ . All voltages are with respect to VOUT. Current is positive into and negative out of the specified terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>VDD Section</b>					
IDD	From VOUT (Note 1)	3.0	5	11	mA
UVLO Turn On Threshold		7.9	8.8	9.7	V
UVLO Off Voltage		5.5	6.5	7.5	V
VSS Regulator Voltage		−6	−5	−4	V
<b>Fault Timing Section</b>					
Overcurrent Threshold	$T_A = 25^\circ\text{C}$	47.5	50	53	mV
	Over Operating Temperature	46	50	54	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	$V_{CT} = 1\text{V}$	−78	−50	−28	μA
CT Catastrophic Fault Threshold		3.4		4.5	V
CT Fault Threshold		2.25	2.5	2.75	V
CT Reset Threshold		0.32	0.5	0.62	V
Output Duty Cycle	Fault Condition	1.7	2.7	3.7	%
<b>Output Section</b>					
Output High Voltage	$I_{OUT} = 0$	6	8	10	V
	$I_{OUT} = -500\mu\text{A}$	5	7	9	V
Output Low Voltage	$I_{OUT} = 0$		0	0.05	V
	$I_{OUT} = 500\mu\text{A}$		0.1	0.5	V
	$I_{OUT} = 1\text{mA}$		0.5	0.9	V
<b>Linear Current Section</b>					
Sense Control Voltage	$MAXI = 100\text{mV}$	85	100	115	mV
	$MAXI = 400\text{mV}$	370	400	430	mV
Input Bias	$MAXI = 200\text{mV}$		50	500	nA
<b>SHUTDOWN Section</b>					
Shutdown Threshold		2.0	2.4	2.8	V
Input Current	$SHTDWN = 0\text{V}$	24	40	60	μA
Shutdown Delay			100	500	ns

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>LATCH Section</b>					
Latch Threshold		1.7	2	2.3	V
Input Current	LATCH = 0V	24	40	60	$\mu\text{A}$
<b>Fault Out Section</b>					
Fault Output High		6	8	10	V
Fault Output Low			0.01	0.05	V
<b>Power Limiting Section</b>					
VSENSE Regulator Voltage	$I_{\text{PLIMIT}} = 64\mu\text{A}$	4.5	5	5.5	V
Duty Cycle Control	$I_{\text{PLIMIT}} = 64\mu\text{A}$	0.6	1.2	1.7	%
	$I_{\text{PLIMIT}} = 1\text{mA}$	0.045	0.1	0.2	%
<b>VREF/CATFLT Section</b>					
VREF Regulator Voltage		4.5	5	5.5	V
Fault Output Low	$I_{\text{VREF/CATFLT}} = 5\text{mA}$		0.22	0.50	V
Output Sink Current	$V_{\text{CT}} = 5\text{V}$ , $V_{\text{VREF/CATFLT}} = 5\text{V}$	15	40	70	mA
Overload Comparator Threshold	Relative to MAXI	110	200	290	mV

Note 1: Set by user with  $R_{\text{SS}}$ .

## PIN DESCRIPTIONS

**C1N:** Negative side of the upper charge pump capacitor.

**C1P:** Positive side of the upper charge pump capacitor.

**C2N:** Negative side of the lower charge pump capacitor.

**C2P:** Positive side of lower charge pump capacitor.

**CT:** A capacitor is connected to this pin to set the fault time. The fault time must be more than the time to charge the external load capacitance (see Application Information).

**FLTOUT:** This pin provides fault output indication. Interface to this pin is usually performed through level shift transistors. Under a non-fault condition, FLTOUT will pull to a high state. When a fault is detected by the fault timer or the under voltage lockout, this pin will drive to a low state, indicating the output NMOS is in the off state.

**LATCH:** Pulling this pin low causes a fault to latch until this pin is brought high or a power on reset is attempted. However, pulling this pin high before the reset time is reached will not clear the fault until the reset time is reached. Keeping LATCH high will result in normal operation of the fault timer. Users should note there will be an RC delay dependent upon the external capacitor at this pin.

**MAXI:** This pin programs the maximum allowable sourcing current. Since VREF/CATFLT is a regulated voltage, a voltage divider can be derived to generate the program level for MAXI. The current level at which the output appears as a current source is equal to the volt-

age on MAXI divided by the current sense resistor. If desired, a controlled current start up can be programmed with a capacitor on MAXI (to VOUT), and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

**OUTPUT:** Gate drive to the NMOS pass element.

**PLIM:** This feature ensures that the average external NMOS power dissipation is controlled. A resistor is connected from this pin to the drain of the external NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into PLIM which adds to the fault timer charge current, reducing the duty cycle from the 3% level.

**SENSE:** Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VOUT, a fault is sensed, and CT starts to charge.

**SHTDWN:** This pin provides shutdown control. Interface to this pin is usually performed through level shift transistors. When shutdown is driven low, the output disables the NMOS pass device.

**VDD:** Power to the I.C. Is supplied by an external current limiting resistor on initial power-up or if the load is shorted. As the load voltages rises (VOUT), a small amount of power is drawn from VOUT by an internal charge pump. The charge pump's input voltage is regulated by an on-chip 5V zener. Power to VDD is supplied



## APPLICATION INFORMATION (cont.)

$$\text{Duty Cycle} = \frac{I_2}{I_{PL} + I_1} \cong \frac{1.5\mu\text{A}}{I_{PL} + 50\mu\text{A}}$$

where  $I_{PL}$  is  $0\mu\text{A}$  under normal operations (see Fig. 2).

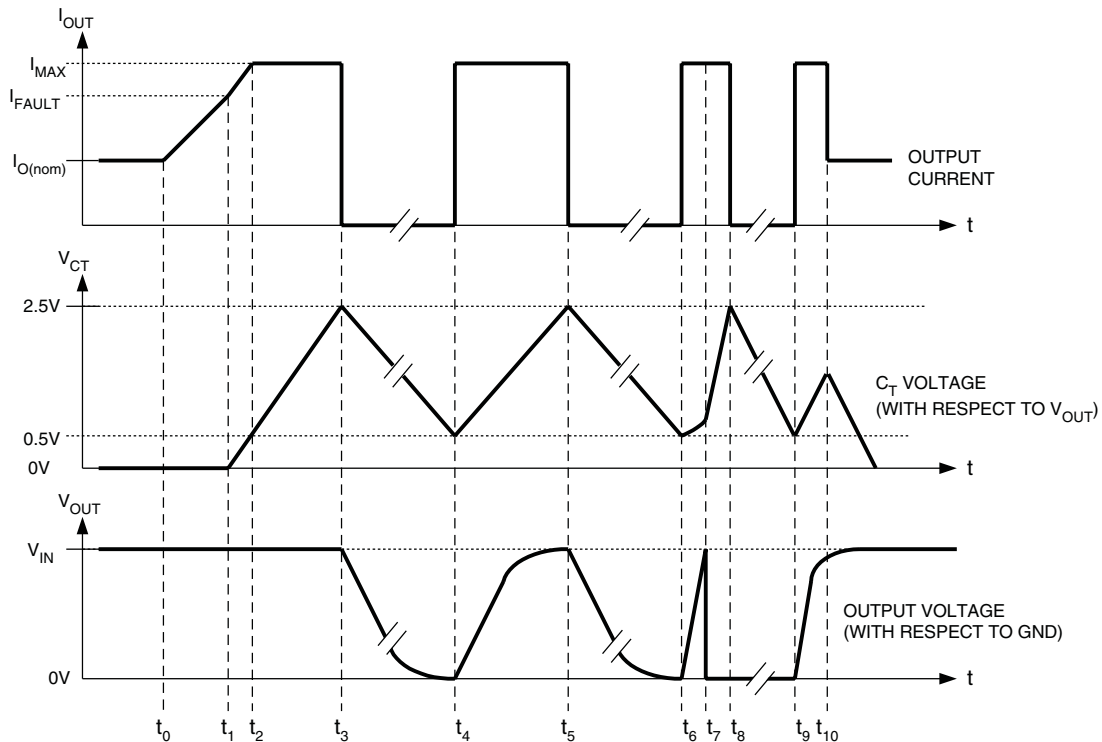
However, under large transients, average power dissipation can be limited using the PLIM pin. A proof follows, average dissipation in the pass element is given by:

$$P_{\text{FET AVG}} = (V_{\text{IN}} - V_{\text{OUT}}) \cdot I_{\text{MAX}} \cdot \text{Duty Cycle}$$

$$= (V_{\text{IN}} - V_{\text{OUT}}) \cdot I_{\text{MAX}} \cdot \frac{1.5\mu\text{A}}{I_{PL} + 50\mu\text{A}}$$

Where  $(V_{\text{IN}} - V_{\text{OUT}}) \gg 5\text{V}$ ,

$$I_{PL} \cong \frac{V_{\text{IN}} - V_{\text{OUT}}}{R_{PL}}$$



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**t0:** Safe condition - output current is nominal, output voltage is at the positive rail,  $V_{\text{IN}}$ .

**t1:** Fault control reached - output current rises above the programmed fault value, CT begins to charge with  $\cong 50\mu\text{A}$ .

**t2:** Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value  $I_{\text{MAX}}$ .

**t3:** Fault occurs - CT has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow,  $V_{\text{OUT}}$  discharges to ground.

**t4:** Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on,  $V_{\text{OUT}}$  rises to  $V_{\text{IN}}$ .

**t5 = t3:** Illustrates 3% duty cycle.

**t6 = t4:**

**t7:** Output short circuit - if  $V_{\text{OUT}}$  is short circuited to ground, CT charges at a higher rate depending upon the values for  $V_{\text{IN}}$  and  $R_{\text{PL}}$ .

**t8:** Fault occurs - output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

**t9 = t4:** Output short circuit released, still in fault mode.

**t10 = t0:** Fault released, safe condition - return to normal operation of the circuit breaker.

Note that  $t6 - t5 \cong 36 \cdot (t5 - t4)$ .

Figure 2. Nominal timing diagram.

## APPLICATION INFORMATION (cont.)

and where  $I_{PL} \gg 50\mu A$ , the duty cycle can be approximated as:

$$\frac{1.5\mu A \cdot R_{PL}}{V_{IN} - V_{OUT}}$$

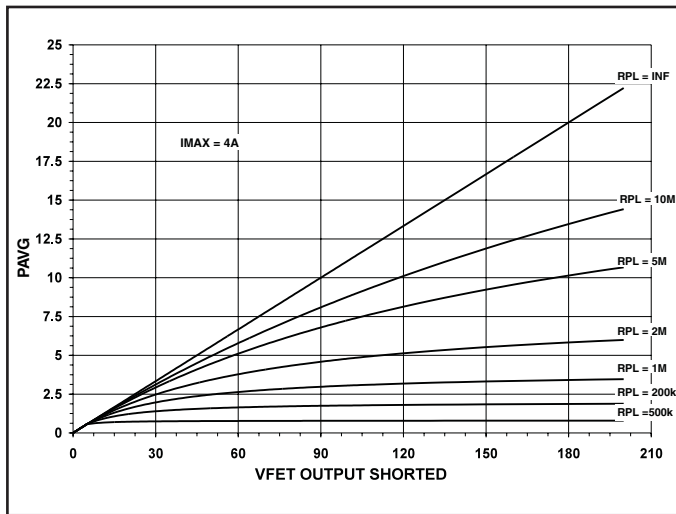
Therefore the average power dissipation in the MOSFET can be approximated by:

$$P_{FET\ AVG} = (V_{IN} - V_{OUT}) \cdot I_{MAX} \cdot \frac{1.5\mu A \cdot R_{PL}}{V_{IN} - V_{OUT}}$$

$$= I_{MAX} \cdot 1.5\mu A \cdot R_{PL}$$

Notice that since  $(V_{IN} - V_{OUT})$  cancels, average power dissipation is limited in the NMOS pass element (see Fig. 3). Also, a value for  $R_{PL}$  can be roughly determined from this approximation.

$$R_{PL} = \frac{P_{FET\ AVG}}{I_{MAX} \cdot 1.5\mu A}$$



**Figure 3. Plot of average power vs. FET voltage for increasing values of  $R_{PL}$ .**

## Overload Comparator

The overload comparator provides protection against a shorted load during normal operation when the external N-channel FET is fully enhanced. Once the FET is fully enhanced the linear current amplifier essentially saturates and the system is in effect operating open loop. Once the FET is fully enhanced the linear current amplifier requires a finite amount of time to respond to a shorted output possibly destroying the external FET. The overload comparator is provided to quickly shutdown the external MOSFET in the case of a shorted output (if the FET is fully enhanced). During an output short CT is charged by  $I_3$  at  $\sim 1mA$ . The current threshold for the overload comparator is a function of  $I_{MAX}$  and a fixed offset and is defined as:

$$I_{OVERLOAD} = I_{MAX} + 200mV / R_S$$

Once the overcurrent comparator trips the UCC3917 will enter programmed fault mode (hiccup or latched). It should be noted that on subsequent retries during Hiccup mode or if a short should occur when the UCC3917 is actively limiting the current, the output current will not exceed  $I_{MAX}$ . In the event that the external FET does not respond during a fault the UCC3917 will set the VREF/CATFLT pin low to indicate a catastrophic failure.

## Selecting the Minimum Timing Capacitance

To ensure that the IC will startup correctly the designer must ensure that the fault time programmed by CT exceeds the startup time of the load. The startup time ( $T_{START}$ ) is a function of several components; load resistance and load capacitance, soft start components R1, R2 and  $C_{SS}$ , the power limit current contribution determined by  $R_{PL}$ , and  $C_{IN}$ .

For a parallel capacitor-constant current load: (1)

$$T_{START} = \frac{C_{LOAD} \cdot V_{IN}}{I_{MAX} - I_{LOAD}}$$

For a parallel R-C load :

$$T_{START} = -R_{LOAD} \cdot C_{LOAD} \cdot \ln \left[ 1 - \frac{V_{IN}}{I_{MAX} \cdot R_{LOAD}} \right] \quad (2)$$

If the power limit function is not be used then CT(min) can be easily found:

$$CT(min) = \frac{I_{CH} \cdot T_{START}}{dV_{CT}} \quad (3)$$

where  $dV_{CT}$  is the hysteresis on the fault detection circuitry. During operation in the latched fault mode configuration  $dV_{CT} = 2.5V$ . When the UCC3917 is configured for the hiccup or retry mode of fault operation  $dV_{CT} = 2.0V$ .

If the power limit function is used the CT charging current becomes a function of  $I_{CH} + I_{PL}$ . And CT(min) is found from:

## APPLICATION INFORMATION (cont.)

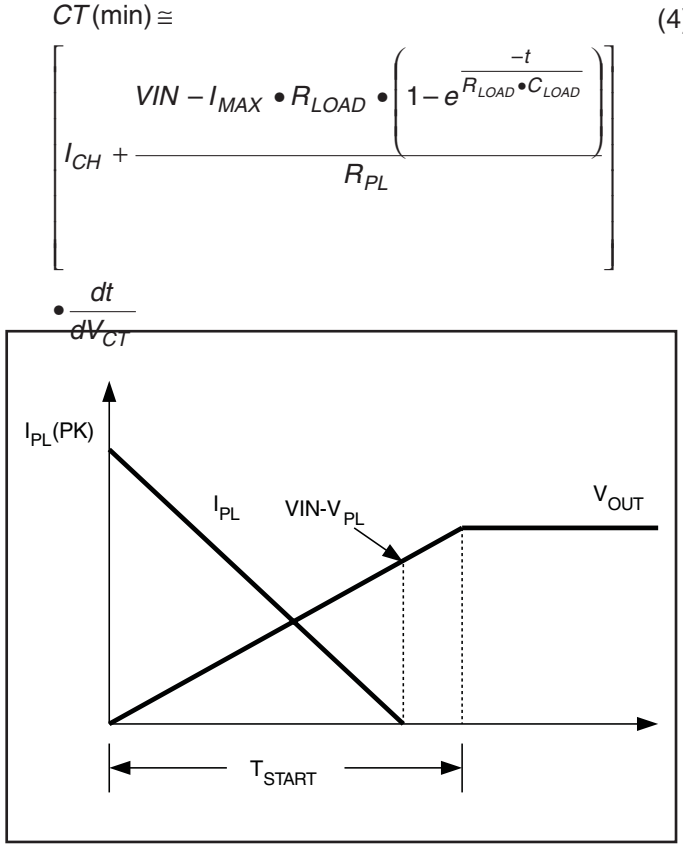


Figure 4. Relationship between  $I_{PL}$ ,  $V_{OUT}$  and  $T_{START}$ .

Since  $I_{PL}$  is a function of the output voltage,  $V_{OUT}$ , which varies over time, equation 4 must be integrated to solve for  $CT(\min)$ . However equation 4 can be easily approximated if the output voltage slews. If the output voltage slews linearly then the  $CT$  charge current contribution from the power limit circuitry is shown to be at a peak when  $V_{OUT} = 0V$  and at  $0A$  when  $V_{OUT} = VIN - V_{PL}$ , where  $V_{PL}$  is the power limit voltage threshold.  $I_{PL}$  is shown in Fig. 4 below.

Where  $I_{PL}$  is defined as:

$$I_{PL} \equiv \frac{(VIN - V_{OUT} - V_{PL})}{R_{PL}} \quad (5)$$

The average  $I_{PL}$  current for the interval  $(0, T_{START})$  from Fig. 4 is defined as:

$$I_{PL}(AVG) \equiv \frac{(VIN - V_{PL})^2}{2 \cdot R_{PL} \cdot VIN} \quad (6)$$

Equation 4 can now be simplified to:

$$CT(\min) \equiv \frac{I_{CH} + I_{PL}(AVG)}{dV_{CT}} \cdot T_{START} \quad (7)$$

(4) Please note that the actual example, if the chip mode when operating into a short is defined by:

$$T(on) = \frac{CT \cdot dV_{CT}}{I_{CH} + I_{PL}(pk)} \text{ seconds} \quad (8)$$

where  $dV_{CT} \sim 2.0V$  and

$$I_{PL}(pk) = \frac{VIN}{R_{PL}} \text{ A} \quad (9)$$

### Selecting Other External Components

Other external components are necessary for correct operation of the IC. Referring to the application diagram at the back of the data sheet, resistors  $R_{SENSE}$ ,  $R_{SS}$ ,  $R1$ ,  $R2$  and  $R3$  are required and follow certain equations with a brief description following where applicable:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}} \text{ (Sense Resistor)}$$

$$R_{SS} = \frac{V_{IN} - 5V}{5mA} \text{ (Connected between VSS and GND)}$$

$$R3 = \frac{V_{IN} - 10}{5mA} \text{ (Used in series with a diode to connect VIN to VDD)}$$

$$(R1 + R2) > 20k\Omega \text{ (Current limit out of VREF)}$$

Lastly, the external capacitors used for the charge pump are required and need to equal  $0.1\mu F$ , i.e.  $C_{IN} = C_H = C1 = C2 = 0.1\mu F$ .

### LEVEL Shift Circuitry (Optional)

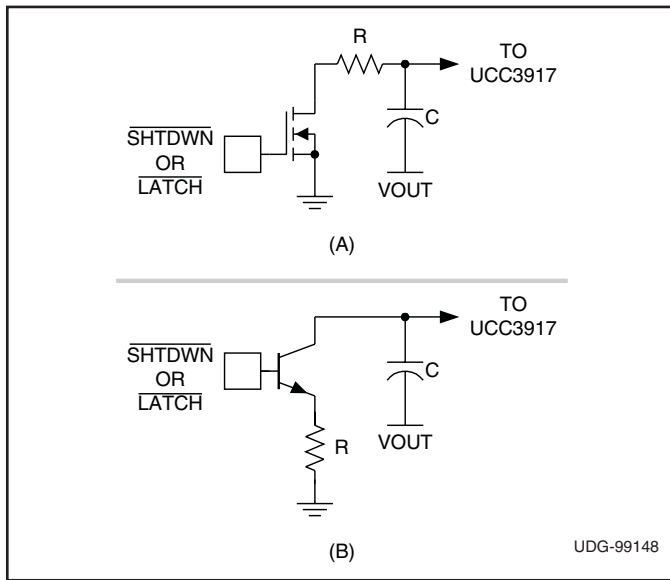
The UCC3917 can be used in many systems without logic command or diagnostic feedback. If a system requires control from low-voltage logic or feedback to low-voltage logic, then level shifting circuits are required. The level shift circuits in Fig. 5A and Fig. 5B show ways to interface to LATCH and SHTDWN and the level shift circuits in Fig. 6 show ways of interfacing from FLTOUT to low-voltage logic.

In Fig. 5A, resistor  $R$  limits the level shift current. Select  $R$  so that the current in the level shift circuit never exceeds the absolute maximum current in the logic command inputs,  $500\mu A$ . For example, if the maximum supply voltage for the system is  $75V$ , select

$$R > \frac{75V}{500\mu A} = 150k\Omega.$$

$R$  must also be chosen so that the minimum current in the level shift circuit exceeds the worst case logic

## APPLICATION INFORMATION (cont.)



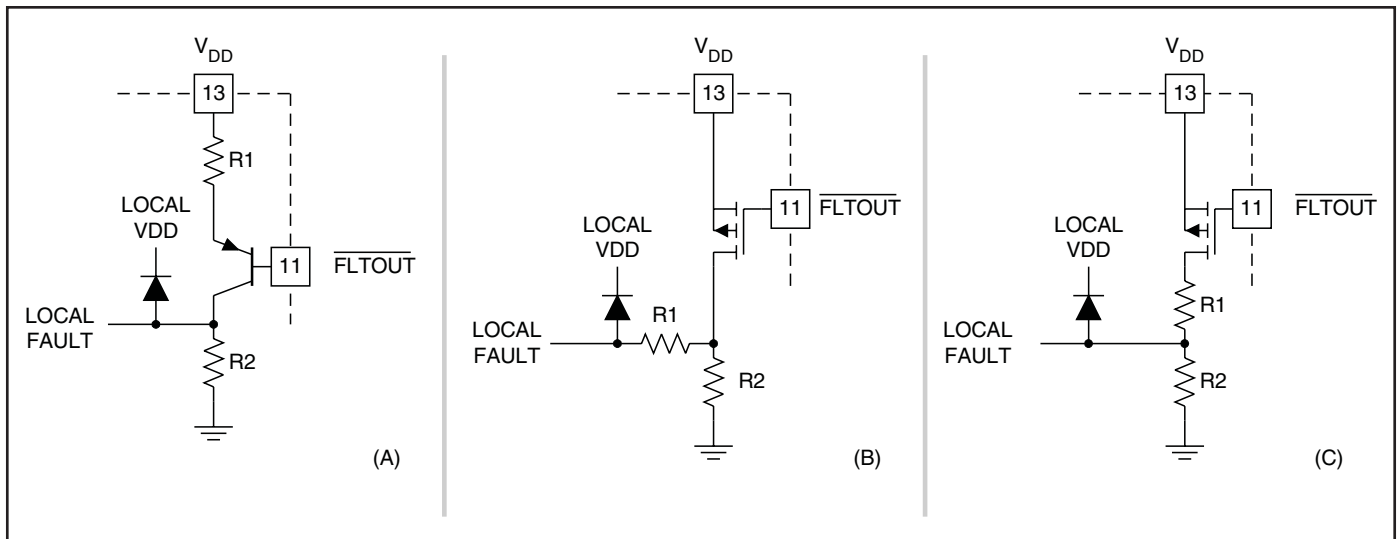
supply voltage for the system is 25V, choose

$$R > \frac{25V}{60\mu A} = 416 k\Omega.$$

The capacitor C shown on the output of this circuit is useful to filter the level shift output and prevent false triggering from noise. The minimum recommended capacitor value is 100pF. Larger capacitors will result in better noise immunity and longer delay to logic command.

The circuit in Fig. 5B accomplished the same function as the circuit in Fig. 5A, using different components. In this circuit, select resistor R so that the transistor draws enough current to exceed the 60μA logic threshold but doesn't exceed the 500μA maximum logic input current. For example, if the input circuit is 5V logic, then

**Figure 5. Potential level shift circuitry to interface to LATCH and SHTDWN on the**



**Figure 6. Potential level shift circuitry to interface to FLTOUT on the UCC3917.**



Although the UCC3917 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3917 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety

device such as a fuse should be placed in series with the power device. The UCC3917 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.