

27-30GHz High Power Amplifier

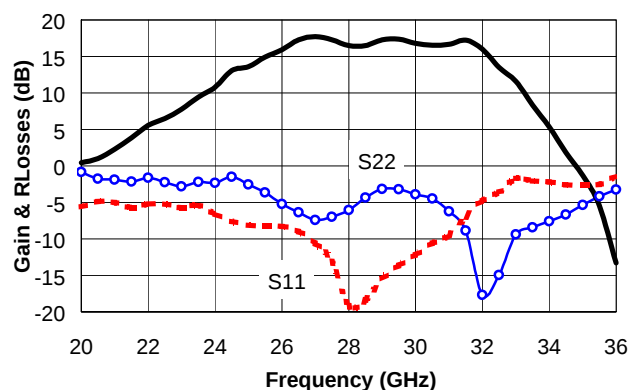
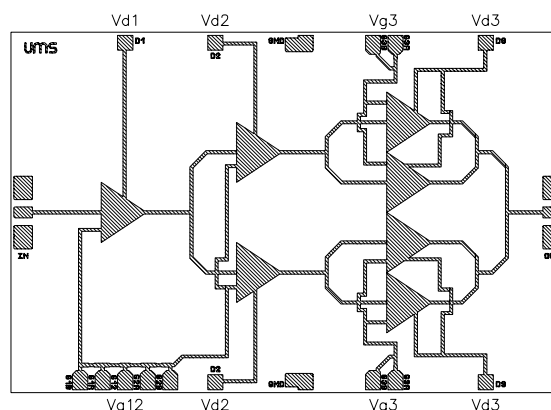
GaAs Monolithic Microwave IC

preliminary

Description

The CHA5296 is a high gain three-stage monolithic high power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process on 50 μ m substrate thickness, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



Typical on jig Measurements

Main Features

- Performances : 27-30GHz
- 29dBm output power @ 1dB comp. gain
- 15 dB $\pm$ 1dB gain
- DC power consumption, 850mA @ 6V
- Chip size : 3.80 x 2.52 x 0.05 mm

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	27		30	GHz
G	Small signal gain	14	15		dB
P1dB	Output power at 1dB gain compression	28	29		dBm
Id	Bias current		850	1000	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics

Tamb = +25°C, Vd = 6V Id #900mA

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Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	27		30	GHz
G	Small signal gain (1)	14	15		dB
ΔG	Small signal gain flatness (1)		± 1		dB
Is	Reverse isolation		50		dB
P1dB	Pulsed output power at 1dB compression (1)	28	29		dBm
P03	Output power at 3dB gain compression (1)	29	30		dBm
IP3	3 rd order intercept point (2)		41		dBm
PAE	Power added efficiency at Psat	12	16		%
VSWRin	Input VSWR (2)			5:1	
VSWRout	Output VSWR (2)			2.5:1	
Tj	Junction temperature for 80°C backside		170		°C
Id	Bias current @ small signal		850	1000	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

(2) Value representative for CW on jig measurement.

Absolute Maximum Ratings

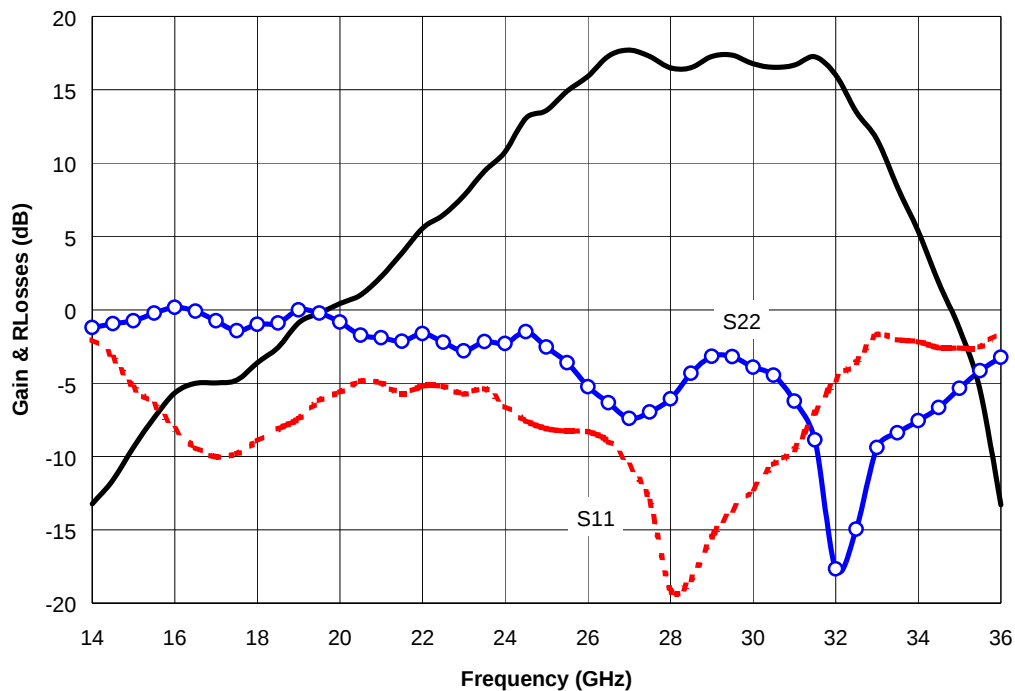
Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.25	V
Id	Drain bias current	1450	mA
Vg	Gate bias voltage	-2.5 to +0.4	V
Vgd	Negative gate drain voltage (= Vg - Vd)	-8	V
Pin	Maximum peak input power overdrive (2)	+18	dBm
Ta	Operating temperature range	-40 to +80	°C
Tstg	Storage temperature range	-55 to +125	°C

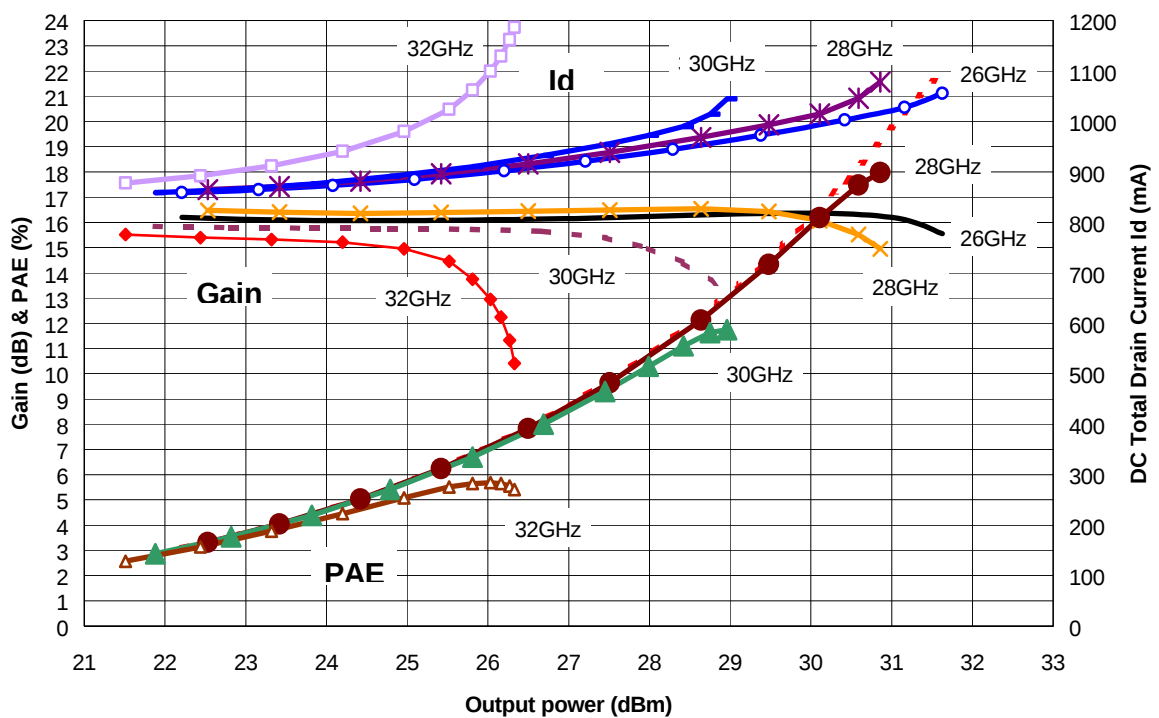
(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Duration < 1s.

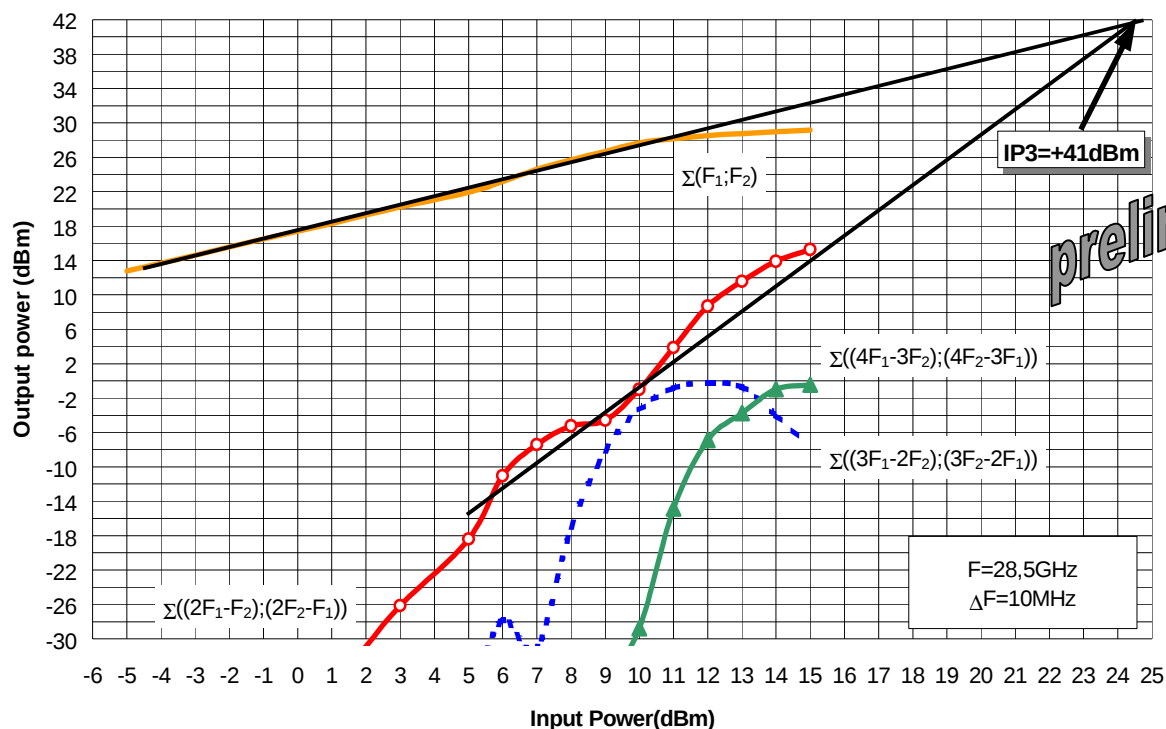
Typical on Jig Measurements

Bias conditions: $V_d=6V$, V_g tuned for $I_d = 850mA$ *preliminary*

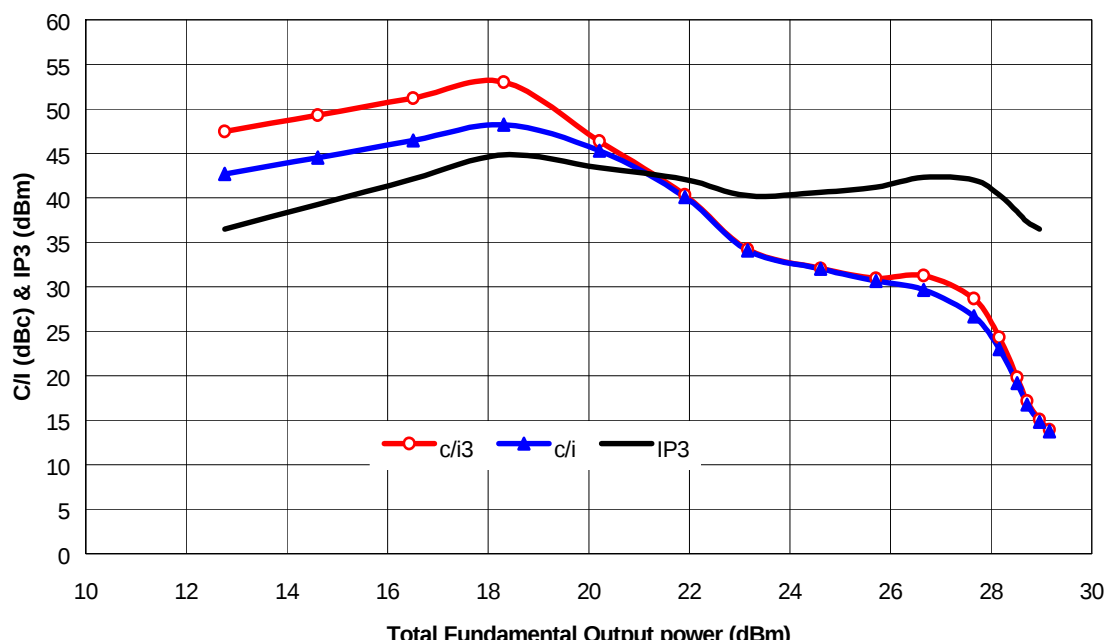
Linear Gain & Return Losses versus frequency



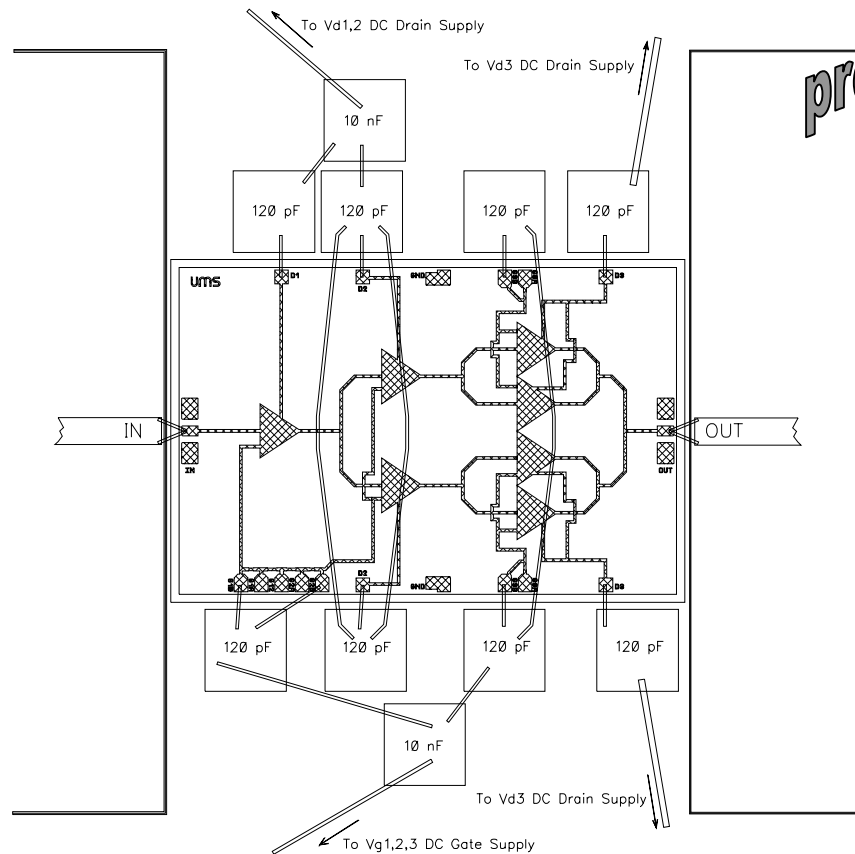
Gain, PAE & DC drain current vs Output power @ different frequencies



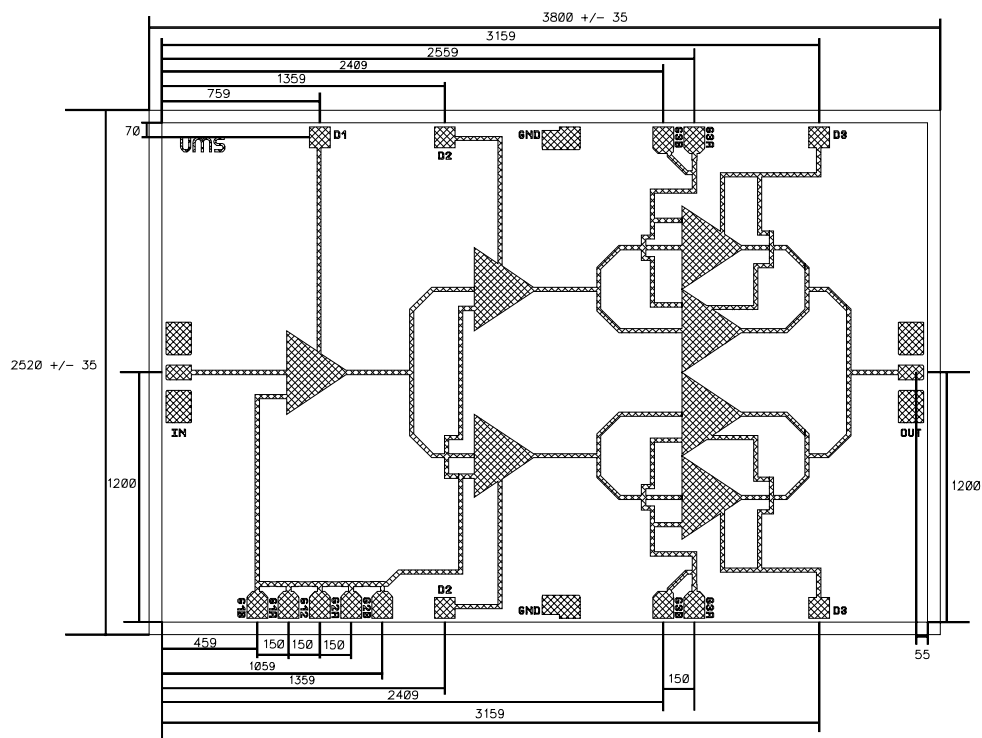
IP3 versus total input power @ 28.5GHz

C/I & IP3 versus total fund. output power @ 28.5GHz ($\Delta F=10\text{MHz}$)

Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25 μ m diameter gold wire is to be preferred.



Bonding pad positions.

(Chip thickness : 50 μ m. All dimensions are in micrometers)

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Application note

Bias operation sequence:

ON: Supply Gate voltage
Supply Drain voltage
OFF: Cut off Drain voltage
Cut off Gate voltage

Due to 50µm thickness, specific care is requested for the handling and assembly.

Ordering Information

Chip form : CHA5296-99F/00

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