FAIRCHILD
SEMICONDUCTOR™

Preliminary
March 2001

FM3565
CPU CONFIGURATION CONTROLLER
Register/Multiplexer for Microprocessor VID

General Description

The Fairchild FM3565 replaces the PC motherboard's CPU configuration switches with an electronic implementation, consisting of a 5-bit multiplexed port, standard 2-wire bus interface, and non-volatile latches with external hardware control.

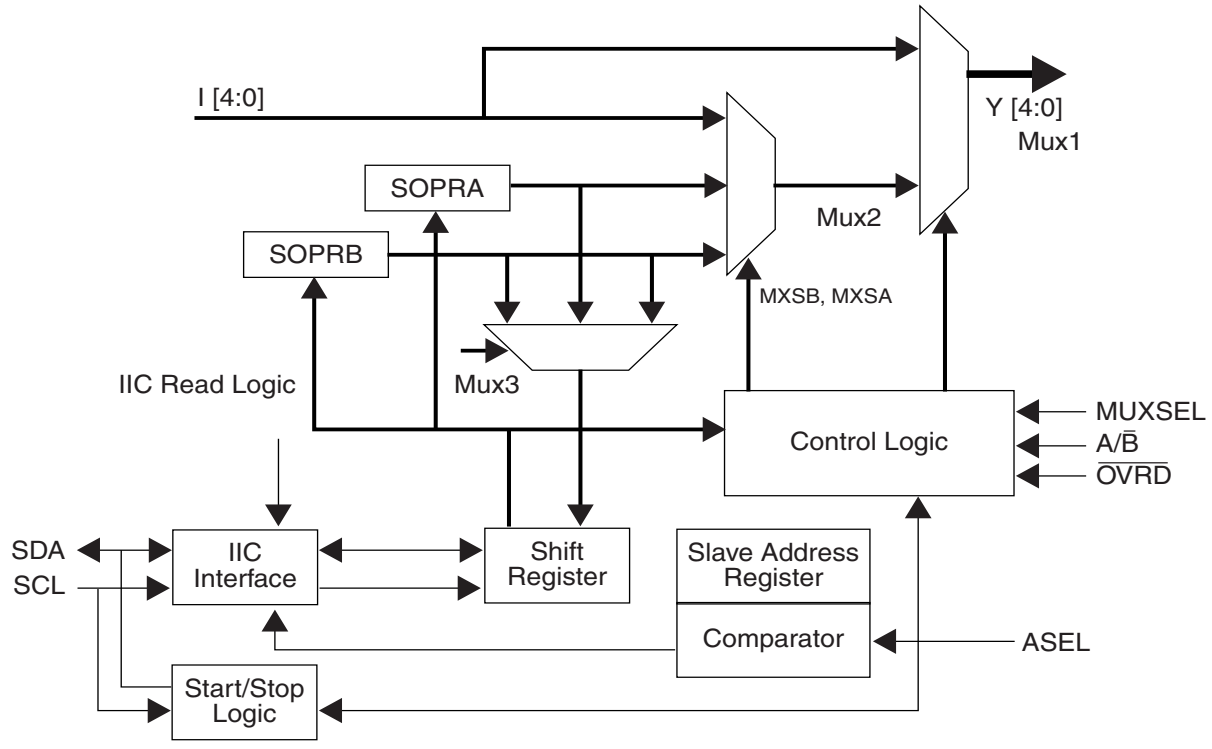
The FM3565 multiplexes the I-port input signals with two internal non-volatile registers that can be loaded through the serial port. The multiplexer output is under hardware control, and is determined by the inputs $\overline{OVRD}$, MUXSEL, and A/$\overline{B}$. Pull-up resistors are provided on the input port to accommodate connections to open drain outputs and to eliminate the need for external resistors. The device has open-drain outputs for easy interface to devices with different V_{DD} Levels.

The serial port is an IIC compatible slave-only interface and supports both 100kbit and 400kbit modes of operation. The port is used to read the I-Port and to write data to the internal non-volatile registers. The FM3565 is fabricated with advanced CMOS technology to achieve high density and low power operation.

Features

- Extended Operating Voltage Range 3.0V-5.5V
- IIC Compatible Slave Interface.
- ESD performance: Human body model > 2000V
- Open-Drain Outputs

Block Diagram



Ordering Code

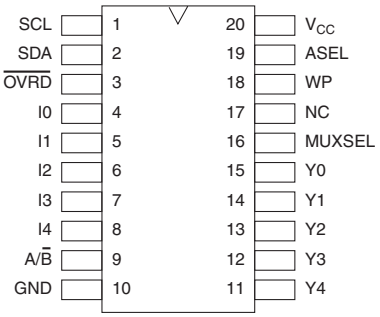
FM 3565 XXXX X

Blank	Tube
X	Tape & Reel
M20	20-Pin SO Package Option
MT20	20-Pin TSSOP Package Option

Order Number	Package Number	Package Description
FM3565MT20	MTC20	20-Pin TSSOP
FM3565MT20X	MTC20	20-Pin TSSOP T & R
FM3565M20	M20B	20 Pin SO
FM3565M20X	M20B	20 Pin SO T & R
For all other combinations, check with Fairchild Marketing/Sales		

Pin Connection Diagram

20-Pin Packages
FM3565



Pin Description

Pin Name	Description
I [0:4]	Data Inputs w/Pullups (10K-40K)
Y [0:4]	Open-Drain Data Outputs
SCL	Serial Port Clock Input (120K pullup)
$\overline{\text{OVRD}}$	Override Input. Sets all outputs to 0
WP	Write Protect Input
NC	No Connect
MUXSEL	Multiplex Select Input
A/$\overline{\text{B}}$	Level Select Input
ASEL	Address Select Input
SDA	Serial Port Data I/O (120K pullup)

Functional Description

The FM3565 block diagram is shown in Figure 1.

Operational Modes

During standard operation, the device will pass data to the Y-Port either from the I-Port or from one of the internally stored Non-Volatile Register values.

The I-port values are generated from the motherboard of the system and may be hardwired or driven by another device. Pull-up resistors are provided on the device to accommodate this device being driven by open-drain output drivers. The device expects standard CMOS input signals. The outputs (Y0-Y4) operate in the open-drain mode. The $\overline{\text{OVRD}}$ (override) input, when set to 0, will cause all the outputs to be set to 0. The WP signal, if set to logic 1, will prevent data from being written to the non-volatile register.

The functioning of this device is described by the truth table in Table 1.

Output Port: Y0-Y4

The output port is an open-drain output to allow for easy connection to devices running at different voltage levels. The port is always active and either passes the value on the I-Port or data from one of the internal non-volatile registers (SOPRA/B). Changing the Mux Path is accomplished using the external hardware controls – $\overline{\text{OVRD}}$, MUXSEL, and A/$\overline{\text{B}}$.

Register Description

The FM3550/60 has 3 registers in total. These registers are made up of a combination of read-only, write-only and read/write bits. The two registers are listed below.

Serial Output Port Register A(SOPRA) Address: 00H - A read/write register that contains the new value of SOPRA.

Serial Output Port Register B(SOPRB) Address: 01H - A read/write register that contains the new value for SOPRB.

Parallel Input Port Register (PIPR) Address: 02H - A read-only register that is loaded with the 5-bit value of the I-Port.

Serial Output Port Register (SOPR)

(Address 000b and 001b)

MXSB	MXSA	Data Field					
0	0	I5	0	I3	I2	I1	I0
b7	b6	b5	b4	b3	b2	B1	b0

b7-b6 - Multiplexer Select Bits (MXSB,MXSA)

00 - Multiplexer passes the SOPR(A).

01 - Multiplexer passer the SOPR(B).

10 - Multiplexer defaults to passing the I-Port Value.

b5, b3-b0 - Data Field. New value to be output through the multiplexer.

Parallel Input Port Register (PIPR)

(Address 002b)

Address Field			Data Field				
0	0	0	I4	I3	I2	I1	I0
b7	b6	b5	b4	b3	b2	B1	b0

b7-b5 - Address field. Value is always 000

b4-b0 - Data Field. Value is equal to the value on the I-Port.

The external Port Register captures the value on the I-Port. Data is latched into this register on the first clock after a start condition is seen. This insures that a valid value will always be in this register if it is read. This register is a-read only register with respect to the IIC port.

$\overline{OVRD}$	MUXSEL	A/$\overline{B}$	Mux_outputs
0	0	X	all 0's
0	1	X	Mux_inputs
1	0	0	From Non-volatile register (SOPRB)
1	0	1	From Non-volatile register (SOPRA)
1	1	X	Mux_inputs

Table 1. Multiplexer Control Options

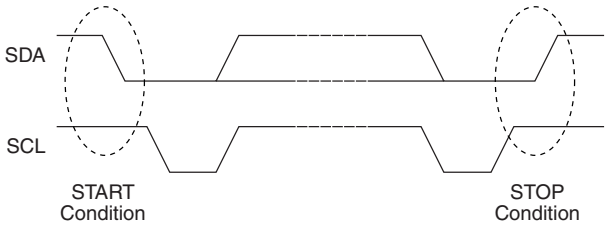
Multiplexer Logic

The output multiplexer logic determines what value is actually output to the Y-port. The above table describes all the combinations.

Serial Interface

The IIC Interface is a standard slave interface. As such, the device will not generate its own clock. Data can be read from and written into the device. Commands for reading and writing the registers are generated by the Master.

START and STOP Conditions



This protocol uniquely defines START and STOP conditions. A START condition is defined as a HIGH to LOW transition of the SDA signal while SCL is HIGH. A STOP condition is defined as a LOW to HIGH transition of the SDA signal while SCL is HIGH. These are shown in Figure 2.

Device Addressing

The device uses 7-bit addressing. The address has been defined as 1001 110 if the ASEL input is '1' and 0110 111 if the ASEL input is '0'. The address byte is the first byte of data sent after a start condition. This is the only address that this device will respond to. The device will not respond to the general call address 0000 000.

Reading from the Registers

Data can be read from both of the internal registers. All reads are non-destructive and do not change the value in the register or the internal state of the device. When a start condition is received with a read request, both registers can be read out in the following sequence:

(1) SOPRA: Serial Output Port Register A

(2) SPORB: Serial Output Port Register B

(3) PIPR: PORT-I Value

If so desired, only the SOPRA register can be read. This is accomplished by issuing a stop command after the acknowledge bit for the first byte is read. If no stop is issued, the device will output the registers in the above sequence.

Writing to the Registers

Data is written to the SOPR registers through the serial port interface. When a write request is received with the Start Address, it is assumed that the intent is to write to the SOPR registers. The value placed in the least 6 significant bits of the register contain the new code to be placed in the SOPR A/B registers. The value of the two most significant bits must contain the address of the destination register SOPRA or SOPRB.

The internal non-volatile latch takes about 10 ms to update its data.

Register Read Sequence

S	Slave Address	R	A	SOPRA Register	A	SOPRB Register	A	PIPR Register	A	P
S	1001110	1	A	00bbbbbb	A	00bbbbbb	A	00bbbbbb	A	P

Register Write Sequence

S	Slave Address	W	A	SOPRx Register	A	S
S	1001110	0	A	xxbbbbbb	A	S

xx = Register Selection bits (MXSB and MXSA) xx = 00 selects SOPRA, 01 selects SOPRB

Register Write Sequence using Repeated Start Condition

S	Slave Address	R	A	SOPRA Register	A	S	Slave Address	W	A	SOPRx Register	A	P
S	1001110	1	A	00bbbbbb	A	S	1001110	0	A	xxbbbbbb	A	P

Figure 4

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +6.5V
DC Input Voltage (V_I)	-0.5V to +6.5V
Output Voltage (V_O)	
Outputs 3-stated	-0.5V to +6.5V
Outputs Active (Note 2)	-0.5 to V_{CC}+0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	-50mA
DC Output Diode Current (I_{OK})	
V_O < 0V	-50mA
V_O > Vcc	+50mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	±100mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	3.0V to 5.5V
Input Voltage	-0.3V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Output Current I_{OL}	3mA
Free Air Operating Temperature(TA)	-0°C to +70°C
Minimum Input Edge Rate (dt/dv)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Floating or unused pins (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics (4.5V < V_{CC} ≤ 5.5V unless stated otherwise)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		V_{CC} x 0.7		V
V_{IL}	Low Level Input Voltage			V_{CC} x 0.3	V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA I_{OL} = 3mA		0.2 0.4	V
I_{IR}	Input Leakage Current	V_I=V_{IL}, V_{CC} = 5.5V	-10	+10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND V_{CC} ≤ (V_I, V_O) ≤ 3.6V	300	975	µA

DC Electrical Characteristics Extended (3.0V ≤ V_{CC} ≤ 5.5V unless stated otherwise)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		V_{CC} x 0.7		V
V_{IL}	Low Level Input Voltage			V_{CC} x 0.3	V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA I_{OL} = 3mA		0.2 0.4	V
V_{OH}	Output High Voltage	Fixed output mode, ('S' grade samples, or FM3560 with LEVEL input = logical '0') 1 TTL load, 50pF capacitance	2.3	2.5	V
I_{IR}	Input Leakage Current	V_I=V_{IL}, V_{CC} = 5.5V	-10	+10	µA
I_{CC}	Quiescent Supply Current	V_{CC} ≤ (V_I, V_O) ≤ 3.6V	300	975	µA

AC Characteristics

Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $C_L = 30pF$, $R_L = 500\Omega$				Units
		$V_{CC} = 5.0V \pm 0.5V$		$V_{CC} = 3.3V \pm 0.3V$		
		Min	Max	Min	Max	
t_{PHL}	Prop Delay I to Y		50		50	ns
t_{PLH}	Prop Delay I to Y		50		50	ns
t_{PHL}	Prop Delay to Y (from $\overline{OVRD}$ or MUXSEL)		50		50	ns
t_{PLH}	Prop Delay to Y (from $\overline{OVRD}$ or MUXSEL)		50		50	ns

IIC AC Characteristics

Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $C_L = 30pF$, $R_L = 500\Omega$				Units
		100kHz		400kHz		
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_1	Noise Supression Time Constant		100		50	nS
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µS
t_{BUF}	Time the Bus must be free before a new Transmission can start	4.7		1.3		µS
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µS
t_{LOW}	Clock Low Period	4.7		0.6		µS
t_{HIGH}	Clock High Period	4.0		0.6		µS
$t_{SU:STA}$	Start Condition Setup Time (For a repeated Start Condition)	4.7		0.6		
$t_{HD:DAT}$	Data in Hold Time	0		0		µS
$t_{SU:DAT}$	Data in Setup Time	250		100		nS
t_R	SDA and SCL Rise Time		1000		300	nS
t_F	SDA and SCL Fall Time		300		300	nS
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µS

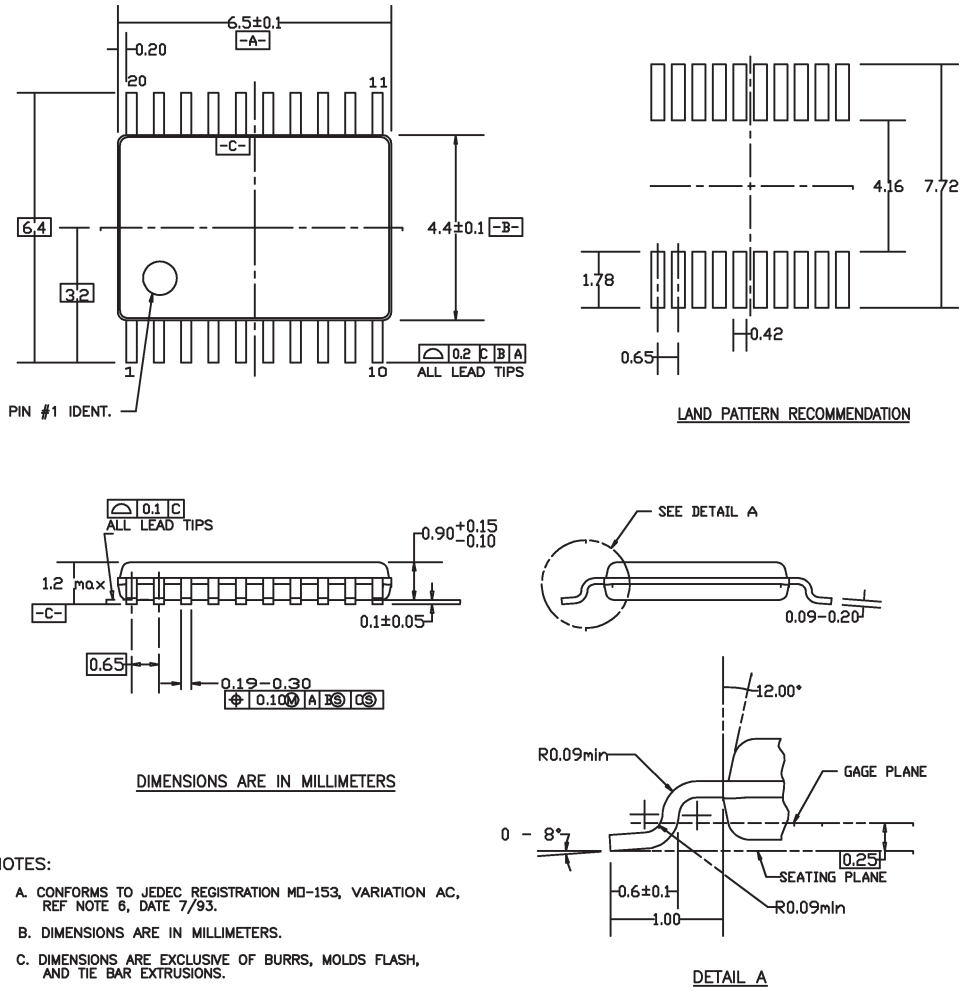
Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance (I4-I0)	V_I =0V or V_{CC}, V_{CC}=3.3 or 5.0	6	pF
$C_{I/O}$	Input/Output Capacitance (SDA)	V_I=0V or V_{CC}, V_{CC}=3.3 or 5.0	7	pF
C_{OUT}	Output Capacitance (Y4-Y0)		7	pF

Non-Volatile Memory Characteristics

Parameter	Specification
Data Retention	10 years minimum
Number of writes	1,000,000 cycles

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

Order Number FM3565MT
Package Number MTC20

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Americas
Customer Response Center
Tel. 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +44 (0) 1793-856858
Deutsch Tel: +49 (0) 8141-6102-0
English Tel: +44 (0) 1793-856856
Français Tel: +33 (0) 1-6930-3696
Italiano Tel: +39 (0) 2-249111-1

Fairchild Semiconductor Hong Kong
8/F, Room 808, Empire Centre
68 Mody Road, Tsimshatsui East
Kowloon. Hong Kong
Tel; +852-2722-8338
Fax: +852-2722-8383

Fairchild Semiconductor Japan Ltd.
4F, Natsume Bldg.
2-18-6, Yushima, Bunkyo-ku
Tokyo, 113-0034 Japan
Tel: 81-3-3818-8840
Fax: 81-3-3818-8841