TEXAS INSTRUMENTS

TSB42AA9/TSB42AA9I

StorageLynx 1394 Link-Layer Controller for ATA/ATAPI Storage Products

Data Manual

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1 Introduction

1.1 Description

The Texas Instruments TSB42AA9 (StorageLynx) is a 1394 Link Layer Controller designed to function as a native bridge between the 1394 bus and ATA (AT Attachment) or ATAPI (AT Attachment with Packet Interface) data storage applications. These data storage devices can include external hard disk drives (HDDs), ZIP drives, magneto-optical (MO) drives, ORB drives, CD-ROMs, CD-R/Ws, DVD-ROMs, and DVD-RAMs. The ATA/ATAPI interface of the TSB42AA9 supports signaling and timing for programmed input/output (PIO) modes 0–4, direct memory access (DMA) modes 0–2, and Ultra DMA modes 0–4. The 1394 interface of StorageLynx is IEEE P1394a[1] and IEEE Std 1394-1995[2] compliant, and it supports 400, 200, and 100 Mbps serial bus data rates.

StorageLynx is particularly designed for any data storage application that supports the SBP–2[3] (Serial Bus Protocol 2) transaction layer as a target device. The TSB42AA9 automates the SBP-2 target controller functions by implementing the management and command agents in hardware. Data handling is also executed in hardware, with no assistance from the processor needed to setup a DMA transaction to fetch data from the ATA/ATAPI device and return it to the SBP-2 initiator via the 1394 bus. StorageLynx translates SBP-2 protocol commands to ATA/ATAPI commands using the hardware-implemented functions and an embedded 8052 processor executing firmware. The firmware is located in the internal ROM of the device or optionally, an external memory location.

A 2-wire serial bus interface is included on the TSB42AA9. This interface enables configuration ROM information required by IEEE Std 1394-1995[2] and SBP-2 to be loaded from a serial EEPROM into the device's internal parameter RAM. The internal parameter RAM allows StorageLynx faster access to important configuration information as well as automatic responses to configuration ROM read requests from the system host. In addition, StorageLynx provides a memory interface which can be used to access firmware from an external Flash PROM/EPROM for testing and development purposes, or to support storage applications which require specialized functionality. The StorageLynx memory interface also supports write operations to the Flash PROM/EPROM, removing the need for parts to be in sockets and allowing for easy software downloads. Flash memory is not required unless custom functionality and in-system reprogrammability are requirements.

1.2 Features

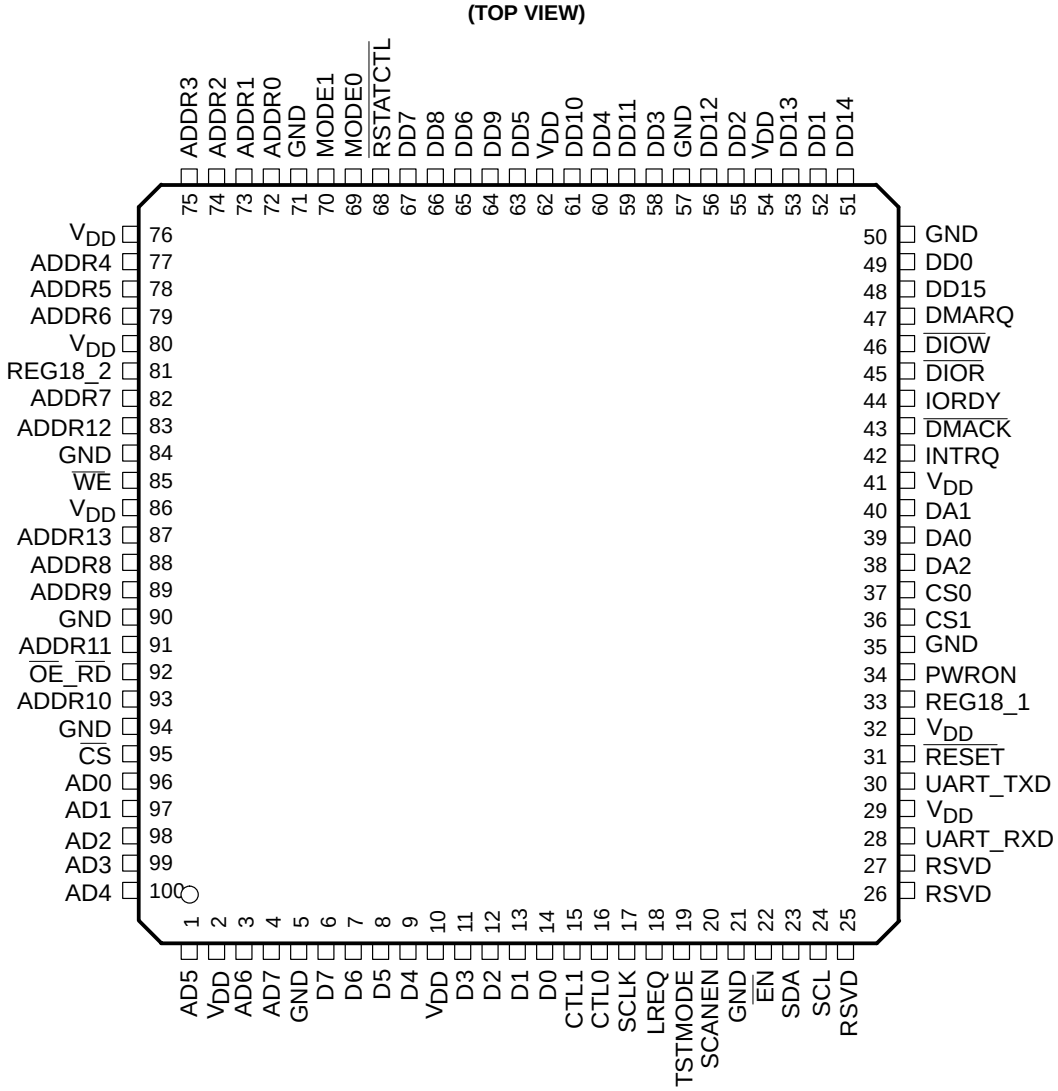
- Serial bus data rates of 100, 200, and 400 Mbps
- IEEE P1394a compliant and IEEE Std 1394-1995
- Automated SBP-2 transport protocol engine
- ATA/ATAPI command translation by embedded processor and firmware
- Programmable ATA/ATAPI interface supporting PIO modes 0–4, DMA modes 0–2, and Ultra DMA modes 0–4
- Automated 1394 and SBP-2 header removal and insertion
- Internal parameter RAM for fast access to configuration ROM and key SBP-2 parameters
- Automatic response to configuration ROM quadlet and block read requests
- External flash PROM / EPROM interface for easy program code changes during prototyping
- Separate address and data busses for the external flash PROM / EPROM interface (no external latches)
- 16K internal ROM program memory
- 576 Byte (128 quadlet) transmit control FIFO, 576 byte (128 quadlet) receive control FIFO
- Bidirectional data FIFO
- 0.18 micron CMOS technology with embedded RAM and ROM
- Space-saving 100 pin TQFP package

1.3 Related Documents

- TSB42AA9 (StorageLynx) *EVM User's Guide* (literature number SLLU017)
- IEEE P1394a, *Draft Standard for a HIgh Performance Serial Bus* (Supplement)
- T10 Project 1155D, ANSI NCTIS.xxx-199x, *Serial Bus Protocol 2 (SBP-2)*
- NCITS T10 1240D, *Reduced Block Commands Revision 10 (RBC)*
- American National Standards Institute, ANSI NCITS 317-1998, *AT Attachment with Packet Interface Extension—(ATA/ATAPI-5 v3.0)*

1.4 Terminal Assignments/Package

TSB42AA9
PZT PACKAGE
(TOP VIEW)



1.5 Terminal Descriptions

The terminal descriptions in this section are grouped by functionality with the package pin numbers added for reference. The following conventions are used in the tables: signals with overbar denote an active low signal; (I) denotes an input; (O) denotes an output; (I/O) denotes a 3-state input and output.

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
POWER			
GND	5, 21, 35, 50, 57, 71, 84, 90, 94	I	Device ground terminals
V_{DD}	2, 10, 29, 32, 41, 54, 62, 76, 80, 86	I	3.3V power supply terminals
REG18_1, REG18_2	33, 81	O	Regulates the 3.3 V supply for core 1.8 V. These pins should be tied to GND through 0.1 µF decoupling capacitors.
$\overline{EN}$	22	I	Enable for 1.8 V regulators (active low). This pin should be tied to GND during normal operation.
$\overline{RESET}$	31	I	Power-on reset input (active low).
ATA/ATAPI INTERFACE			
DD[15:0]	48, 51, 53, 56, 59, 61, 64, 66, 67, 65, 63, 60, 58, 55, 52, 49	I/O	Host-device data bus. This is an 8- or 16-bit bidirectional data interface between the host and the storage device. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16-bits wide. DD15 is the most significant bit.
DA[2:0]	38, 40, 39	O	Device address 0 to 2. This is the 3-bit binary coded address asserted by the host to access a register or data port in the storage device.
$\overline{CS0}$	37	O	Chip select 0 (active low). This chip select signal is used by the host to select the command block registers in the ATA controller in the storage device.
$\overline{CS1}$	36	O	Chip select 1 (active low). This chip select signal is used by the host to select the command block registers in the ATA controller.
INTRQ	42	I	Interrupt request. This signal is used by the ATA controller in the storage device to interrupt its host system. INTRQ is asserted only when the controller has a pending interrupt.
$\overline{DMACK}$	43	O	DMA acknowledge (active low). This signal from the host handshakes with the DMARQ for the DMA transfers.
DMARQ	47	I	DMA request. This signal, used for DMA data transfers between host and storage device, is asserted by the ATA controller in the device when it is ready to transfer data to or from the host. This signal is released (high impedance state) whenever the device is not selected or is selected and no DMA command is in progress.
$\overline{IORDY}$ ($\overline{DDMARDY}$, DSTROBE)	44	I	I/O ready. This signal is negated to extend the transfer cycle of any host ATA register access (read or write) when the ATA controller is not ready to respond to a data transfer request. The use of IORDY is required for PIO modes 3 and above, and otherwise is optional. (Ultra DMA ready (active low). This signal is a flow control for Ultra DMA data out bursts. It is asserted by the ATA device to indicate to the host that the device is ready to receive Ultra DMA data out bursts. Ultra DMA data strobe. This signal is the data in strobe from the device for an Ultra DMA data in burst.)
$\overline{DIOR}$ ($\overline{HDMARDY}$, HSTROBE)	45	O	Read strobe signal (active low). The falling edge of $\overline{DIOR}$ enables data from the ATA device onto the signals, DD (7:0) or DD (15:0). The rising edge of $\overline{DIOR}$ latches data into the device. The device does not act on the data until it is latched. The direction of data (16 bits) transfer is controlled by $\overline{DIOR}$ and $\overline{DIOW}$. (Ultra DMA ready (active low). This is a flow control signal for ultra DMA in bursts. It is asserted by the host to indicate to the device that the host is ready to receive ultra DMA data in bursts. Ultra DMA data strobe. This is the data out strobe from the host for an ultra DMA data out burst.)
$\overline{DIOW}$ (STOP)	46	O	Write strobe signal (active low). The rising edge of $\overline{DIOW}$ latches data from the signals, DD (7:0) or DD (15:0), into the ATA device. The ATA device does not act on the data until it is latched. The direction of data (16 bits) transfer is controlled by $\overline{DIOR}$ and $\overline{DIOW}$. (Stop ultra DMA burst. This signal is negated by the host prior to initiation of an ultra DMA burst.)
$\overline{RSTATCTL}$	68	O	Reset ATA controller (active low). This output allows the host to asynchronously reset the ATA controller of the device.

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PHY INTERFACE			
CTL1, CTL0	15, 16	I/O	PHY-link control bus. CTL1 and CTL0 indicate the four operations that can occur on this interface (see Annex J of the IEEE 1394-1995 standard[2] for more information about the four operations).
D7 – D0	6, 7, 8, 9, 11, 12, 13, 14	I/O	PHY-link data bus. Data is expected on D0–1 for 100 Mb/s packets, D0–D3 for 200 Mb/s, and D0–D7 for 400 Mb/s. D0 is the most significant bit.
LREQ	18	O	Link request. LREQ is an output that makes bus requests and register access requests to the PHY.
SCLK	17	I	System clock. SCLK is a 49.152-MHz clock supplied by the PHY±100 ppm.
FLASH PROM/EPROM INTERFACE			
ADDR[13:0]	87, 83, 91, 93, 89, 88, 82, 79, 78, 77, 75, 74, 73, 72	O	Flash PROM/EPROM address bus. ADDR is a 14-bit address bus between StorageLynx and its (optional) external memory. ADDR13 is the most significant bit.
AD[7:0]	4, 3, 1, 100, 99, 98, 97, 96	I/O	Flash PROM/EPROM data bus. AD is a birdirectional 8-bit data bus between StorageLynx and its (optional) external memory. AD7 is the most significant bit.
$\overline{CS}$	95	O	Flash PROM/EPROM chip enable (active low). $\overline{CS}$ is the external memory chip enable.
$\overline{OE}\_\overline{RD}$	92	O	Flash PROM/EPROM output enable (active low). $\overline{OE}\_\overline{RD}$ is the external memory output enable.
$\overline{WE}$	85	O	Flash PROM/EPROM write enable (active low). $\overline{WE}$ is the external memory write enable. During normal operation this signal is asserted high.
2-wire Serial Bus			
SDA	23	I/O	Serial Data. SDA is the data interface for the serial EEPROM. SDA should be pulled up with a 10K resistor at the serial EEPROM.
SCL	24	O	Serial Clock. SCL provides serial clock signaling. 100 kHz (Nclk/256) for serial EEPROM.
RESERVED			
RSVD	25, 26, 27		Reserved. Test Signals
MISCELLANEOUS			
UART_RXD	28	I	UART RXD. Mux-selectable input. On power up, this signal is sampled to set the embedded processor clock speed setting. A detected logic high sets the internal clock to 50 MHz (pull-up through a 10K resistor). A logic low sets the clock to 25 MHz (pull down through a 1K resistor).
UART_TXD	30	O	UART TXD. Mux-selectable output.
MODE0	69	I	MODE0. This signal is device configuration select 0. See Table 2–4.
MODE1	70	I	MODE1. This signal is device configuration select 1. See Table 2–4.
PWRON	34	O	Power on. This signal is asserted on power up. PWRON is negated when an SBP–2 logout occurs. This signal can also be used as a general-purpose output.
TSTMODE	19	I	Test mode select. Tie to GND during normal operation.
SCANEN	20	I	Test mode scan enable. Tie to GND during normal operation.

1.6 Chapter References

1. IEEE P1394a, *Draft Standard for a High Performance Serial Bus* (Supplement)
2. IEEE Std 1394–1995, *Standard for a High Performance Serial Bus*
3. T10 Project 1155D, ANSI NCTIS.xxx-199x, *Serial Bus Protocol 2 (SBP-2)*

2 Detailed Description

TASB42AA9 comprises:

- IEEE P1394a Compliant Link Core
- Receive Packet Router
- Transmit Packetizer
- SBP–2 Transport Protocol Engine
- FIFOs (Control Tx/Rx and Data)
- Embedded 8052 Processor
- Internal ROM (16K × 8)
- Configuration ROM Registers (Parameter RAM)
- ATA/ATAPI Interface
- Flash PROM/EPROM Interface
- 2-wire Serial EEPROM Bus Interface

2.1 Functional Block Diagram

The functional block architecture of TSB42AA9 is shown in Figure 2–1.

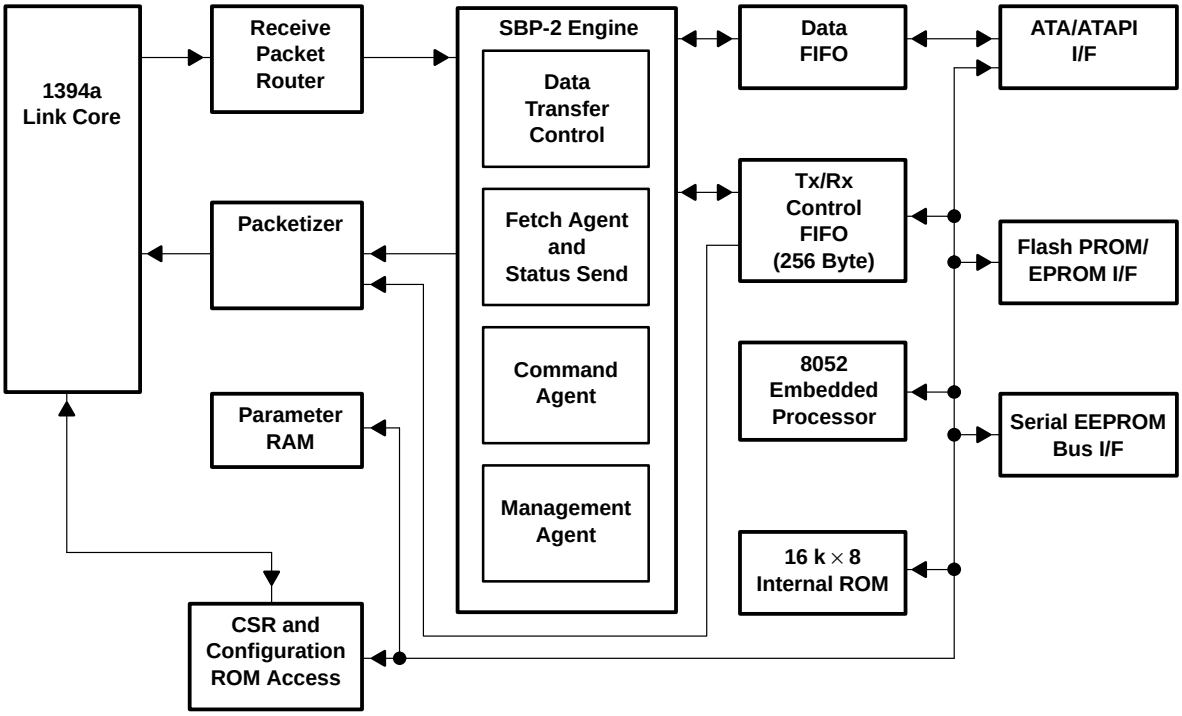


Figure 2–1. StorageLynx Block Diagram

2.2 Functional Block Descriptions

2.2.1 IEEE 1394a Link Core

The TSB42AA9 contains an IEEE P1394a compatible link core. The link layer is the protocol layer responsible for the interface between the transaction layer and physical layers for asynchronous transactions. The link core

communicates with a 1394 PHY at speeds of 100, 200, or 400 Mbps by transmitting and receiving IEEE 1394–1995/P1394a serial bus packets. The link core builds packets during transmission and generates the cyclic redundancy check (CRC) values. During packet reception, the link core decodes packets and performs data checking. StorageLynx is not required to contend for Bus Manager, Cycle Master, or Isochronous Resource Manager (IRM) on the 1394 bus because it does not support isochronous transactions.

The StorageLynx link core implements the minimum control and status registers (CSR) necessary for an SBP–2 target device. The CSRs are arranged by the core registers required by ISO/IEC 13213:1994[1], the bus dependent registers required by 1394–1995 standard[2]/P1394a standard[1], and the unit architecture registers required by the SBP–2 protocol standard[4]. Table 2–1 depicts the locations and functions of the core registers. The start address location of the initial register space is FFFF F000 0000h offset from the initial node space.

Table 2–1. CSR Registers

OFFSET	REGISTER NAME	DESCRIPTION
000h	STATE_CLEAR	State and control information
004h	STATE_SET	Sets STATE_CLEAR bits
008h	NODE_IDS	Specifies 16 bit node_ID of the node
00Ch	RESET_START	Resets the node's state
018–01Ch	SPLIT_TIMEOUT	Time limit for split transactions
200h	CYCLE_TIME	Maintains cycle time for isochronous transactions (not supported).
210h	BUSY_TIMEOUT	Controls transaction layer retries
218h	PRIORITY_BUDGET	Controls asynchronous priority arbitration

Also included in Table 2–1 are the bus-dependant registers described by the 1394–1995/P1394a standards for a target device, these registers are the CYCLE_TIME, BUSY_TIMEOUT, and PRIORITY_BUDGET registers. The StorageLynx link core supplements the PRIORITY_BUDGET register to the minimum CSR.

The PRIORITY_BUDGET register is implemented because the 1394a specification allows nodes that are transmitting asynchronous packets to arbitrate for the bus more than once during a fairness interval (cycle). This means that StorageLynx can arbitrate for the 1394 bus more often and thus transmit more asynchronous packets increasing data throughput. The pri_max field of the PRIORITY_BUDGET register shown in Figure 2–2 defines the maximum number of asynchronous priority requests that can be performed by StorageLynx per fairness interval. It is read only (Default = 3Fh). The pri_req field defines the current number of additional asynchronous priority requests that can be attempted during the present fairness interval. The bus manager node is responsible for reading the value of the pri_req field. See the IEEE 1394–1995 standard, 1394a standard, and CSR architecture descriptions of the link core and 1394 protocol for more detail on arbitration enhancements.

Format

31–14	13–08	07–06	05–00

Definition

Reserved	Pri_max	r	Pri_req

Initial values

Zeros	Value	r	Zeros

Read effects

Zeros	Value	Z	Undefined

Write effects

Ignored	Stored

Figure 2–2. PRIORITY_BUDGET Register

2.2.2 Receive Packet Router

The receive packet router examines the header information of received 1394 packets to determine their destination (see Table 2–2). The Destination_ID in the header contains a combination of the 1394 bus address and the physical ID of StorageLynx. The Destination_Offset specifies the address location within the TSB42AA9 that is being accessed. The Source_ID identifies the 1394 node that is sending the packet. During SBP–2 operation, request and response packets are routed to the correct agent/FIFO by decoding the header information, specifically the Source_ID field or the Destination_ID and Destination_Offset fields. The Tlabel field of a request packet is used to route its corresponding response packet. A Tlabel is a transaction label that is specified by a node sending a request. This same value is then returned to the node in the response packet sent by StorageLynx.

Table 2–2. General Asynchronous Request Header Format

31–24	23–16	15–08		07–00	
Destination ID		Tlabel	RT	Tcode	Priority
Source ID		Destination_Offset			
Destination_Offset					
Packet Type–Specific Data					
Header CRC					

FIELD NAME	DESCRIPTION
Destination ID	Destination ID – Contains the address of the target node.
Tlabel	Transaction Label– A label specified by the requester that identifies this transaction.
RT	Retry Code – This code specifies whether this packet is an attempted retry and defines the retry protocol to be used.
Tcode	Transaction Code – Identifies type of request being made.
Priority	Not used.
Source ID	Source ID – Identifies the node that is sending this packet.
Destination_Offset	Destination Offset – Specifies the address location within the target node that is being accessed.
Header CRC	Header CRC – CRC value for the header.

Table 2–3. General Asynchronous Response Header Format

31–24	23–16	15–08		07–00	
Destination ID		Tlabel	RT	Tcode	Priority
Source ID		Rcode	Reserved		
Reserved					
Packet Type–Specific Data					
Header CRC					

FIELD NAME	DESCRIPTION
Destination ID	Destination ID – Contains the address of the node receiving the packet.
Tlabel	Transaction Label– Contains the value sent by the requester for this transaction.
RT	Retry Code – This code specifies whether this packet is an attempted retry and defines the retry protocol to be used.
Tcode	Transaction Code – Identifies type of response being made.
Priority	Not used.
Source ID	Source ID – Identifies the node that is sending this packet.
Rcode	Response Code – Specifies the result of this transaction.
Header CRC	Header CRC – CRC value for the header.

2.2.3 Transmit Packetizer

The transmit packetizer provides automated packetization services for 1394 transmit packets. The outgoing data stream from the Data FIFO is transmitted in packets with appropriate header information provided by the packetizer.

The destination address (Destination_ID and Destination_Offset) is incremented based on the size of the data payload sent in the previous packet, so the next packet destination address is correct. The packetizer also provides transaction control services that control packet transmission priority between packets in the Control FIFO and in the Data FIFO. It also controls split transaction management and busy retry. If an acknowledge packet with a busy code is received by StorageLynx, the packetizer is responsible for resending the packet until the packet succeeds or the retry limit is reached.

2.2.4 SBP-2 Transport Protocol Engine

Serial Bus Protocol 2 (SBP-2) is a transport protocol that defines the means for communicating commands sourced by a device connected to the serial bus (initiator) to other devices on the serial bus (targets). SBP-2 also defines the means required for the transfer of data or status associated with these commands. StorageLynx is designed to provide the SBP-2 protocol required by a target device. StorageLynx accelerates much of the SBP-2 protocol by implementing it in hardware. This hardwired functionality is distributed in the StorageLynx architecture to affect SBP–2 acceleration of management, command, and data movement during respective phases of operation. The TSB42AA9 is not designed to provide SBP-2 initiator services.

A target agent is the part of the SBP-2 Engine that receives signals that indicate when an initiator has a command ready. There are two types of target agent; one that can process one command at a time, and one that can manage linked lists of commands. In the first case, the initiator signals the command to the agent by means of a block write request with the address of the command. In the other case, the initiator adds new commands to an active list and rings a doorbell that causes the agent to fetch another command from the system memory. These two types of target agents are known respectively as the management agent and the command block agent.

2.2.4.1 Management Agent

The management agent can accept various types of requests (commands) from an initiator node such as: login, task management, and logout. The first request an initiator makes is always a login request. After the initiator completes a login, the management agent can accept task management requests from the initiator. Ultimately, the initiator will generate a logout command to release the target. Management agents service a single request at a time.

The initiator node processes a request by writing the address of the management operation request block (ORB) containing the request to the pointer register of the management agent. The target then fetches the ORB by reading it over the 1394 bus and stores it in the management ORB registers where it is processed. Whenever the management agent register is written to, the management agent reads and fetches ORBs automatically.

The management agent register location is specified in the configuration ROM. The StorageLynx management agent register base address is offset by 10000h from the initial CSR space at FFFF_F000_0000h. All management agent ORBs are 32-byte data structures written to the register at FFFF_F001_0000h. The management agent is also responsible for storing management information as outlined in the SBP–2 protocol[1].

The management agent supported in the hardware of the TSB42AA9 can process the following types of management ORB requests:

- Login
- Query Login
- Reconnect
- Set Password
- Logout
- Abort Task Set
- Target Reset

2.2.4.2 Command Agent

A successful login request to the management agent of StorageLynx returns the address of the command block agent. Command block agents service command block ORBs that are structured in the form of a linked list or a page table. Command ORBs are used to encapsulate data transfer or device control commands from the initiator for transmission to the target device. A target system's command set and device type determine the size of the ORBs. This size is reported in the StorageLynx (target) configuration ROM.

The command agent of StorageLynx also implements CSRs as shown in Table 2–4 at a predefined offset that is reported by the target device during the login processed by the management agent. The command agent location is FFFF_F001_0020h, which is 32 bytes above the location of the management agent. See the SBP-2 protocol[1] for more detail on the command agent responsibilities.

Table 2–4. Command Agent Registers

RELATIVE OFFSET	NAME	DESCRIPTION
00h	AGENT_STATE	Reports command (fetch) agent state
04h	AGENT_RESET	Resets command agent
08h	ORB_POINTER	Address of ORB
10h	DOORBELL	Signals command agent to refetch an address pointer
14h	UNSOLICITED_STATUS_ENABLE	Acknowledges the initiator's receipt of unsolicited status
18h–1Ch		Reserved

2.2.4.3 Data Transfer Control

The data transfer control block is responsible for moving large blocks of data between the initiator (host) and target (storage) devices. The data block also performs the buffer management functions at the ATA/ATAPI (target) interface. Buffer management includes controlling buffer direction (Tx or Rx) and packet sizes, filling and emptying the buffer without overflow or underflow, and detecting errors. It is responsible for managing the size and number of read / write transactions necessary to transfer all the requested data since data block lengths may be larger than the maximum data payload that can be accommodated in a single transaction. The data control block may choose any appropriate size for the data transfer transactions subject to alignment, speed, and data payload length constraints specified by the command ORB that requested the data. Refer to the SBP-2 protocol[1] for more detail on the data transfer control block responsibilities.

2.2.5 FIFO

The StorageLynx FIFO is partitioned according to the type of information it contains. Separate storage for control (management / command) and data is provided. The FIFO also provides a packet buffer for data exchange between the attached ATA/ATAPI device and the 1394 serial bus.

2.2.5.1 Data FIFO

The data FIFO is used for the transfer of data to/from the ATA/ATAPI interface. The data FIFO provides sufficient storage for two maximum size asynchronous packets at the maximum bus speed of 400 Mbps. The data movement direction determines whether the FIFO is a transmit or a receive FIFO.

2.2.5.2 Control FIFO

The control FIFO is used for the transfer of the commands to the embedded processor. The FIFO is partitioned with a fixed size transmit FIFO and receive FIFO. The embedded processor reads the Rx FIFO, also known as the general receive FIFO (GRF), through a dedicated CFR address (see section 3.2.22). Reading all four byte addresses stored in the register causes new data to be pulled from the receive FIFO and become available for reading. Two accesses to a single byte address in the Rx FIFO CFR address range can also cause a new quadlet to be fetched from the Rx FIFO. The embedded processor can write the Tx FIFO, also known as the asynchronous transmit FIFO (ATF),

through a dedicated CFR address (see section 3.2.19, Control Transmit FIFO: First and Continue Register). Writing all four byte addresses in the register causes more data to be queued into the Tx FIFO. Two write accesses to a byte address in the Tx FIFO CFR address also causes a new quadlet to be queued to the Tx FIFO with the unwritten bytes defaulting to zeroes.

2.2.6 Embedded 8052 Processor

A high performance 8-bit 8052-type microcontroller, onboard the StorageLynx, performs RBC to ATA command translation. The firmware also pulls ATAPI commands from the receive FIFO and loads them into the ATAPI device taskfile registers (see section 3.2.14, Taskfile (0) Register). The embedded processor usually executes the program code contained in the on-chip internal ROM, but it can also execute customized program code stored in an external memory by switching the mode (see Table 2–5.). See the MacroWare Library description of the M8052 MegaMacro Design[2] for more information on the embedded processor.

The speed of the embedded processor can be customized. The UART_RXD terminal is sampled at power up to select the embedded processor clock speed setting. When the signal is detected logic high, the internal clock is set to 50 MHz. A logic low on the UART_RXD pin sets the processor clock to 25 MHz. The TSB42AA9 should be run at 50 MHz if an ATA device is attached, and at 25 MHz for an ATAPI device. Also, while optimal performance for ATA devices is obtained at 50 MHz, running the processor at 25 MHz (to accommodate slower flash memory devices) only causes a slight degradation in speed performance.

2.2.7 Internal ROM

StorageLynx contains on-board mask ROM of 16K to store program code for the embedded processor. This ROM is written during production and cannot be rewritten.

2.2.8 Configuration ROM Fast Access Storage (Parameter RAM)

At power up some of the configuration ROM information required for implementation of a SBP-2 serial bus node is copied from external memory and written to the on-chip parameter RAM (internal configuration storage space). The configuration ROM stored in the EEPROM is accessed through the 2-wire serial bus interface and copied to the internal configuration storage space. The internal storage of configuration ROM information allows the device faster access to important configuration information as well as automatic responses to some read requests from the system host.

Both internal and external configuration storage spaces remain accessible to the embedded processor through the parameter access register @68h (see section 3.2.25) while StorageLynx is powered up. Read requests to a configuration ROM address outside of the data stored in the internal parameter RAM are routed through the 2-wire serial bus.

2.2.9 ATA/ATAPI Interface

The ATA/ATAPI interface is responsible for movement of data between the ATA/ATAPI storage device and the data FIFO of StorageLynx. The StorageLynx firmware performs ATA command and status translation using the reduced block command (RBC)[3] set for ATA devices. However, the StorageLynx firmware acts mainly as a pass through for ATAPI devices pulling commands from the receive FIFO and loading the ATAPI device taskfile registers (see section 3.2.14). The ATA/ATAPI interface block hardware is responsible for transferring the ATAPI packets by generating PACKET commands.

The ATA/ATAPI interface meets the critical timing requirements for the PIO 0-4, DMA 0-2, and Ultra DMA 0-4 modes defined in the ATA/ATAPI-5 v3.0 spec[4]. The ATA/ATAPI interface terminals are all 5-Volt tolerant and 5-Volt failsafe, which means that StorageLynx can interface with an ATA/ATAPI device that is running the ATA/ATAPI interface at 5 Volts without damage, even if StorageLynx is powered down.

2.2.10 Flash PROM/EPROM Interface

The Flash PROM/EPROM interface allows the embedded processor to execute external program code instead of the internal program code. This capability is useful for system debugging and testing purposes. This external memory

option can also be used to support custom commands and functionality desirable in storage applications. Sockets for parts are not needed because the memory interface also supports writes to the flash PROM/EPROM (even to blank devices), allowing for easy software downloads via the 1394 bus. An external flash memory can be used in applications where in-system reprogrammability is a requirement.

2.2.11 2-Wire Serial EEPROM Bus Interface

The 2-wire serial bus interface allows configuration ROM (see section 4) information stored in an external serial EEPROM to be loaded into the StorageLynx parameter RAM to allow quicker responses to configuration ROM read requests from the system host and faster access to device parameters. On power-up, the logic stored in the serial EEPROM is loaded into parameter RAM via the 2-wire serial bus interface. The configuration ROM logic in the external serial EEPROM is also accessible to the embedded processor through the 2-wire serial bus. This 2-wire interface also allows changes and updates to be made easily to the configuration ROM information using the StorageLynx programming application via the 1394 bus, thus removing the need for preprogrammed and socketed parts. The TSB42AA9 also supports writes to blank serial EEPROMs.

2.3 Operational Modes

StorageLynx supports two separate modes of operation shown in Table 2–4. The MODE0 and MODE1 signals are used to configure the mode of the device. These two signals must always be driven to just one state and cannot be dynamically switched during operation. Figures 2–3, 2–4, and 2–5 show block diagrams for each of the modes.

Table 2–5. Operational Modes

MODE	MODE [0:1]	DESCRIPTION
0	00	ATA/ATAPI bridge mode 1. The embedded 8052 processor is enabled and executes program code loaded in the internal Program ROM. StorageLynx can be in either ATA or ATAPI mode, depending on the setting of bit ATP at Register 28h. This register setting may be overwritten by the firmware after accessing the external device to check its device type.
1	01	ATA/ATAPI bridge mode 2 (development mode). The embedded 8052 processor is enabled and executes program code loaded in external Flash PROM/EPROM. The internal ROM is disabled. StorageLynx is in either ATA or ATAPI mode, depending on the setting of bit ATP at Register 28h. This register setting may be overwritten by the firmware after accessing the external device to check its device type.
2-3		Reserved

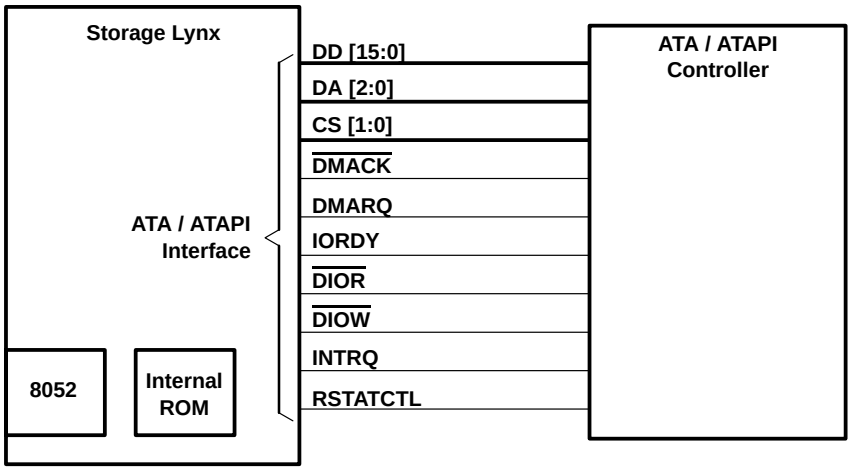


Figure 2–3. Mode 0, ATA/ATAPI Bridge, Internal ROM

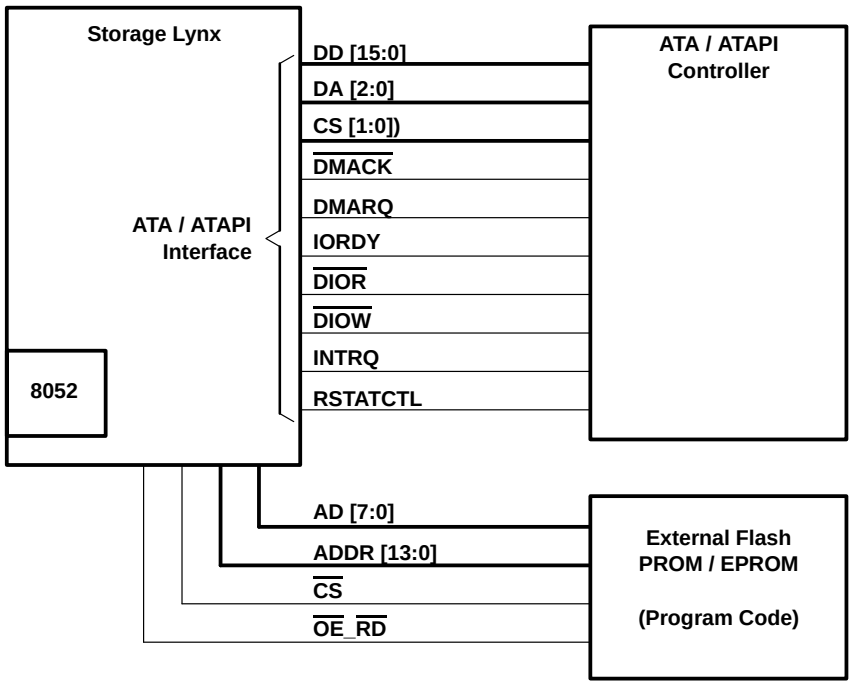


Figure 2–4. Mode 1, ATA/ATAPI Bridge, External ROM

2.4 Chapter References

1. *Serial Bus Protocol 2 (SBP-2), T10 Project 1155D*, Revision 4, May 19, 1998
2. *Mentor Graphics, 3Soft M8042 MegaMacro Design*
3. NCITS T10 1240D, *Reduced Block Commands Revision 10 (RBC)*
4. American National Standards Institute, ANSI NCITS 317-1998, *AT Attachment with Packet Interface Extension – (ATA/ATAPI-5 v3.0)*

3 Configuration Registers (CFR)

This section describes the layout and content of the TSB42AA9 configuration registers. The address space begins at 00h in the XDATA memory space of the embedded processor.

3.1 Register Map

Table 3-1 shows the StorageLynx register map.

Table 3–1. StorageLynx Register Map

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Register Name
00h	7				3				1				6				3				0				0				0				Version
04h																																	Reserved
08h	SFTRST			PAGEBIT	BSYCTL	TXEN	RXEN				RSTTX	RSTRX			ENA_LHOLD									CLRSIDER				PWRON				Control
0Ch	INT	PHINT	PHRRX	PHRST	SELFIDEND	RXGRFPKT	CMDRST	SELFIDER	ATSTK	ATFEMPTY	SNTRJ	HDRERR	TCERR	FIFOACK		CYST	RTRYLMT				ARBGP	SUBGP		LIN/LOUT	NORM	ABSY	AERR	PIERR	PDERR	SCMIS	NDMIS	AINT	Interrupt
10h	INT	PHINT	PHRRX	PHRST	SELFIDEND	RXGRFPKT	CMDRST	SELFIDER	ATSTK	ATFEMPTY	SNTRJ	HDRERR	TCERR	FIFOACK		CYST	RTRYLMT				ARBGP	SUBGP		LIN/LOUT	NORM	ABSY	AERR	PIERR	PDERR	SCMIS	NDMIS	AINT	Interrupt Mask
14h	CY_SECONDS								CY_COUNT												CY_OFFSET												Cycle Timer
18h																																	Reserved
1Ch	E_HCRC	E_DCRC	NO_PKT	F_ACK	NO_ACK				ACK																PING VALUE								Maintenance Control
20h																																	Reserved
24h	RDPHY	WRPHY			PHYRGAD				PHYRGADATA												PHYRECAD				PHYRECDATA								PHY Access
28h	ATP			TM						DMA_SPD					PIO_SPD		ATPSFTRST	ATPHRDRST		TRANSFER_DIR		AUTOCMD	STRTATPI	NONDTCMD									ATA/ATAPI Interface Configuration
2Ch	ATP_DATA [15:0]																SCNT										ATP_BUSWR	ATP_BUSRD	ATP_ADDR [3:0]				ATA/ATAPI Access
30h	ATFAVAIL								ATFCLR	ATFWBMTY	ATFFULL	ATACK					CD	CLEAR_GRF	GRF_EMPTY	CLR_STATFIFO	STATFIFO_ USED				GRFUSED								FIFO Status
34h	NRIDVAL		NODECNT						ROOT								BUS_NUMBER								NODE_NUMBER								Bus Reset
38h	BYTE1								BYTE0								BYTE3								BYTE2								Taskfile (0)
3Ch	BYTE4								BYTE3								BYTE7								BYTE6								Taskfile (1)
40h	BYTE9								BYTE8								BYTE11								BYTE10								Taskfile (2)
44h–48h																																	Reserved

Table 3–1. StorageLynx Register Map (Continued)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Register Name
4Ch					ASYNC RETRY LIMIT				RETRY INTERVAL													PRIMAX				BUDGETEN	PRIBUDGET							Asynchronous Retry
50h	FANDC																																Control transmit FIFO: First and Continue
54h	UPDATE																																Control transmit FIFO: Update
58h																																	Reserved
5Ch	CNTRLRF																																Control Receive FIFO
60h		MSTRST		CSTRST		DTRST			SCSISTATEN	CMDABORT	UNSOLSTATEN						SBP-2_STATUS												DISABLCSR	BACKPLANE	INITCMPLT	CNFGVLD	SBP-2 Control
64h	MGMTVLD	CMDSTATE		UNSOLEN																													SBP-2 Status
68h																									PADDR						ROM_RD	ROM_WR	Parameter Access
6Ch	PDATA																																Parameter Data
70h	CSD_FANDC																																Command Set Status FIFO: First and Continue
74h	CSD_UPDATE																																Command Set Status FIFO: Update
78h					BLKSIZE [11:0]												DATA [15:0]																Data FIFO Access
7Ch																																	Reserved

3.2 Register Descriptions

Within a byte, the most significant bit (MSB) is that which is transmitted first and the least significant bit (LSB) is that which is transmitted last over the 1394 bus. Within a quadlet (4 bytes or 32 bits), the most significant byte is that which is transmitted first and the least significant byte is that which is transmitted last over the 1394 bus. All software writes to the registers go to the first (and thus, most significant) byte (00:07). Table 3–2 describes the specifications given to the registers.

Table 3–2. Direction Tag Descriptions

DIR	NAME	MEANING
R	read	Field may be read by software.
W	write	Field may be written by software to any value.
U	update	Field may be autonomously updated

3.2.1 Version Register at 00h

This register uniquely identifies this part to the software. This read-only register has a fixed value of 73163000h.

3.2.2 Reserved Register at 04h

3.2.3 Control Register at 08h

Unless otherwise noted, all bits in this register are cleared to 0 at power up.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00	SFTRST	R	Software controlled device reset. This bit is used by software to generate a reset.
01–02			Reserved
03	PAGEBIT	R/W	Data memory page select. This bit is used by the embedded processor to select between two banks of 256 bytes of data memory. The embedded processor is address limited to 256 bytes of data memory. A 0 selects the lower 256 bytes of the 512 byte RAM used for processor data memory space. A 1 selects the upper 256 bytes of the 512 byte RAM.
04	BSYCTL	R/W	Busy control. This bit selects which busy state StorageLynx returns to an incoming packet. A 0 selects the normal busy/retry protocol, which only sends busy when necessary. A 1 selects a busy acknowledge sent to all incoming packets.
05	TXEN	R/W	Transmit enable. When this bit is cleared, the 1394 transmitter does not arbitrate or send packets. This bit is set after a power-on reset.
06	RXEN	R/W	Receive enable. When this bit cleared, the 1394 receiver does not receive any packets. This bit is not affected by a bus reset and is set after a power-on reset.
07–09			Reserved
10	RSTTX	R/W	Reset transmit. A 1 resets the entire transmitter synchronously. This bit clears itself.
11	RSTRX	R/W	Reset receive. A 1 resets the entire receiver synchronously. This bit clears itself.
12, 13			Reserved
14	ENA_LHOLD	R/W	Enable long hold cycle. A 1 increases the hold time on a bus grant to 10 cycles.
15–22			Reserved
23	CLRSIDER	W	Clear self-ID error. A 1 allows this bit to be automatic-cleared after one Nclock cycle.
24–26			Reserved
27	PWRON	R	Power on switch signal. This bit drives the output signal PWRON. This signal is activated by firmware in a power-on event.
28–31			Reserved

3.2.4 Interrupt and Interrupt Mask Register at 0C and 10h

The interrupt register is located at 0Ch and the interrupt mask register is located at 10h. The interrupt register powers up with 0 in all bits. The interrupt mask register powers up with the INT mask bit set, i.e., 8000_0000h. The mask bits allow individual control of each interrupt. A 1 in the mask bit field allows the corresponding interrupt in the Interrupt register to be generated. Once an interrupt is generated it must be cleared by writing a 1 to the bit to be cleared in the Interrupt register.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00	INT	R/W	Interrupt. This bit contains the value of all interrupt and interrupt mask bits ORed together.
01	PHINT	R/W	PHY interrupt. When this bit is set, the PHY has signaled an interrupt through the PHY interface.
02	PHRRX	R/W	PHY register receive. When this bit is set, a register value has been transferred to the PHY Access register (see section 3.2.9) from the PHY interface.
03	PHRST	R/W	PHY reset. When this bit is set, a PHY-LLC reconfiguration has started (1394 bus reset).
04	SELFIDEND	R/W	Self-ID end. This bit is set at the end of the self-ID reporting process and indicates the contents of the bus reset CFR register (see section 3.2.13) are valid.
05	RXGRFPKT	R/W	Receive packet to GRF. When this bit is set, a complete packet has been confirmed into the general receive FIFO (GRF) interface.
06	CMDRST	R/W	Command reset. When this bit is set, the receiver has been sent a quadlet write request addressed to the RESET_START CSR register (see section 2.2.1).
07	SELFIDER	R/W	Self-ID error. When this bit is set, an error in the self-ID process has been detected.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
08	ATSTK	R/W	ATF stuck. When this bit is set, the transmitter has detected invalid data at the asynchronous transmit FIFO (ATF) interface. If the first quadlet of a packet is not written to the control transmit FIFO: first and continue register (see section 3.2.19), the transmitter enters a state denoted by this interrupt. An underflow of the ATF also causes the same interrupt. When this *stuck* state is entered, no asynchronous packets can be sent until the ATF is cleared by way of the ATFCLR control bit (see section 3.2.12).
09	ATFEMPTY	R/W	ATF empty. When this bit is set, the ATF is empty.
10	SNTRJ	R/W	Sent rejected. When this bit is set, the receiver is forced to send a busy acknowledge to a packet addressed to this node because the GRF overflowed.
11	HDRERR	R/W	Header CRC error. When this bit is set, the receiver has detected a header cycle redundancy check (CRC) error on an incoming packet that may have been addressed to this node.
12	TCERR	R/W	Transaction code error. When this bit is set, the transmitter has detected an invalid transaction code in the data at the ATF interface.
13	FIFOACK	R/W	FIFO acknowledge interrupt. When this bit is set, an acknowledge from a previous ATF transmit has been received.
14			Reserved
15	CYST	R/W	Cycle start. When this bit is set, the transmitter has sent a cycle-start packet or the receiver has received a cycle-start packet.
16	RTRYLMT	R/W	Retry limit reached. Informs the initiator of an undeliverable packet (see section 3.2.18)
17-19			Reserved
20	ARBGP	R/W	Arbitration gap idle. When this bit is set, the serial bus has been idle for an arbitration reset gap.
21	SUBGP	R/W	Subaction gap idle. When this bit is set, the serial bus has been idle for a subaction gap. This bit can only be set in diagnostic mode.
22			Reserved
23	LIN/LOUT	R/W	Login complete or logout complete. This bit notifies the embedded processor of the login/logout state.
24	NORM	R/W	Normal (In operational mode 0 or 1). When this bit is set, a command has completed normally with no error. Writing a 1 to this bit clears the bit.
25	ABSY	R/W	Busy at start of a command. When this bit is set, the ATA/ATAPI device is busy at the start of the command (after writing to STRTATPI; see section 3.2.10). The command is not executed. The processor then reads the taskfile registers (see section 3.2.14) to determine the cause of this interrupt.
26	AERR	R/W	ATA error. When this bit is set, an error (error bit set) occurred during the ATA/ATAPI auto-sequence. The processor then reads the taskfile registers (see section 3.2.14) to determine the cause of the error.
27	PIERR	R/W	ATAPI sequence error after taskfile writes. In ATAPI mode with full auto sequencing, a 1 indicates that a sequence error has occurred after initializing the taskfile registers (see section 3.2.14) and before command packet bytes have been issued.
28	PDERR	R/W	Sequence error during data transfer. In ATAPI mode, a 1 indicates that there was a sequence error during data transfer.
29	SCMIS	R/W	Sector count mismatch. In ATA PIO mode, a 1 indicates that there is a mismatch between the sector count (provided in the sector count field, see section 3.2.11) and the ATA transfer.
30	NDMIS	R/W	Nondata command mismatch. A 1 indicates that a nondata command is specified in the ATA/ATAPI interface configuration register (see section 3.2.10) but when the command was issued, the ATA device indicated that the data transfer operation was active.
31	AINT	R/W	ATA/ATAPI interrupt. A 1 indicates that an interrupt has occurred at the ATA/ATAPI interface. This bit is only set during the *manual* phase of a sequence. During the automatic phase of a sequence, AINT is cleared because the hardware handles INTRQ automatically without processor intervention.

3.2.5 Cycle Timer Register at 14h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This read/write register indicates the current cycle number and offset. It is loaded with the data field from an incoming cycle start packet. In the event that the cycle start messages are not received, the fields can continue to maintain a local time reference. The cycle timer register must be written as a quadlet (32 bits).

Since all accesses to this register must be 32 bits, and the host bus is only 8 bits wide, the four bytes to be delivered to or from this register go through a stacking buffer. Address 14h should be accessed first, followed consecutively by the other three addresses, or an invalid value may be read/written. The order of bytes in the stacking buffer is as follows:

Address 14h = Byte 3 (00:07) (most significant byte)
Address 15h = Byte 2 (08:15)
Address 16h = Byte 1 (16:23)
Address 17h = Byte 0 (24:31) (least significant byte)

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–06	CY_SECONDS	R/W/U	Cycle seconds. This field counts seconds (CY_COUNT rollovers) modulo 128.
07–19	CY_COUNT	R/W/U	Cycle counts. This field counts cycles (CY_OFFSET rollovers) modulo 8000.
20–31	CY_OFFSET	R/W/U	Cycle offset. This field counts 24.576 MHz clocks modulo 3072, i.e. ,125 µs. If an external 8 kHz clock configuration is being used, CY_OFFSET must be set to 0 at each tick of the external clock.

3.2.6 Reserved Register at 18h

3.2.7 Maintenance Control Register at 1Ch

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register provides the ability to simulate or force errors during the transmission of packets.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00	E_HCRC	R/W	Header CRC error. When this bit is set, the packet header CRC component of the next primary packet generated by this node is in error or is invalid. After the next packet for this node is generated, this bit is cleared.
01	E_DCRC	R/W	Data CRC error. When this bit is set, the data CRC component of the next primary packet generated by this node is in error or is invalid. This bit is cleared to 0 immediately upon transmission of the erroneous CRC.
02	NO_PKT	R/W	No packet. When this bit is set, the next primary packet to be generated by this node is discarded. This bit is cleared to 0 immediately after the next packet for this node is discarded.
03	F_ACK	R/W	Modified acknowledge field. When this bit is set, the acknowledge field (ACK) is used within the next acknowledge packet generated by this node. This bit is cleared to 0 immediately after the next acknowledge packet for this node is generated.
04	NO_ACK	R/W	No acknowledge. When this bit is set, the next acknowledge packet (that would normally have been generated by this node) is not sent. This bit is immediately cleared to 0 when the next acknowledge packet for this node is discarded.
05–07			Reserved
08–15	ACK	R/W	Acknowledge field. This 8-bit field contains the 8-bit acknowledge packet (ack_code and ack_parity) to be supplied when the F_ACK bit indicates a modified acknowledge packet will be generated.
16–22			Reserved
23–31	PING VALUE	R	Ping timer value. This 8-bit field reflects the time it takes a node to respond to a ping packet. The granularity of this timer is 40 ns.

3.2.8 Reserved Register at 20h

3.2.9 PHY Access Register at 24h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register allows the StorageLynx link core access to the PHY interface.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00	RDPHY	R/W	PHY read register request. When this bit is set, a read register request with the address equal to PHYRGAD is sent to the PHY interface. This bit is cleared when the request is sent.
01	WRPHY	R/W	PHY write register request. When this bit is set, a write register request with address equal to PHYRGAD is sent to the PHY interface. This bit is cleared when the request is sent.
02–03			Reserved
04–07	PHYRGAD	R/W	PHY register address. The address of the PHY register that is to be accessed.
08–15	PHYRGDATA	R/W	PHY register data. The data to be written to the PHY register indicated in PHYRGAD.
16–19			Reserved
20–23	PHYRECAD	R/W	PHY received address.
24–31	PHYRECDATA	R/W	PHY received data.

3.2.10 ATA/ATAPI Interface Configuration Register at 28h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is used to configure the ATA and ATAPI modes. The embedded firmware performs an identify device command immediately after power up to determine the device type and speed capabilities of the attached media device. After parsing the parameter data returned from this command, the firmware automatically loads the ATP, TM, and SPD fields in the register below.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00	ATP	R/W	ATA/ATAPI device type select. When this bit is 0, the device uses ATA transfer protocol. When this bit is 1, the device uses ATAPI transfer protocol.
01			Reserved
02–03	TM	R/W	Transfer mode When TM = 00, the transfer mode is PIO. When TM = 01, the transfer mode is multiword DMA. When TM = 10, the transfer mode is reserved. When TM = 11, the transfer mode is ultra DMA.
04–08			Reserved
09–11	DMA_SPD	R/W	Multiword and ultra direct memory access (DMA) transfer speeds. When the transfer mode is multiword DMA, the ATA/ATAPI transfer mode speed is specified as follows: DMA_SPD = 0 DMA Mode 0 (default) DMA_SPD = 1 DMA Mode 1 DMA_SPD = 2 DMA Mode 2 DMA_SPD = 3–7 Reserved When the transfer mode is Ultra DMA, the ATA/ATAPI transfer mode speed is specified as follows: DMA_SPD = 0 Ultra DMA mode 0 DMA_SPD = 1 Ultra DMA mode 1 DMA_SPD = 2 Ultra DMA mode 2 DMA_SPD = 3 Ultra DMA mode 3 DMA_SPD = 4 Ultra DMA mode 4 DMA_SPD = 5–7 Reserved
12			Reserved

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
13–15	PIO_SPD	R/W	PIO transfer speed. When the transfer mode is PIO, the ATA/ATAPI transfer mode speed is specified as follows: PIO_SPD = 0 PIO Mode 0 (default) PIO_SPD = 1 PIO Mode 1 PIO_SPD = 2 PIO Mode 2 PIO_SPD = 3 PIO Mode 3 PIO_SPD = 4 PIO Mode 4 PIO_SPD = 5–7 Reserved.
16	ATPSFTRST	R/W	ATAPI soft reset. A 1 resets the StorageLynx ATA controller.
17	ATPHRDRST	R/W	ATAPI hard reset. When this bit is set, a 25 µs reset pulse to the ATA device RESET pin is generated. The microprocessor can poll this bit to determine the completion of the reset.
18			Reserved
19	TRANSFER_DIR	R/W	Transfer direction. This bit indicates the direction of the transfer across the ATA/ATAPI interface.
20			Reserved
21	AUTOCMD	W	Auto command. AUTOCMD is used to qualify the auto sequencing action when writing to STRTATPI trigger bit. A 1 allows the command phase, packet phase for ATAPI, and the data transfer phase to execute automatically after writing to STRTATPI. A 0 allows only the data transfer phase to execute automatically after writing to STRTATPI.
22	STRTATPI	W	Start ATAPI. When this bit is written it triggers the sequencer to start the ATA/ATAPI sequence. A 1 allows the entire ATA/ATAPI sequence to execute automatically. A 0 triggers the data transfer phase to execute automatically. The command phase (issuing task file writes and command packets) must have been done by the processor before writing to STRTATPI. This bit is cleared after one clock cycle.
23	NONDTCMD	R/W	Nondata command. When this bit is set, the command to be executed in autotransfer mode is a nondata command. A 0 indicates data transfer commands.
24–31			Reserved

3.2.11 ATA/ATAPI Access Register at 2Ch

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is used to manually access registers in the external ATA controller. The read and write protocols for using this register are as follows:

Write operations to the ATA controller:

- The data to be written is stored at ATP_DATA[15:0].
- The address to be accessed is stored at ATP_ADDR[3:0].
- The write bit is set (ATP_BUSWR). At this point the write operation begins.
- After the write is complete the write bit is cleared automatically.
  (These register accesses use the PIO protocol only.)

Read operations from the ATA controller:

- The address to be accessed is stored at ATP_ADDR[3:0].
- The read bit is set (ATP_BUSRD). At this point the read operation begins.
- After the read is complete the read bit is cleared automatically.
- The data returned is available at ATP_DATA[15:0].
  (These register accesses use the PIO protocol only.)

Table 3–3. Command Block Register Addressing From ATA/ATAPI Access Register

ATP_ADDR[3:0]	COMMAND BLOCK REGISTER
0000	DATA
0001	Write: FEATURES
	Read: ERROR
0010	SECTOR COUNT
0011	SECTOR NUMBER
0100	CYLINDER LOW
0101	CYLINDER HIGH
0110	DEVICE/HEAD
0111	Write: COMMAND
	Read: STATUS
1000	Read: ALTERNATE STATUS
	Write: DEVICE CONTROL
Others	Invalid

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
0–15	ATP_DATA[15:0]	R/W	ATA/ATAPI data [15:0]. This field contains the data to be written to the ATA/ATAPI controller for a write operation, or holds the data returned from the ATA/ATAPI controller for a read operation.
16–24	SCNT	R/W	Sector count. This field is used for ATA PIO mode transfers only. It indicates the number of 512-byte sectors to transfer. SCNT decrements each time a block has been transferred.
25			Reserved
26	ATP_BUSWR	R/W	ATA/ATAPI bus write flag. When this bit is set, a write operation to an ATA/ATAPI controller command block register is initiated. Data to be written is provided at ATP_DATA[15:0]. The address to be accessed is provided at ATP_ADDR[3:0]. This bit automatically clears to 0 after the write operation is complete.
27	ATP_BUSRD	R/W	ATA/ATAPI bus read flag. When this bit is set, a read operation from an ATA/ATAPI controller command block register is initiated. Data read is returned to ATP_DATA[15:0]. The address to be accessed is loaded at ATP_ADDR[3:0]. This bit automatically clears to 0 after the read operation is complete.
28–31	ATP_ADDR[3:0]	R/W	ATA/ATAPI address [3:0]. This field indicates the command or control register to be accessed. See Table 3–3 for register addressing.

3.2.12 FIFO Status Register at 30h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register contains information on the control FIFO used by the embedded processor.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–07	ATFAVAIL	R	ATF available. This field indicates the space available, in quadlets, in the asynchronous transmit FIFO (ATF).
08	ATFCLR	R/W	ATF clear. When this bit is set, the ATF is cleared.
09	ATFWBMTY	R	ATF write buffer empty. This bit is set if the 4 quadlet FIFO write buffer is empty.
10	ATFFULL	R	ATF full. When this bit is set the ATF is full.
11–15	ATACK	R	ATF acknowledge. This bit is set when an acknowledge is received in response to a packet sent via the ATF.
16	CD	R	Set if the 33rd bit is a 1 during a read of the general receive FIFO (GRF).
17	CLEAR_GRF	R/W	GRF clear. When this bit is set, the GRF is cleared.
18	GRF_EMPTY	R	GRF read buffer empty. This bit is set if the 4 quadlet GRF read buffer is empty.
19	CLR_STATFIFO	R/W	Status FIFO clear. When this bit is set, the status FIFO is cleared.
20–23	STATFIFO_USED	R	Status FIFO used. This field indicates the amount of quadlets used in the status FIFO.
24–31	GRFUSED	R	GRF space used. This field indicates the amount of quadlets used in the GRF.

3.2.13 1394 Bus Reset Register at 34h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register contains information from 1394 bus resets.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00	NRIDVAL	R	Node/Root ID valid. This bit is set if the Node ID, IRM Node ID, Node Count, and Root information is valid.
01			Reserved
02–07	NODECNT	R	Nodes detected. This field contains the number of nodes detected in the system.
08	ROOT	R	Root. This bit is set if the current node is the root node.
09–15			Reserved
16–25	BUS_NUMBER	R/W	10-bit IEEE–1212 bus number. This field is set to 3FFh when BusNum is set and there is a bus reset.
26–31	NODE_NUMBER	R/W	Node number. This field is automatically updated with the node number of the current node following a bus reset.

3.2.14 Taskfile (0) Register at 38h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. The taskfile registers are accessed to transfer ATAPI commands to/ from an ATAPI storage device.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–07	BYTE1	R/W	ATAPI command register, byte 1. This field contains byte 1 of the 12 Byte command issued if STRATPI and AUTOCMD are set (see section 3.2.10).
08–15	BYTE0	R/W	ATAPI command register, byte 0. This field contains byte 0 of the 12 Byte command issued if STRATPI and AUTOCMD are set.
16–23	BYTE3	R/W	ATAPI command register, byte 3. This field contains byte 3 of the 12 Byte command issued if STRATPI and AUTOCMD are set.
24–31	BYTE2	R/W	ATAPI command register, byte 2. This field contains byte 2 of the 12 Byte command issued if STRATPI and AUTOCMD are set.

3.2.15 Taskfile (1) Register at 3Ch

Unless otherwise noted, all bits in this register are cleared to 0 at power up.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–07	BYTE5	R/W	ATAPI command register, byte 5. This field contains byte 5 of the 12 byte command issued if STRATPI and AUTOCMD are set.
08–15	BYTE4	R/W	ATAPI command register, byte 4. This field contains byte 4 of the 12 byte command issued if STRATPI and AUTOCMD are set.
16–23	BYTE7	R/W	ATAPI command register, byte 7. This field contains byte 7 of the 12 byte command issued if STRATPI and AUTOCMD are set.
24–31	BYTE6	R/W	ATAPI command register, byte 6. This field contains byte 6 of the 12 byte command issued if STRATPI and AUTOCMD are set.

3.2.16 Taskfile (2) Register at 40h

Unless otherwise noted, all bits in this register are cleared to 0 at power up.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–07	BYTE9	R/W	ATAPI command register, byte 9. This field contains byte 9 of the 12 byte command issued if STRATPI and AUTOCMD are set.
08–15	BYTE8	R/W	ATAPI command register, byte 8. This field contains byte 8 of the 12 byte command issued if STRATPI and AUTOCMD are set.
16–23	BYTE11	R/W	ATAPI command register, byte 11. This field contains byte 11 of the 12 byte command issued if STRATPI and AUTOCMD are set.
24–31	BYTE10	R/W	ATAPI command register, byte 10. This field contains byte 10 of the 12 byte command issued if STRAT-PI and AUTOCMD are set.

3.2.17 Reserved Register at 44h–48h

Registers 44h through 48h are reserved for future use.

3.2.18 Asynchronous Retry/Priority Budget Register at 4Ch

Unless otherwise noted, all bits in this register are cleared to 0 at power up.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–03			Reserved
04–07	ASYNC RETRY LIMIT	R/W	Asynchronous retry limit. This field contains the number of times StorageLynx automatically retries sending asynchronous packets from the ATF before giving up. After the retry count is exhausted, a FIFOACK interrupt is generated and the ATACK field (see section 3.2.12) is updated to reflect the timeout. This field is also addressable as the BUSY_TIMEOUT register in the CSR at initial node space address: FFFF_F000_0210h (see section 2.2.1).
08–15	RETRY INTERVAL	R/W	Asynchronous retry interval. This field monitors the time between asynchronous retries in increments of isochronous cycles.
16–20			Reserved
21–23	PRIMAX	R/W	Priority maximum. This field defaults to 0. Its maximum value is 7. PRIMAX is set by the application initialization and is also mapped to the corresponding field in the PRIORITY_BUDGET register, CSR PRI_MAX, at initial node space address: FFFF_F000_0218h.
24			Reserved
25	BUDGETEN	R/W	Enable priority budget arbitration. This bit enables priority budget arbitration to begin.
26–31	PRIBUDGET	R/W	Priority budget allotment. This field is mapped to the corresponding field in the PRIORITY_BUDGET register, CSR PRI_REQ.

3.2.19 Control Transmit FIFO: First and Continue Register at 50h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is for the first quadlet and consecutive quadlets of a packet to be sent to the control packet transmit FIFO. The byte accesses to this register need to be ordered properly, or invalid values may be read/written from/to this register. Since all accesses to this register must be as a quadlet (32 bits) and the host bus is only 8 bits wide, the four bytes to be delivered to or from this register go through a stacking buffer. Address 50h must be accessed first, followed consecutively by the other three addresses, or an invalid value may be read/written. The order of bytes in this stacking buffer is as follows:

Address 50h = Byte 3 (00:07) (most significant byte)
Address 51h = Byte 2 (08:15)
Address 52h = Byte 1 (16:23)
Address 53h = Byte 0 (24:31) (least significant byte)

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–31	FANDC	R/W	First and continue. This field contains the first and consecutive quadlets of a packet to be sent to the control packet transmit FIFO.

3.2.20 Control Transmit FIFO: Update Register at 54h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is for the last quadlet of a packet to be sent to the control packet transmit FIFO. When the last byte of this register is written to, the packet is confirmed for transmission. The byte accesses to this register must be ordered properly, or invalid values may be read/written from/to this register. Since all access to this register must be as a quadlet (32 bits), and the host bus is only 8 bits wide, the four bytes to be delivered to or from this register go through a stacking buffer. Address 54h should be accessed first, followed consecutively by the other three addresses, or an invalid value may be read/written. The order of bytes in this stacking buffer is as follows:

Address 54h = Byte 3 (00:07) (most significant byte)
Address 55h = Byte 2 (08:15)
Address 56h = Byte 1 (16:23)
Address 57h = Byte 0 (24:31) (least significant byte)

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–31	UPDATE	R/W	Update. This field contains the last data quadlet of a packet to be sent to the control packet transmit FIFO.

3.2.21 Reserved at 58h

3.2.22 Control Receive FIFO Register at 5C

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is for received data for a packet from the control receive FIFO. The byte accesses to this register must be ordered properly, or invalid values may be read/written from/to this register. Since all access to this register must be as a quadlet (32 bits), and the host bus is only 8 bits wide, the four bytes to be delivered to or from this register go through a stacking buffer. Address 5Ch should be accessed first, followed consecutively by the other three addresses, or an invalid value may be read/written. The order of bytes in this stacking buffer is as follows:

Address 5Ch = Byte 3 (00:07) (most significant byte)
Address 5Dh = Byte 2 (08:15)
Address 5Eh = Byte 1 (16:23)
Address 5Fh = Byte 0 (24:31) (least significant byte)

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–31	CNTRLRF	R/W	Control packet receive FIFO data. This field contains a quadlet from a received data packet from the control packet receive FIFO.

3.2.23 SBP-2 Control Register at 60h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register contains the control for the SBP–2 management and command agents.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00			Reserved
01	MSTRST	W	Management agent reset. A 1 resets management agent state machines. This bit is self-clearing.
02			Reserved
03	CSTRST	R/W	Command agent reset. A 1 resets the command agent state machine to idle. This bit is self-clearing.
04			Reserved
05	DTRST	R/W	Data transfer reset. A 1 resets the data transfer state machine to idle and the BLKSIZE register in the data transfer register (see section 3.2.29) is cleared. The data transfer must be reinitialized for the next transfer to begin. This bit is self-clearing.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
06–07			Reserved
08	SCSISTATEN	W	SCSI status enable. When this bit is set, the command set status is transmitted after the command set dependent status FIFO (see section 3.2.27) has been loaded and confirmed.
09	CMDABORT	W	Command abort. When this bit is set, the data transfer control aborts the current command being processed. A SBP-2 status is returned to the initiator after the abort.
10	UNSOLSTA-TEN	R	Unsolicited status enable. This bit is set if the SBP-2 host (the initiator) has enabled the link to send an unsolicited status.
11–15			Reserved
16–23	SBP-2_STA-TUS	W	SBP-2 status. A write to this field causes a SBP-2 response packet to be sent with the response code loaded in this field.
24–27			Reserved
28	DISABLCSR	R/W	Disable automatic CSR (IEEE 1212 registers) access response. When this bit is set, the link does not respond automatically to CSR register accesses and the CSR requests are forwarded to the GRF.
29	BACKPLANE	R/W	Backplane enable. A 1 specifies that the backplane PHY specification must be used for the NODE_IDs CSR.
30	INITCMPLT	R/W	Initialization complete. Until this bit is set, StorageLynx responds with an ack_tardy code. The initialization routine sets this bit to enable the TSB42AA9. If the configuration ROM is loaded on power–up by the 2-wire serial bus interface, the internal circuitry enables INITCMPLT and CNFGVLD after completion of the load. If INITCMPLT is set and the CNFGVLD is not set, then StorageLynx functions normally but does not automatically respond to read requests to configuration ROM space.
31	CNFGVLD	R/W	Configuration memory valid. The 2-wire serial bus state machine sets this bit when the parameter RAM is initialized. If no 2-wire serial bus connection exists then the parameter RAM may be loaded by the embedded processor. In this case the embedded processor must set CNFGVLD when parameter RAM is initialized. If CNFGVLD is not set then the device does not automatically respond to read requests to the configuration ROM space and the read requests are routed to the control receive FIFO to be handled by the embedded processor.

3.2.24 SBP-2 Status Register at 64h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register contains the status for the SBP–2 management and command agents.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00	MGMTVLD	R/W	Management login valid. The management agent automatically sets this bit.
01–02	CMDSTATE	R/W	Command state. This field indicates the command agent functional state: reset, active, suspended, or dead. This value is also reported in the AGENT_STATE command agent CSR.
03	UNSOLEN	R/W	Send unsolicited status enable. When this bit is set, the status packet loaded in the command set dependent status FIFO (see section 3.2.27) is transmitted to the SBP-2 host (initiator). This bit automatically clears to 0 after the status FIFO is emptied. UNSOLEN is only useful if unsolicited status reception has been enabled by the host (see section 0).
04–31			Reserved

3.2.25 Parameter Data Register at 60Ch

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register provides read/write access to the configuration ROM.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–23			Reserved
24–29	PADDR	R/W	Parameter address. This field indicates the quadlet address for a configuration ROM read/write.
30	ROM_RD	R/W	Configuration ROM read. This bit initiates a read to the configuration ROM It clears itself when the read is complete.
31	ROM_WR	R/W	Configuration ROM write. This bit initiates a write to the configuration ROM It clears itself when the write is complete.

3.2.26 Parameter Data Register 6Ch

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is the data buffer for parameter access.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–31	PDATA	R/W	Parameter data. This field contains the parameter data buffer for parameter reads and writes.

3.2.27 Command Set Dependent Status FIFO: First and Continue at 70h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is for all status FIFO data except for the last quadlet. The byte accesses to this register must be ordered properly, or invalid values may be read/written from/to this register. Since all access to this register must be as a quadlet (32 bits), and the host bus is only 8 bits wide, the four bytes to be delivered to or from this register go through a stacking buffer. Address 70h must be accessed first, followed consecutively by the other three addresses, or an invalid value may be read/written. The order of bytes in this stacking buffer is as follows:

Address 70h = Byte 3 (00:07) (most significant byte)
Address 71h = Byte 2 (08:15)
Address 72h = Byte 1 (16:23)
Address 73h = Byte 0 (24:31) (least significant byte)

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–31	CSD_FANDC	R/W	Command set dependent status FIFO: first and continue. This field contains the first and consecutive quadlets of command set dependant status FIFO data.

3.2.28 Command Set Dependent Status FIFO: Update at 74h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is for the last quadlet of a command set dependent status message. The byte accesses to this register must be ordered properly, or invalid values may be read/written from/to this register. Since all access to this register must be as a quadlet (32 bits), and the host bus is only 8 bits wide, the four bytes to be delivered to or from this register go through a stacking buffer. Address 74h must be accessed first, followed consecutively by the other three addresses, or an invalid value may be read/written. The order of bytes in this stacking buffer is as follows:

Address 74h = Byte 3 (00:07) (most significant byte)
Address 75h = Byte 2 (08:15)
Address 76h = Byte 1 (16:23)
Address 77h = Byte 0 (24:31) (least significant byte)

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–31	CSD_UPDATE	R/W	Command set dependent status FIFO: Update. This field contains the last quadlet of a command set dependent status message.

3.2.29 Data FIFO Access Register at 78h

Unless otherwise noted, all bits in this register are cleared to 0 at power up. This register is used to load data into the data FIFO from the embedded 8052 processor. The DATA[15:0] field contains the data to be written to the data FIFO. The byte, 7Ah, must be loaded first, then the next consecutive byte of data is loaded to address 7Bh. After byte 7Bh is loaded, the data at 7Ah and 7Bh is written to the data FIFO. The processor can use the information in the upper half of this register (BLKSIZE[11:0]) to determine how many bytes it can load into the data FIFO prior to the data being packetized and transmitted out to 1394. The number of bytes is determined from the last previously received command block ORB header contents (*data_size*, *page_size*, *page_table_present*, *max_payload*, and *spd* fields[1]). The BLKSIZE[11:0] value is static, so it is the responsibility of the embedded processor to read this value and keep track of the number of bytes that have been loaded prior to transmit.

Once the number of bytes shown in BLKSIZE[11:0] have been written to the FIFO, the data transfer control block moves the data from the FIFO to the transmit packetizer where it is sent to the initiator. After the data has been transmitted and the FIFO can again be loaded, the data transfer control block waits for the next write from the ATA/ATAPI interface.

BIT NUMBER	BIT NAME	DIR	DESCRIPTION
00–03			Reserved
04–15	BLKSIZE[11:0]	R	Data block size. This field indicates the number of bytes that the processor needs to load into the data FIFO prior to the next 1394 transfer. This field is updated after each command block ORB is received from the initiator.
16–31	DATA[15:0]	W	Data. The field contains 16-bit data to be written to the data FIFO.

3.2.30 Reserved at 7Ch

[1]T10 Project 1155D, ANSI NCTIS.xxx-199x, Serial Bus Protocol 2 (SBP-2)

4 Configuration ROM

This section describes the contents and addressing of the configuration ROM that all SBP–2 target nodes must implement. The values contained in configuration ROM depend upon the type and characteristics of the storage device attached to StorageLynx.

4.1 Configuration ROM Requirements (All Values in Hex)

The configuration ROM is located internal to StorageLynx at a base address of FFFF F000 0400h. The configuration ROM consists of a bus information block, a root directory, a unit directory, and related text leaves containing additional information on the device. The bus information block and the root directory are at fixed locations, and all other data in the configuration ROM are addressed using information from within these two blocks. Entries within the root directory and unit directory can be arranged in any order, except the text leaf pointers must follow the module vendor id and model id entries. The text leaves must be arranged and pointed to in the manner shown below.

Only the required entries of the root directory and unit directory are shown in the following table. Additional entries can be added. The ASCII text strings in the Module Vendor ID text leaf, the product revision text leaf, and the product ID text leaf can also be longer; however the only the first 8 bytes, 4 bytes, and 16 bytes (respectively) of each text string are returned with the INQUIRY data. The stated lengths of the blocks and the offset addresses of the text leaves will change with the addition of optional entries and longer text strings. The maximum internal storage (parameter RAM) allocated for configuration ROM immediate storage is 192 bytes (48 quadlets).

BLOCK	ADDR	REQ	DESCRIPTION	0–7	8–15	16–23			24–31		
Bus Info Block	400	E1	General ROM	**04** Bus Infor Block Length	**25** CRC Length	ROM CRC Value					
	404	E1, V1	ASCII 1394	**31**	**33**	**39**			**34**		
	408	E1		**00** No Iso Support	**FF** Not used	Max Rec (4)	rsvd (2)	Max ROM (2)	General (4)	rsvd (1)	Lnk Spd (3)
	40C	E1	EUI 64	Vendor ID					Chip ID HI		
	410	E1	EUI 64	Chip ID LO							
Root Directory	414	E1	Length & CRC	**0005** Length of Root Directory in Quadlets		Root Directory CRC					
	418	E1	Node Capabilities	**0C**	**00** Reserved	**83C0** spt, 64, fix, lst, drq implemented					
	41C	E3		**03**	Module Vendor ID						
	420	E3, P3	Text Leaf Pointer: Vendor ID	**81**	**00000E** Number of Quadlets until beginning of Vendor ID Text Leaf						
	424	E4	Text Leaf Pointer: Product Revision	**81**	**000012** Number of Quadlets until beginning of Product Revision Text Leaf						
	428	E1	Unit Directory Offset	**D1**	**000001** Number of Quadlets until beginning of Unit Director						

Requirements Key:
E1 Entry required by the 1394 Standard[1]
V1 Value shown in bold required by the 1394 Standard[1]
E2 Entry required by the RBC Standard[2]
V2 Value shown in bold required by the RBC Standard[2]
E3 Entry required by the SBP–2 Standard[3]
V3 Value shown in bold required by the SBP–2 Standard[3]
P3 Placement required by the SBP–2 Standard[3]
E4 Entry required by TI
V4 Value shown in bold required by TI

[1] IEEE Std 1394–1995, *Standard for a High Performance Serial Bus*
[2] NCITS T10 1240D, *Reduced Block Commands Revision 10 (RBC)*
[3] T10 Project 1155D, ANSI NCTIS.xxx–199x, *Serial Bus Protocol 2 (SBP–2)*

BLOCK	ADDR	REQ	DESCRIPTION	0–7	8–15	16–23	24–31
Unit Directory	42C	E1	Length & CRC	**000A** Length of Unit Directory in Quadlets		Unit Directory CRC	
	430	E3, V3	Unit Spec ID	**12**	**00609E** Defined in SBP-2 Standard		
	434	E3, V3	Unit SW Version	**13**	**010483** Defined in SBP-2 Standard		
	438	E4, V4	CSR offset	**54**	**00400**		
	43C	E2	Unit Characteristics	**3A**	**000A08** Defined by SBP-2 Standard		
	440	E3, V3	Command Set Spec ID	**38**	**00609E** T10 Technical Committee		
	444	E3, V3	Command Set (RBC)	**39**	**0104D8** Command Set (RBC)		
	448	E4, V4	Firmware/ Hardware Rev.	**3C**	**0028** (16)	**00** (3)	Firmware Rev. (5)
	44C	E2, V2	Device Type and LUN	**14**	**00** RSVD (3) / **00** Direct Access, **05** CD/DVD, **0E** RBC Device Type (5)	**00** Logical Unit (LUN) (16)	
	450	E3	Model ID	**17**	**000000** Determined by Vendor		
	454	E3, P3	Text Leaf points to Product Revision	**81**	**00000A** Number of Quadlets until beginning of Product Revision Text Leaf		
Text Leaf: Module Vendor ID	458	E3	Length & CRC	**0004** Length of Leaf in Quadlets		Leaf CRC	
	45C	E1, V1	ASCII Test	**00000000**			
	460	E1, V1	ASCII Test	**00000000**			
	464	E3	ASCII Test	Vendor ID			
	468	E3	ASCII Test				
Text Leaf: Product Revision	46C	E4	Length & CRC	**0003** Length of Leaf in Quadlets		Leaf CRC	
	470	E1, V1	ASCII Test	**00000000**			
	474	E1, V1	ASCII Test	**00000000**			
	478	E4	ASCII Test	Product Revision			
Text Leaf: Product ID	47C	E3	Length & CRC	**0006** Length of Leaf in Quadlets		Leaf CRC	
	480	E1, V1	ASCII Test	**00000000**			
	484	E1, V1	ASCII Test	**00000000**			
	488	E3	ASCII Test	Product ID			
	48C	E3	ASCII Test				
	490	E3	ASCII Test				
	494	E3	ASCII Test				

Requirements Key:

E1 Entry required by the 1394 Standard[1]
V1 Value shown in bold required by the 1394 Standard[1]
E2 Entry required by the RBC Standard[2]
V2 Value shown in bold required by the RBC Standard[2]
E3 Entry required by the SBP–2 Standard[3]
V3 Value shown in bold required by the SBP–2 Standard[3]
P3 Placement required by the SBP–2 Standard[3]
E4 Entry required by TI
V4 Value shown in bold required by TI

[1] IEEE Std 1394–1995, *Standard for a High Performance Serial Bus*
[2] NCITS T10 1240D, *Reduced Block Commands Revision 10 (RBC)*
[3] T10 Project 1155D, ANSI NCTIS.xxx–199x, *Serial Bus Protocol 2 (SBP–2)*

4.2 Parameter RAM

Efficient hardware implementation of the SBP–2 protocol requires internal RAM storage of the configuration ROM. ASIC implementation is more efficient using embedded RAM than using registers. The configuration ROM storage access can be a combination of on-chip RAM and off-chip ROM through the 2-wire serial bus interface. The parameter interface in the CFR registers (see section 3.2.25) is contiguous. Internal storage of configuration ROM information allows StorageLynx to respond faster to requests for information from the host like the INQUIRY command, rather than having to poll an external EEPROM via the 2-wire serial bus interface every time information is required.

5 Firmware

The StorageLynx firmware stored in the internal ROM and executed by the embedded processor performs translation between the reduced block command (RBC)[1] set and ATA commands. The processor translates the SCSI commands: RBC, SCSI–3 primary commands 2 (SPC)[2], or SCSI–3 block commands (SBC)[3] used by SBP–2 into equivalent ATA commands (and vice versa), although not all commands require an ATA command to be issued. At power up, the StorageLynx firmware issues an IDENTIFY DEVICE ATA command and retains certain data from the response. This ATA device data is used to respond to certain SCSI commands without another ATA command being issued.

The StorageLynx firmware acts mainly as a pass through for ATAPI devices. When an interrupt is received from the host designating a received packet (command), the firmware simply pulls the command out of the receive FIFO and places it in the StorageLynx ATAPI taskfile registers (see section 3.2.11). The StorageLynx hardware then transfers the PACKET command to the ATAPI device. When an interrupt is received from the ATAPI device designating command completion, the firmware signals the hardware to send a SBP–2 status packet of GOOD to the host. When an interrupt is received from the ATA/ATAPI interface designating an error condition, the firmware issues a REQUEST SENSE command to determine sense and additional sense.

5.1 SCSI Command Set

Table 5–1 shows the core SCSI commands supported by StorageLynx for ATA devices (predominately RBC commands). This table lists the command operation code and the relevant standard from which the command is derived.

Table 5–1. SCSI Commands Supported for ATA Devices

COMMAND	OPCODE	REFERENCE
INQUIRY	0x12	RBC
MODE SENSE (6)	0x1A	SPC
MODE SENSE (10)	0x5A	SPC
READ (6)	0x08	SBC
READ (10)	0x28	RBC
READ CAPACITY	0x25	RBC
TEST UNIT READY	0x00	SPC
VERIFY (10)	0x2F	RBC
WRITE (6)	0x0A	SBC
WRITE (10)	0x2A	RBC
WRITE BUFFER	0x3B	SPC
PASS THROUGH	0X01	Section 5.2

[1]NCITS T10 1240D, *Reduced Block Commands Revision 10 (RBC)*
[2]ANSI X3.301-1997, *SCSI-3 Primary Commands (SPC)*
[3]ANSI NCITS 306-1998, *SCSI-3 Block Commands (SBC)*

5.2 Supported Commands

This section provides descriptions and additional information on the SCSI commands supported by the StorageLynx firmware.

5.2.1 INQUIRY

The INQUIRY command does not require StorageLynx to generate an ATA command to be sent to the ATA device in order to respond. Data is taken from the saved IDENTIFY DEVICE response information from the ATA device and from the configuration ROM data loaded into StorageLynx, and the command response to be sent to the host is generated.

5.2.2 MODE SENSE (6) and MODE SENSE (10)

The MODE SENSE (6) and MODE SENSE (10) commands are only supported by the firmware when the commands request the device parameters page (page code 0x06) or all pages (page code 0x3F). When the host sends an all pages MODE SENSE command, StorageLynx only returns the device parameters page. The necessary data for the device parameters page MODE SENSE command response is taken from the saved IDENTIFY DEVICE data without the need for an ATA command to be sent to the storage device.

5.2.3 READ (6) and READ (10)

When StorageLynx receives a READ (6) or READ (10) command, the firmware issues a READ DMA ATA command to the ATA device. Since the most a single ATA command can request is 256 sectors, or 128 KB, the firmware breaks large requests into smaller requests. Therefore, StorageLynx can support the full 32 MB read request allowed by the READ (10) RBC command. Only one status packet is sent after all data transfer is complete. If an error occurs before the ATA command is completed, the firmware sends a response packet with a sense key of HARDWARE ERROR and no additional sense.

5.2.4 READ CAPACITY

The READ CAPACITY command does not require the TSB42AA9 to get information from the storage device to generate a response. Data is taken from the saved IDENTIFY DEVICE response information and the command response is generated.

5.2.5 TEST UNIT READY

The TEST UNIT READY command also does not require an ATA command to be issued by StorageLynx. The firmware reads the status register of the ATA device and waits for the BSY bit to be 0. When the BSY bit is 0, the DRDY bit is valid. If DRDY is 1, the firmware returns a GOOD status packet to the host. If it is 0, the firmware returns a status packet with a sense key of NOT READY with addition sense code of LOGICAL UNIT NOT READY CAUSE UNREPORTABLE.

5.2.6 VERIFY (10)

Receiving the VERIFY command from the host results in the firmware sending a READ VERIFY SECTORS ATA command to the ATA device. If the READ VERIFY SECTORS command completes properly, a GOOD SBP–2 status packet is returned to the host. Otherwise a status packet with a sense key of HARDWARE ERROR with no additional sense is returned.

5.2.7 WRITE (6) and WRITE (10)

When StorageLynx receives a WRITE (6) or WRITE (10) command from the host, the firmware issues a WRITE DMA ATA command to the ATA device. Since the most data one ATA command can request is 256 sectors, or 128 KB, the

firmware breaks large requests into smaller requests. This allows StorageLynx to support the full 32MB write request allowed by the WRITE (10) RBC command. Only one status packet is sent to the host after all data transfer is complete. If an ATA error occurs before the WRITE command is completed, the firmware sends a response with a sense key of HARDWARE ERROR and no additional sense to the host.

5.2.8 WRITE BUFFER

The WRITE BUFFER command allows the SBP–2 initiator to download and save new microcode in the target. The MODE parameter of the WRITE BUFFER command must be set equal to 0x05. Also, the length set inside the command must be a multiple of 512 because the ATA command translation must report a sector count and sectors are 512 bytes. A length value that is not a multiple of 512 results in a sense key of ILLEGAL REQUEST, with an additional sense code of COMMAND SEQUENCE ERROR, is reported.

5.2.9 PASS THROUGH

This command places given values into ATA registers. Data can be transferred in PIO or DMA mode at the highest support speed. The following table describes the command descriptor block (CDB) for this special command.

bit	0	1	2	3	4	5	6	7
0	Special Opcode (0x01)							
1	Value to place in **Device/Head** register							
2	Value to place in **Features** register							
3	Value to place in **Sector Count** register							
4	Value to place in **Sector Number** register							
5	Value to place in **Cylinder Low** register							
6	Value to place in **Cylinder High** register							
7	Value to place in **Command** register							
8	Reserved							PIO
9	Sector Count							

The PIO bit determines the mode for data transfer. If PIO = 1, the fastest supported PIO data transfer mode will be selected. If PIO = 0, the fastest supported DMA or UDMA mode will be selected. The 8-bit value Sector Count will be used by the link hardware to automate data transfer in PIO mode. This is the number of 512 byte sectors that must be transferred in PIO mode. If PIO = 0, this field is reserved. If sector count = 0, no data is transferred.

6 Memory Interfaces

This section describes the memory interfaces provided by the StorageLynx device. These memory interfaces are the flash PROM/EPROM interface for the storage of optional custom or test firmware and the 2-wire serial bus interface for the external storage of configuration ROM information. These two external memory access ports allow external memories to be programmed and reprogrammed while in-circuit. This in-circuit programmability also applies to the initial programming of blank parts.

6.1 External Flash PROM/EPROM

The StorageLynx internal 8052 processor can execute code from either its internal ROM or from an external flash PROM/EPROM device depending on the operational mode selected by the setting of the MODE[0:1] terminals at device power-up (see section 2.3). The specific external flash PROM/EPROM device that StorageLynx was designed to work with is the AMD (AM29LV010) 128K x 8-bit flash memory. However, any memory with a similar erase mechanism, comparable access time, and command set compatible with the Joint Electronic Devices Engineering Council (JEDEC) single-power-supply flash standard will work.

Using flash memory allows users to download code to memories in-circuit; however, nonflash memories can be used if in system programmability is not an issue, assuming the access times are comparable. (see section 7). The internal 8052 processor running at 50 MHz with instruction fetches three clocks long allows for a maximum flash access time of around 60 ns. The internal 8052 running at 25 MHz with instruction fetches three clocks long, allows for a maximum external flash PROM/EPROM access time of around 90 ns. See section 9 for more information on selecting external memories.

Custom or test program code, can be downloaded to an external flash PROM device from a host PC via 1394, using a programming application provided by Texas Instruments. The flash erase/write process requires the programming application to supply a password to enable StorageLynx flash write algorithm. UNLOCK requests to the device should be written to FFFF F001 0104h with the password 9ABC DEF0h. Data transfers to the flash must be written to the address: FFFF F001 010Ch. Any other access will cause the flash to be locked. Write requests, except the last write request, must have a data length of 256 bytes. The flash write algorithm initiates the first 256 byte write to the flash PROM beginning at address 0000h (14 bit address) and increments the address by 256 for each consecutive write request from the host PC. The last block of data must be less than 256 bytes. After this last data block is written to the flash, the device locks access to the flash again and returns to the idle state. The protocol for downloading new code to the external ROM is further explained in the AM29LV010 datasheet, revision C (AM29LV010B data sheet, revision C). The datasheet for the AM29LV010 also describes the sector erase/write algorithm(AM29LV010B data sheet, revision C).

6.2 Serial EEPROM

An external serial EEPROM allows changes and updates to be made easily to the system configuration ROM information. The configuration ROM information stored in the external serial EEPROM is loaded into the internal parameter RAM at power-up to allow quicker responses to configuration ROM read requests from the system host and faster access to device parameters. Both internal and external (overflow) configuration storage spaces remain accessible to the embedded processor through the parameter access register at 68h (see section 3.2.25) while StorageLynx is powered up.

Configuration ROM information in the external serial EEPROM can be modified using the StorageLynx programming application via the 1394 interface, thus removing the need for preprogrammed parts. The TSB42AA9 also supports writes to blank serial EEPROMs. Access to the serial EEPROM is locked, and UNLOCK requests require the programming application to submit the password, 1234 5678h, to the StorageLynx address FFFF F001 0100h. After the unlock is complete, the user must perform a block write request of exactly 256 bytes to address FFFF F001 0108h. After this write is complete, the serial EEPROM is locked again (only one write is allowed since only 256 byte Configuration ROM is supported). A write of less than 256 bytes is rejected. An access to any other address other than FFFF F001 0108h will cause the serial EEPROM access to be locked. The serial EEPROM used must be greater than 256 bytes in size.

7 Interface Timing

7.1 ATA/ATAPI Interface Timing

StorageLynx conforms to critical and functional timing requirements for PIO modes 0–4, Multiword DMA modes 0–2, and Ultra DMA modes 0–4, per the ATA/ATAPI–5 v3.0 specification[1]. Refer to this document for details of the ATA interface timing supported for these modes.

7.2 Serial EEPROM Interface Timing

StorageLynx conforms to the standard 2-wire serial bus timing requirements for low voltage serial EEPROMs. The SCL signal is equivalent to a 100 kHz (maximum) clock signal.

7.3 External Flash PROM Interface

The internal 8052 can access external flash via the Flash PROM/EPROM interface. Flash read timing for this interface is shown in Table 7–1. A timing diagram is shown in Figure 7–1.

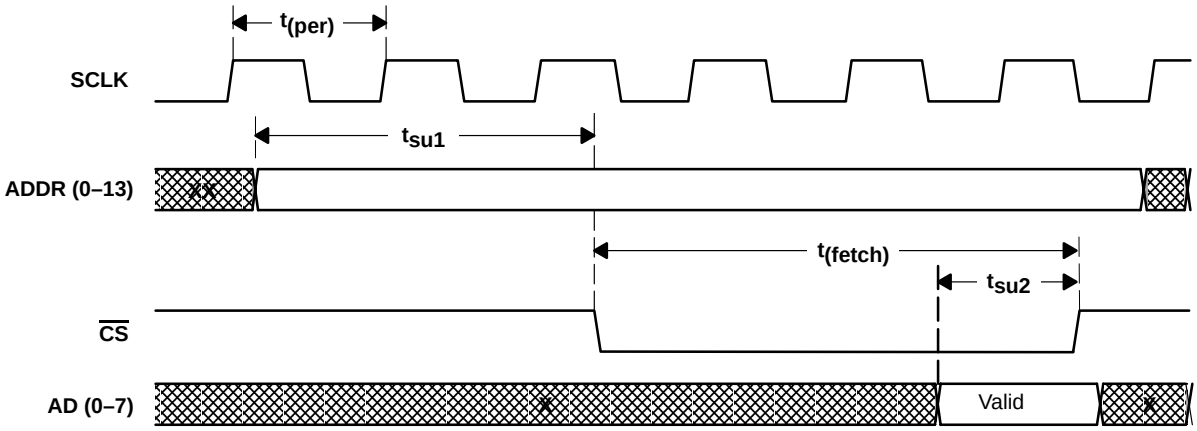


Figure 7–1. External Flash Instruction Fetch Timing

Table 7–1. Instruction Fetch Timing Parameters

PARAMETER	DESCRIPTION	MIN (50 MHz)	MIN (25 MHz)
tper	Internal 8052 clock period	20 ns	40 ns
tfetch	Instruction fetch time	3 SCLK cycles	3 SCLK cycles
tsu1	Setup time from address valid until $\overline{CS}$ active	2 SCLK cycles	2 SCLK cycles
tsu2	Data setup time to chip select	1 SCLK cycle	1 SCLK cycle

[1]American National Standards Institute, ANSI NCTIS 317-1998, *AT Attachment With Packet Interface Extension—(ATA/ATAPI-5 v3.0)*

8 Electrical Characteristics

8.1 Absolute Maximum Ratings Over Free-Air Temperature Range (Unless Otherwise Noted)

Supply voltage range, V_{CC} . . . . . –0.5 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2) . . . . . ±20 mA
Continuous total power dissipation . . . . . See Maximum Dissipation Rating Table
Operating free-air temperature range, T_A TSB42AA9 . . . . . 0°C to 70°C
TSB42AA9I . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This applies to external input and bidirectional buffers.
2. This applies to external output and bidirectional buffers.

MAXIMUM DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PZT	1500 mW	16.9 mW/°C	739.5 mW	486 mW

8.2 Package Thermal Resistance (R_θ) Characteristics†

PARAMETER	TEST CONDITIONS	PZ PACKAGE			UNIT
		MIN	NOM	MAX	
Junction-to-ambient thermal resistance, $R_{\theta JA}$	Board Mounted, No air flow		59		°C/W
Junction-to-case thermal resistance, $R_{\theta JC}$			13		°C/W
Junction temperature, T_J				115	°C

† Thermal resistance characteristics vary depending on die and leadframe pad size as well as mold compound. These values represent typical die and pad sizes for the package. The R value decreases as the die or pad sizes increases. Thermal values represent PWB bands with minimal amounts of metal.

8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3.0	3.3	3.6	V
Input voltage, V_I		0		V_{CC}	V
Output voltage, V_O		0		V_{CC}	V
High-level input voltage, V_{IH}		0.7V_{CC}		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.3V_{CC}	V
Operating free-air temperature, T_A	TSB42AA9	0	25	70	°C
	TSB42AA9I	–40	25	85	

8.4 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –12 mA	$0.8V_{CC}$			V
		I_{OH} = –8 mA	$0.8V_{CC}$			
V_{OL}	Low-level output voltage	I_{OL} = 12 mA			$0.2V_{CC}$	V
		I_{OL} = 8 mA			$0.2V_{CC}$	
I_{IL}	Low-level input current	$V_I = V_{IL}$			–1	µA
I_{IH}	High-level input current	$V_I = V_{IH}$			1	µA
I_{OZ}	High-impedance output current	$V_O = V_{CC}$ or GND			±20	µA
I_{CC}	Static supply current	$V_O = V_{CC}$ or GND		40		mA

9 Memory Recommendations for StorageLynx

The StorageLynx processor can operate at two speeds, 25 MHz and 50 MHz. If optional external memory (FLASH or EPROM) is used to store the program code, differing access times are required dependent on the operating frequency of the processor. Nonperformance critical applications such as most ATAPI and some ATA (HDD) devices can benefit from operating the microcontroller at the slower 25MHz operating frequency, thus allowing the use of slower, more readily available FLASH or EPROM devices.

9.1 Choice of Internal or External Program Code

StorageLynx has an internal 8052 processor that is used for instruction translation. It translates RBC commands into equivalent ATA commands that are executable by the ATA controller embedded within a HDD (or other storage device). The program code that the internal 8052 executes by default is stored on masked-ROM, embedded within the StorageLynx device.

One of the benefits of the StorageLynx device is that it allows user the option of modifying the program code, optimizing it for their specific application. StorageLynx has been designed to allow the program code to be alternately stored within an optional, external EPROM or FLASH device. This configuration mode is achieved by placing the MODE [0:1] inputs into a [0,1] state. Entering this mode disables the internal masked ROM and allows the microcontroller to fetch its program code from external FLASH/EPROM.

9.2 Access Time Requirements of FLASH or EPROM

The maximum access time of the optional external EPROM or FLASH device is dependent on the chosen speed of operation of the 8052 microcontroller within StorageLynx. The 8052 can be operated at either 25 MHz or 50 MHz. The speed of operation of the 8052 is selected upon power-up when the UART_RXD (a dual use pin) is sampled. If the pin is pulled up, the StorageLynx internal clock is set to 50 MHz. If the pin is sampled in a low state, the StorageLynx internal clock is set to 25 MHz.

Another variable involved in the choice of access times is whether the customer wishes to program the device during the manufacturing flow while the memory device is on the board. This would be an option if FLASH memory were used. If this capability is not required, EPROMs make a better choice for external program code storage.

The table below lists the required access times of external nonvolatile memory based on the frequency the StorageLynx 8052 is operated at and whether on-board programming (via the 1394 cable) is being used:

	Execute program code from external memory	Program chip via 1394 cable (applicable for FLASH only)
25 MHz	90 nS	80 nS
50 MHz	60 nS	80 nS

If the ATA or ATAPI application does not require the use of external program code storage, there are no additional requirements to operate out of internal ROM at 50 MHz instead of 25 MHz. The only action required is to pull the UART_RXD pin high with a 10K OHM resistor.

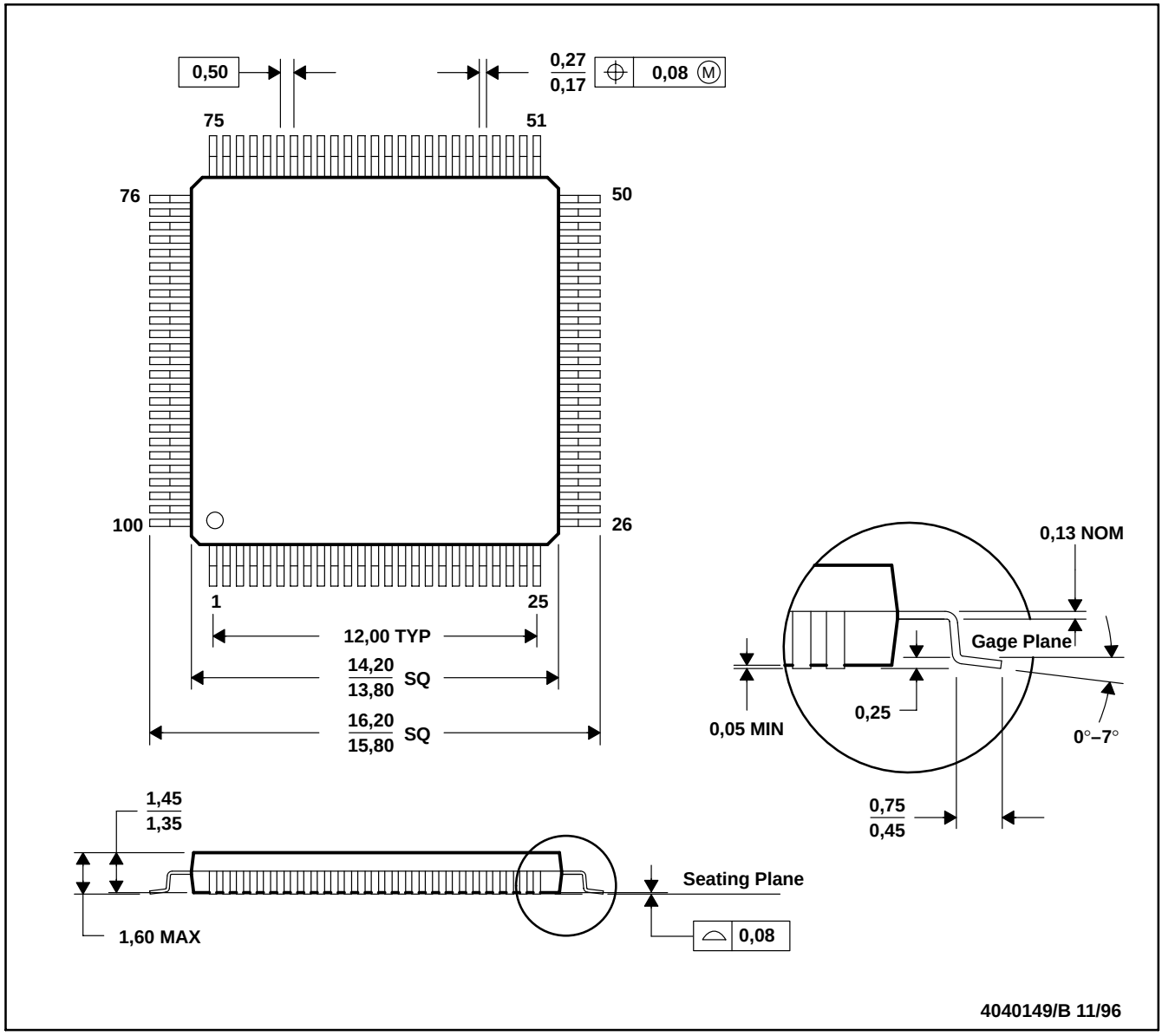
9.3 Memory Usage

The following table contains information on what information can be stored in the various memories accessed by StorageLynx.

MEMORY TYPE	USAGE
Internal ROM of StorageLynx	Contains original firmware (program code) for the embedded processor
Flash/EPROM	May contain customer-modified firmware for the embedded processor
Serial EEPROM	Stores Configuration ROM information

10 Mechanical Data

PZT (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSB42AA9IPZT	ACTIVE	TQFP	PZT	100	90	None	Call TI	Level-3-235C-168 HR
TSB42AA9PZT	OBSOLETE	TQFP	PZT	100		None	Call TI	Call TI
TSB42AA9PZTR	OBSOLETE	TQFP	PZT	100		None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.