DUAL 6A AND 1A LOW DROPOUT POSITIVE FIXED OUTPUT REGULATOR

FEATURES

- **Guaranteed to provide 1.5V and 2.5V Supplies with 3.1V input.**
- **Fast Transient Response**
- **1% Voltage Reference Initial Accuracy**
- Built in Thermal Shutdown

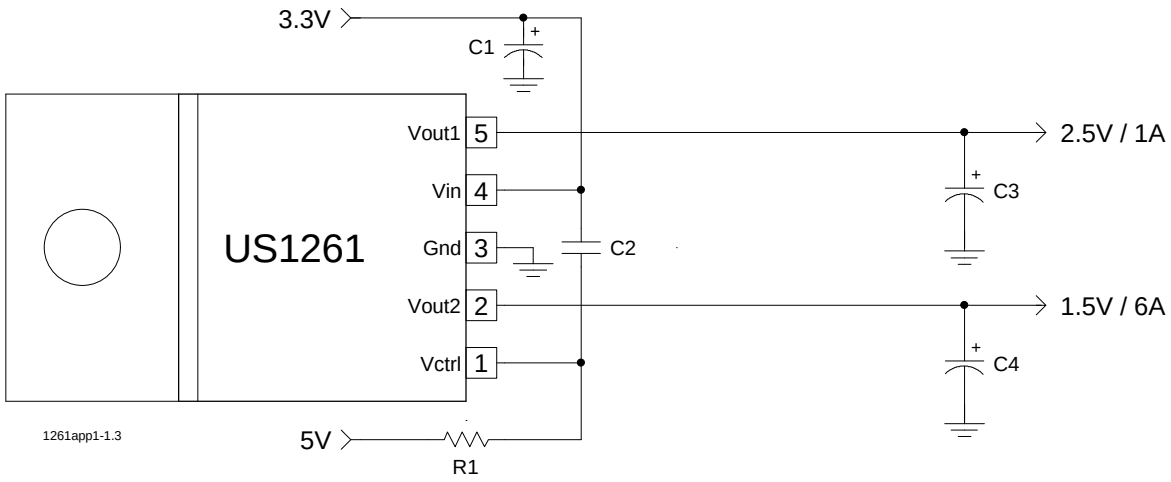
APPLICATIONS

- **Pentium II Processor Applications**

DESCRIPTION

The US1261 product using a **proprietary process** combines a dual low dropout regulators with fixed outputs of 1.5V and 2.5V in a **single package** with the 1.5V output having a minimum of **6A** and the 2.5V having a **1A** output current capability. This product is specifically designed to provide well regulated supplies from **3.3V to generate 1.5V for GTL+ termination resistor supply and 2.5V clock supply for the new generation of the Pentium II processor** applications.

TYPICAL APPLICATION



Typical application of US1261 in a Pentium II processor application

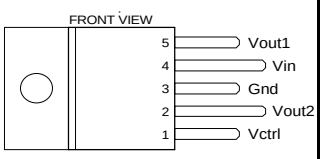
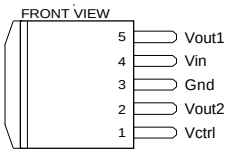
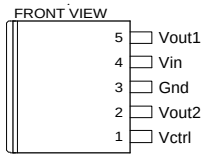
PACKAGE ORDER INFORMATION

Tj (°C)	5 PIN PLASTIC TO220(T)	5 PIN PLASTIC TO263(M)	5 PIN PLASTIC POWER FLEX(P)
0 TO 150	US1261CT	US1261CM	US1261CP

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Vin) 10V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C TO 150°C
Operating Junction Temperature Range ..... 0°C TO 150°C

PACKAGE INFORMATION

7 PIN PLASTIC TO220	7 PIN PLASTIC TO263	7 PIN POWER FLEX (P)
		
θ_{JT} =2.7°C/W θ_{JA} =60°C/W	θ_{JA} =30°C/W for 1"sq pad	θ_{JA} =30°C/W for 1"sq pad

ELECTRICAL SPECIFICATIONS

Unless otherwise specified ,these specifications apply over ,Cin=1 uF,Cout=100uF,and Tj=0 to 150°C.Typical values refer to Tj=25°C. Ifl=6A for output #2 & 1A for output #1.Vctrl=5V,Vin=3.3V.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Vctrl Input Voltage			3.0			V
Output Voltage #2	Vo2	Io=10mA, Tj=25°C Io=10mA	1.485 1.470	1.500 1.500	1.515 1.530	V
Output Voltage #1	Vo1	Io=10mA, Tj=25°C Io=10mA	2.462 2.425	2.500 2.500	2.537 2.575	V
Line Regulation		Io=10mA, 3.1V<Vin<3.6V		0.2		%
Load Regulation (note 1)		10mA<Io<Ifl		0.4		%
Dropout Voltage (output #2)		Note 2, Io=6A, Vctrl=4.75V			1.3	V
Dropout Voltage (output #1)		Note 2, Io=1A, Vctrl=4.75V		0.4	0.6	V
Current Limit (output #2)		dVo=100mV	6.1			A
Current Limit (output #1)		dVo=100mV	1.1			A
Minimum Load Current (note 3)				5	10	mA
Thermal Regulation		30 mS PULSE,Io=Ifl		0.01	0.02	%/W
Ripple Rejection		f=120HZ ,Co=25uF Tan Io=0.5*Ifl		70		dB
Temperature Stability		Io=10mA		0.5		%
Long Term Stability		Tj=125°C,1000 Hrs		0.3		%
RMS Output Noise		10hz<f<10khz		0.003		%Vo

Note 1 : Low duty cycle pulse testing with Kelvin connections are required in order to maintain accurate data.

Note 2 : Drop-out voltage is defined as the minimum differential voltage between Vin and Vout required to maintain regulation at Vout. It is measured when the output voltage drops 1% below its nominal value.

Note 3 : Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that it automatically maintains this current.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
2	Vout2	The output #2 (high current) of the regulator. A minimum of 100uF capacitor must be connected from this pin to ground to insure stability.
5	Vout1	The output #1 (low current) of the regulator. A minimum of 100uF capacitor must be connected from this pin to ground to insure stability.
4	Vin	The power input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than both Vout pins by the amount of the dropout voltage(see datasheet) in order for the device to regulate properly.
3	Gnd	This pin is connected to GND. It is also the TAB of the package.
1	Vctrl	The control input pin of the regulator. This pin via a 10Ω resistor is connected to the 5V supply to provide the base current for the pass transistor of both regulators. This allows the regulator to have very low dropout voltage which allows one to generate a well regulated 2.5V supply from the 3.3V input. A high frequency, 1 uF capacitor is connected between this pin and Vin pin to insure stability.

BLOCK DIAGRAM

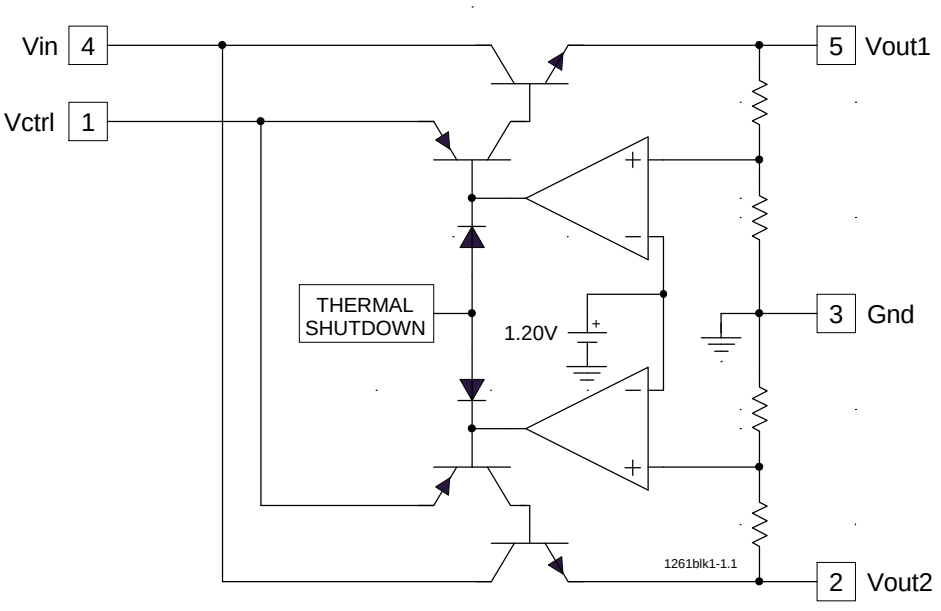


Figure 1 - Simplified block diagram of the US1261

APPLICATION INFORMATION

Introduction

The US1261 is a dual fixed output Low Dropout (LDO) regulator available in a 5 pin TO-220 or TO-263 packages. This voltage regulator is designed specifically for PentiumII processor applications requiring 2.5V and 1.5 V supplies, **eliminating the need for a second regulator resulting in lower overall system cost**. The US1261 is designed to take advantage of 5V supply to provide the drive for the pass transistor, allowing 2.5V supply to be generated from 3.3V input.This feature improves the power dissipation of the 2.5V regulator substantially allowing a smaller heat sink to be used for the application. Compared to the US1260 dual adjustable regulator, the US1261 includes the resistor dividers that are otherwise needed with the US1260, eliminating 4 external components and their tolerances, resulting in a more accurate initial accuracy for each output voltage. Other features of the device include; fast response to sudden load current changes, such as GTL+ termination application and thermal shutdown protection to protect the device if an overload condition occurs.

Stability

The US1261 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for the microprocessor applications use standard electrolytic capacitors with typical ESR in the range of 50 to 100 mΩ and the output capacitance of 500 to 1000uF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The US1261 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100uF aluminum electrolytic capacitor with the maximum ESR of 0.3Ω such as Sanyo, MVGX series ,Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response. The US1261 also requires a 1 uF ceramic capacitor connected from Vin to Vctrl and a 10Ω, 0.1W resistor in series with Vctrl pin in order to further insure stability.

Thermal Design

The US1261 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C ,it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. Two examples are given which shows the steps in selecting the proper regulator heat sink for driving the Pentium II processor GTL+ termination resistors and the Clock IC using 1261 in TO220 and TO-263 packages.

Example # 1

Assuming the following specifications :

$V_{IN} = 3.3V$

$V_{OUT\,2} = 1.5\ V$

$V_{OUT\,1} = 2.5\ V$

$I_{OUT\,2\,MAX} = 5.4A$

$I_{OUT\,1\,MAX} = 0.4\ A$

$T_A = 35°C$

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as :

1) Calculate the maximum power dissipation using :

$$P_D = I_{OUT1} \times (V_{IN} - V_{OUT1}) + I_{OUT2} \times (V_{IN} - V_{OUT2})$$

$$P_D = 0.4 \times (3.3 - 2.5) + 5.4 \times (3.3 - 1.5) = 10\ W$$

2) Select a package from the datasheet and record its junction to case (or Tab) thermal resistance.
Selecting TO220 package gives us :

$\theta_{JC} = 2.7°C/W$

3) Assuming that the heat sink is Black Anodized, calculate the maximum Heat sink temperature allowed :
Assume , θ_{CS} = 0.05 °C/W (Heat sink to Case thermal resistance for Black Anodized)

$$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$$

$$T_S = 135 - 10 \times (2.7 + 0.05) = 107.4\ °C$$

4) With the maximum heat sink temperature calculated in the previous step, the Heat Sink to Air thermal resistance θ_{SA} is calculated as follows :

$$\Delta_T = T_S - T_A = 107.4 - 35 = 72.4\ °C$$

$$\theta_{SA} = \frac{\Delta_T}{P_D}$$

$$\theta_{SA} = \frac{72.4}{10} = 7.24\ °C/W$$

5) Next , a heat sink with lower θ_{SA} than the one calculated in step 4 must be selected. One way to do this is to simply look at the graphs of the “Heat Sink Temp Rise Above the Ambient” vs. the “Power Dissipation” and

select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermaloy meet this criteria.

	Air Flow (LFM)				
	0	100	200	300	400
Thermalloy	7021B	7020B	6021PB	7173D	7141D
AAVID	593101B	551002B	534202B	577102B	576802B

Note : For further information regarding the above companies and their latest product offering and application support contact your local representative or the numbers listed below:

Thermalloy PH# (214) 243-4321
AAVID PH# (603) 528-3400

Example # 2 **:**
Assuming the following specifications :

$V_{IN} = 3.3V$

$V_{OUT\,2} = 1.5\ V$

$V_{OUT\,1} = 2.5\ V$

$I_{OUT\,2\,MAX} = 1.5A$

$I_{OUT\,1\,MAX} = 0.2\ A$

$T_A = 35°C$

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as :
1) Calculate the maximum power dissipation using :

$$P_D = I_{OUT1} \times (V_{IN} - V_{OUT1}) + I_{OUT2} \times (V_{IN} - V_{OUT2})$$

$$P_D = 0.2 \times (3.3 - 2.5) + 1.5 \times (3.3 - 1.5) = 2.86\ W$$

2) Assuming a TO-263 surface mount package, the junction to ambient thermal resistance of the package is:

$\theta_{JA} = 30°C / W$ for 1" square pad area

3) The maximum junction temperature of the device is calculated using the equation below :

$$T_J = T_A + P_D \times \theta_{JA}$$

$$T_J = 35 + 2.86 \times 30 = 121\ °C$$

Since this is lower than our selected 135°C maximum junction temperature (150°C is the thermal shutdown of the device), TO-263 package is a suitable package for our application.

Layout Consideration

The US1261 like all other high speed linear regulators need to be properly laid out to insure stable operation. The most important component is the **output capacitor, which needs to be placed close to the output pin and connected to this pin using a plane connection with a low inductance path.**

TYPICAL APPLICATION

PENTIUM II™ APPLICATION

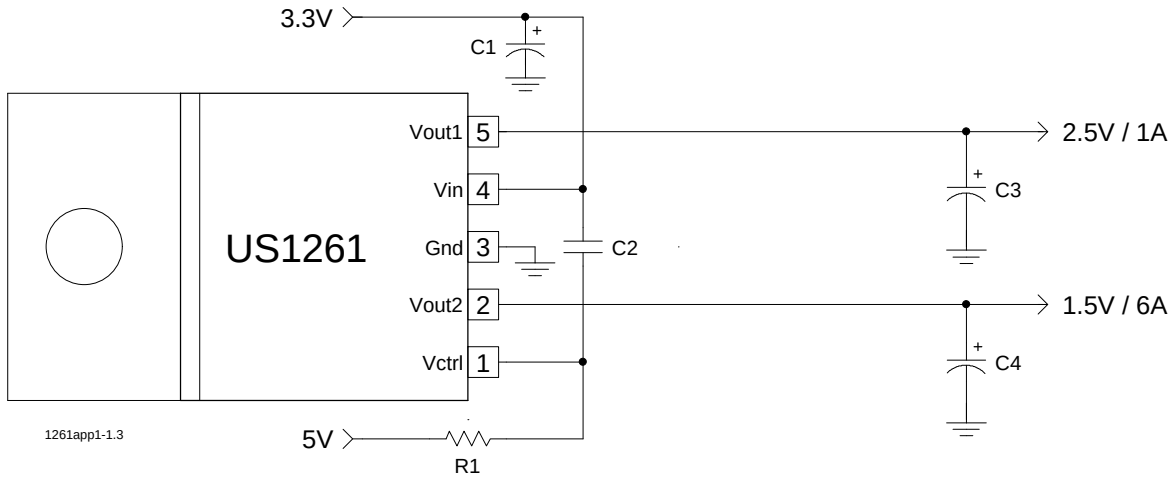


Figure 4 - Typical application of US1261 in the Pentium II™ design with the 1.5V output providing for GTL+ termination while 2.5V supplies the clock chip.

Notes: Pentium II is trade mark of Intel Corp.

Ref Desig	Description	Qty	Part #	Manuf
U1	Dual LDO Regulator	1	US1261CM	Unisem
C1,C4	Capacitor	2	Elect,680uF,EEUFA1A681L	Panasonic
C3	Capacitor	1	Elect,220uF,6.3V,ECAOJFQ221	Panasonic
C2	Capacitor	1	Ceramic,1uF,16V,Z5U	
R1	Resistor	1	3Ω, 0.1W , 0805 SMT	Panasonic
HS1	Heat Sink	1)Use 1" Square Copper Pad area if Iout2<1.7A & Iout1<0.2A. 2)For Iout2<3A & Iout1<0.5A Use US1261CT and Thermalloy 6030B 3)For Iout2<5.4A & Iout1<0.5A Use US1261CT and Thermalloy 7021B		