

# High Speed Power Driver

## FEATURES

- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

## DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both  $V_s$  and  $V_c$  can independently range from 5V to 40V. For additional application details, see the UC1707/3707 data sheet.

The UC1705 is packaged in an 8-pin hermetically sealed Cerdip for -55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

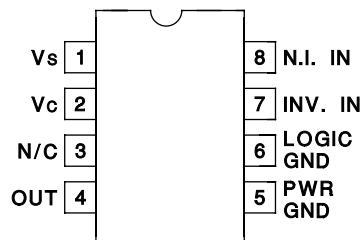
## TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

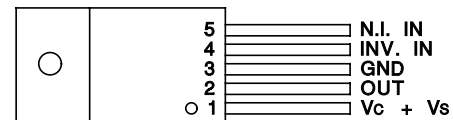
$\overline{OUT} = \overline{INV} \text{ and } \overline{N.I.}$   
 $\overline{OUT} = INV \text{ or } N.I.$

## CONNECTION DIAGRAMS

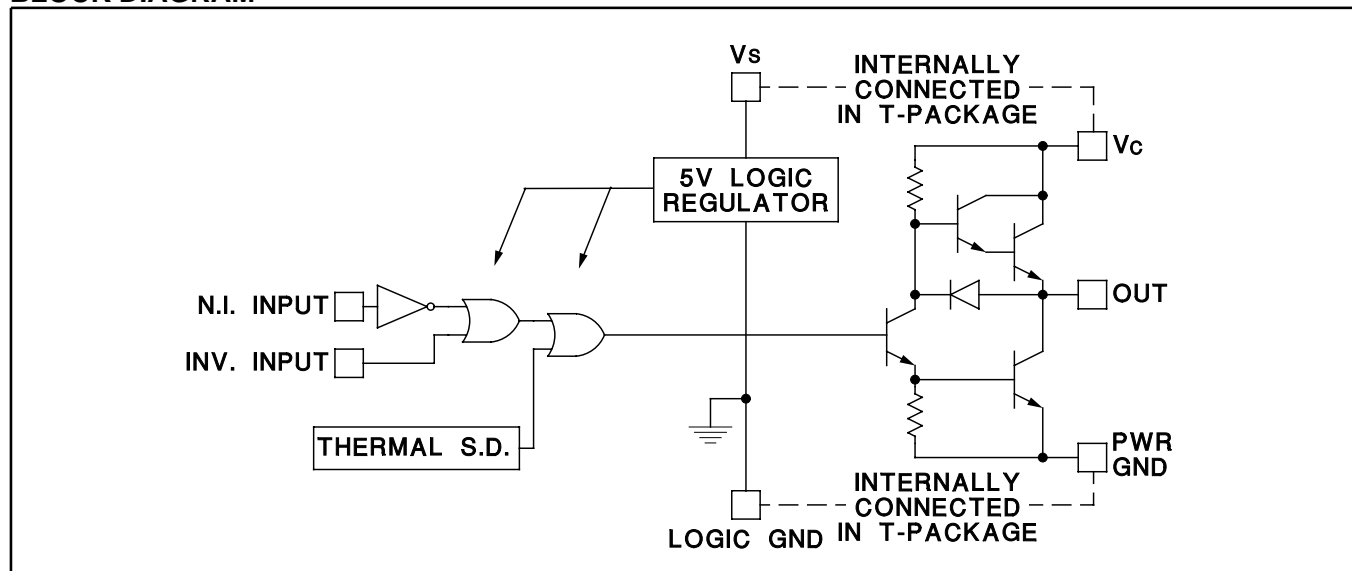
DIL-8 MINIDIP, SOIC-8  
(TOP VIEW)  
N or J Package, D Package



5-PIN TO-220  
(TOP VIEW)  
T Package



## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, $V_{IN}$	40V	40V	40V
Collector Supply Voltage, $V_C$	40V	40V	40V
Output Current (Source or Sink)			
Steady-State	$\pm 500\text{mA}$	$\pm 500\text{mA}$	$\pm 1.0\text{A}$
Peak Transient	$\pm 1.5\text{A}$	$\pm 1.0\text{A}$	$\pm 2.0\text{A}$
Capacitive Discharge Energy	20 $\mu\text{J}$	15 $\mu\text{J}$	50 $\mu\text{J}$
Digital Inputs (See Note)	5.5V	5.5V	5.5V
Power Dissipation at $T_A = 25^\circ\text{C}$ (See Note)	1W	1W	3W
Power Dissipation at $T_A$ (Leads/Case) = $25^\circ\text{C}$ (See Note)	3W	2W	25W
Operating Temperature Range	$0^\circ\text{C}$ to $+70^\circ\text{C}$	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	$0^\circ\text{C}$ to $+70^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 seconds)	$300^\circ\text{C}$	$300^\circ\text{C}$	$300^\circ\text{C}$

Note: All currents are positive into, negative out of the specified terminal.

Digital Drive can exceed 5.5V if input current is limited to 10mA

Consult Packaging Section of Databook for thermal limitations and considerations of package.

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1705,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2705, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3705;  $V_S = V_C = 20\text{V}$ ,  $T_A = T_J$ .

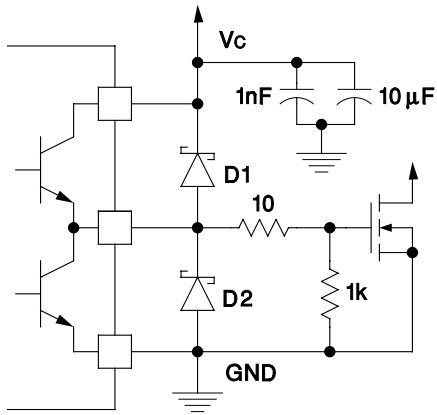
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_S$ Supply Current	$V_S = 40\text{V}$ , (Outputs High, T Pkg)		6	8	mA
	$V_S = 40\text{V}$ , (Outputs Low, T Pkg)		8	12	mA
$V_C$ Supply Current (N, J Only)	$V_C = 40\text{V}$ , Outputs Low		2	4	mA
$V_C$ Leakage Current (N, J Only)	$V_S = 0$ , $V_C = 30\text{V}$		0.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	$V_I = 0$		-0.6	-1.0	mA
Input Leakage	$V_I = 5\text{V}$		0.05	0.1	mA
Output High Sat., $V_C$ - $V_O$	$I_O = -50\text{mA}$			2.0	V
	$I_O = -500\text{mA}$			2.5	V
Output Low Sat., $V_O$	$I_O = 50\text{mA}$			0.4	V
	$I_O = 500\text{mA}$			2.5	V
Thermal Shutdown			155		$^\circ\text{C}$

**TYPICAL SWITCHING CHARACTERISTICS:**  $V_S = V_C = 20\text{V}$ ,  $T_A = 25^\circ\text{C}$ . Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT $C_L =$			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
$V_C$ Cross-Conduction	Output Rise	25			ns
Current Spike Duration	Output Fall	0			ns

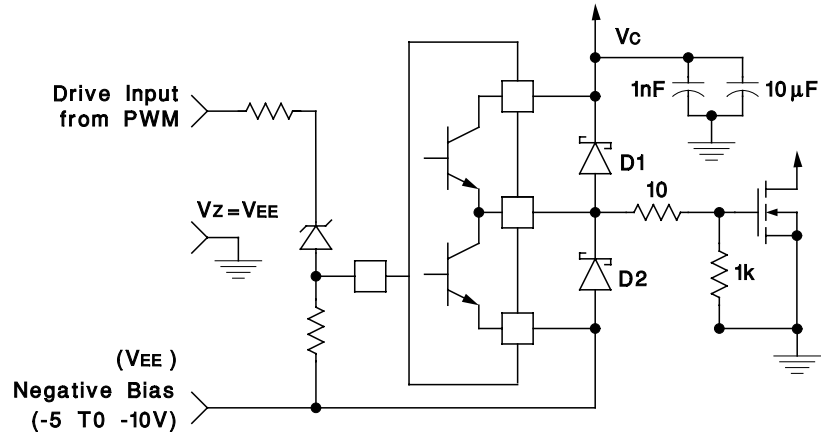
## APPLICATIONS

**Power MOSFET Drive Circuit**



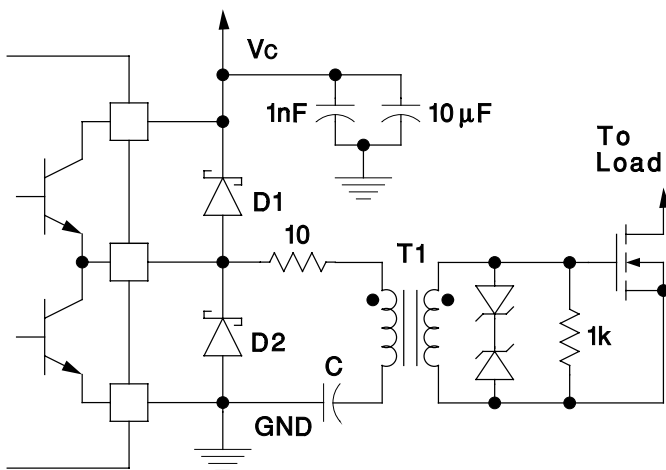
D1, D2: UC3611 Schottky Diodes

**Power MOSFET Drive Circuit using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs.**



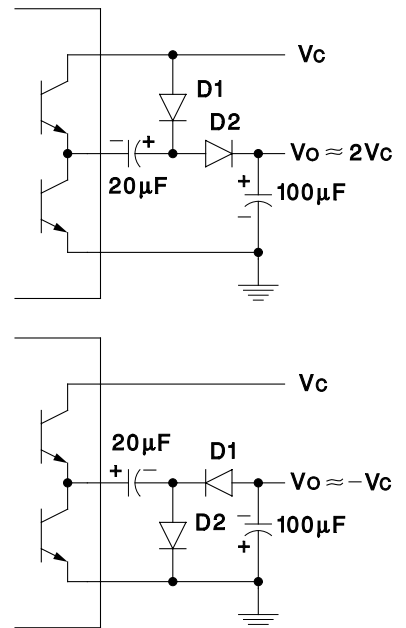
D1, D2: UC3611 Schottky Diodes

**Transformer Coupled MOSFET Drive Circuit**



D1, D2: UC3611 Schottky Diodes

**Charge Pump Circuits**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9579801M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9579801MPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9579801VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	Level-NC-NC-NC
UC1705J	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1705J883B	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1705L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC2705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2705J	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
UC2705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3705DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3705DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3705J	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
UC3705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3705NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3705T	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-NC-NC-NC
UC3705TG3	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

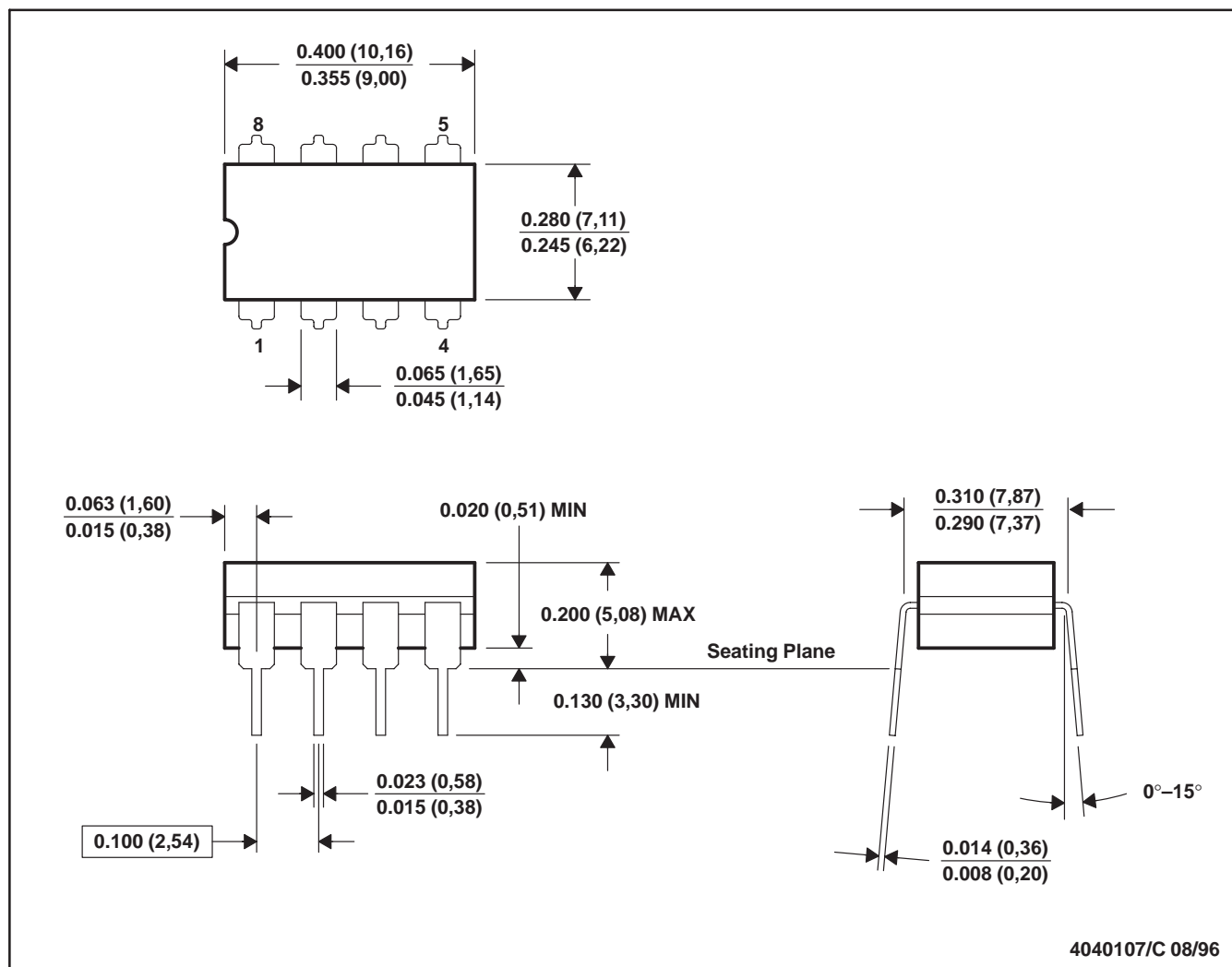
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## JG (R-GDIP-T8)

## CERAMIC DUAL-IN-LINE

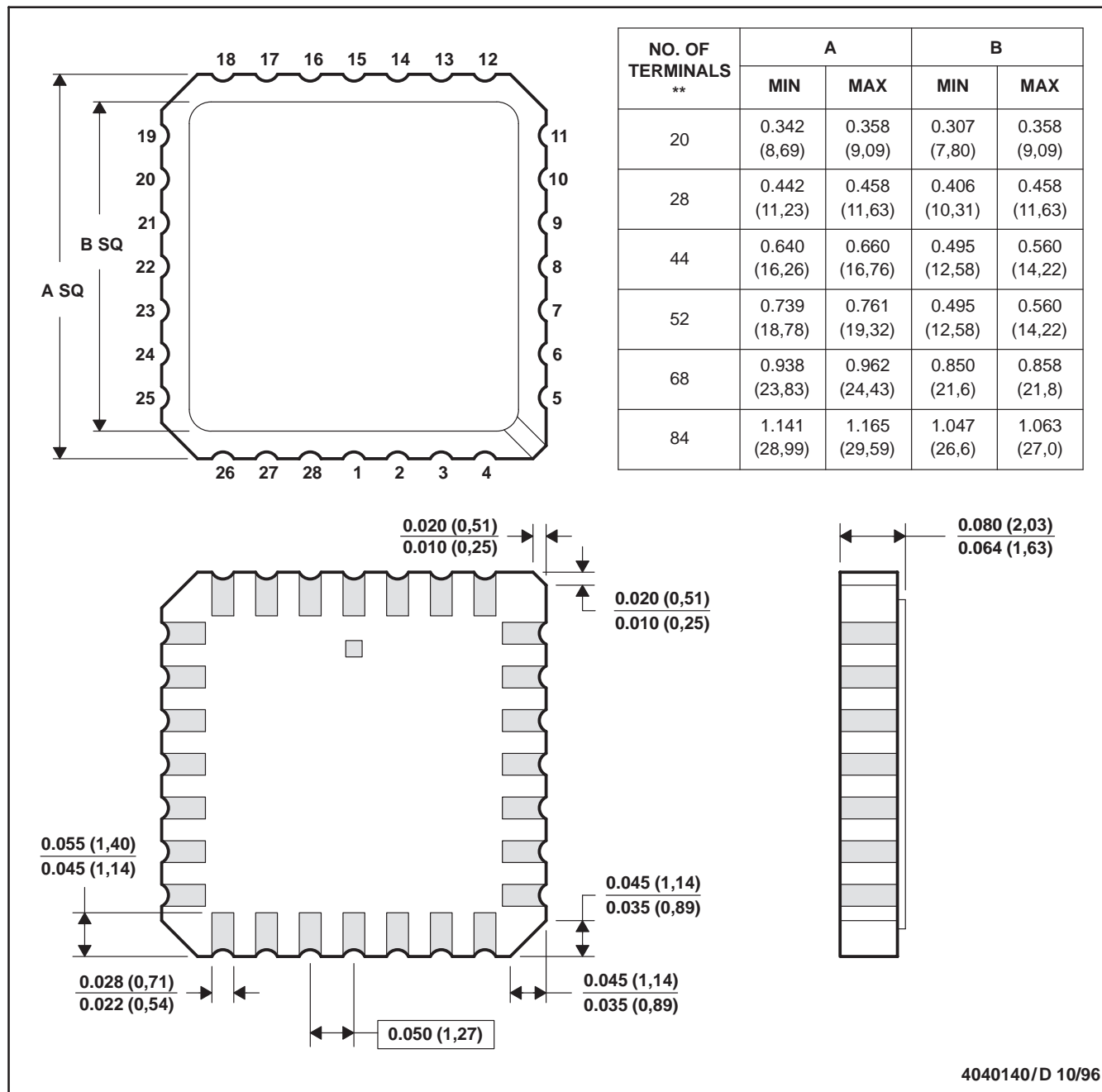


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification.
  - E. Falls within MIL STD 1835 GDIP1-T8

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

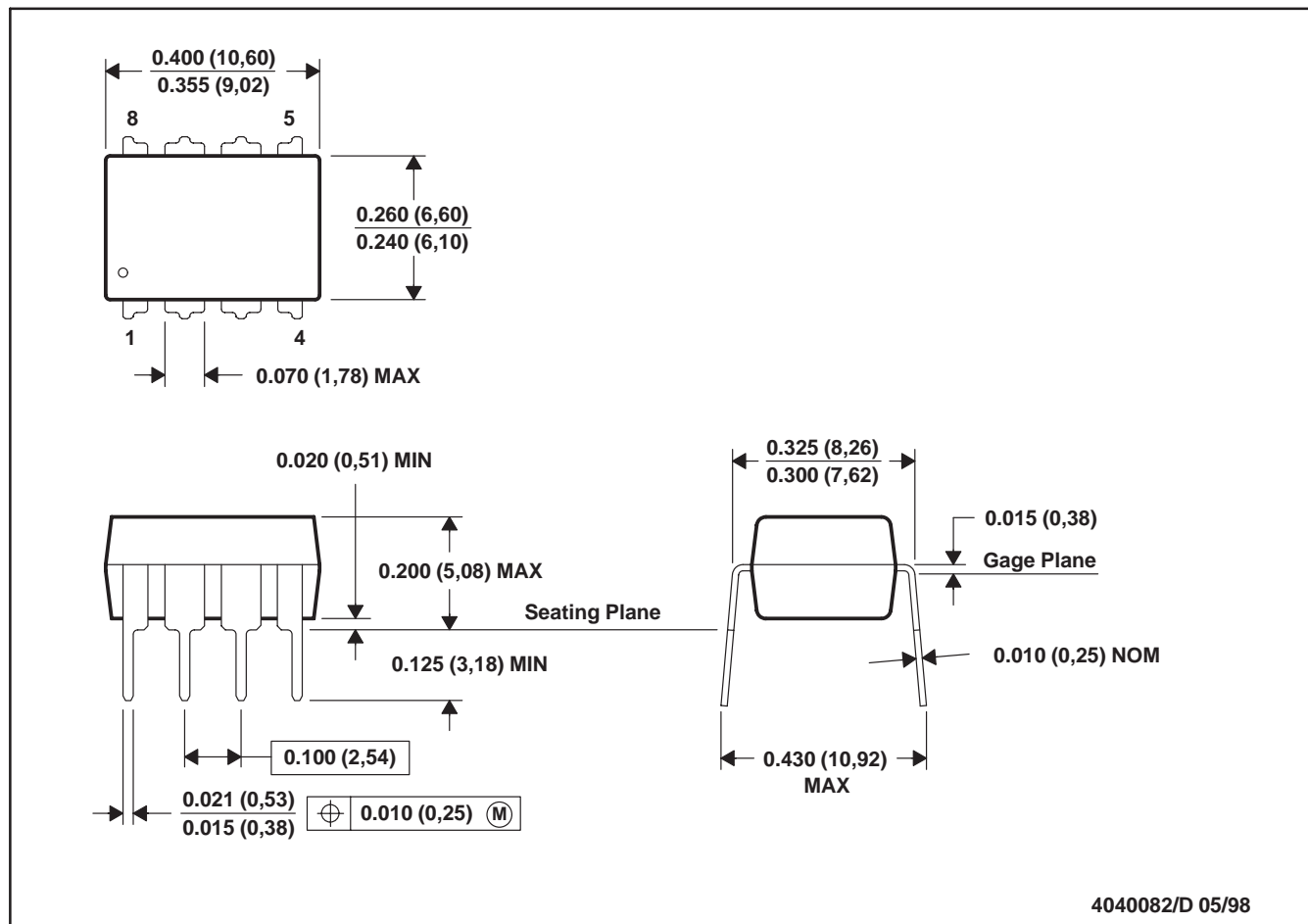
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

## P (R-PDIP-T8)

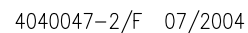
## PLASTIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

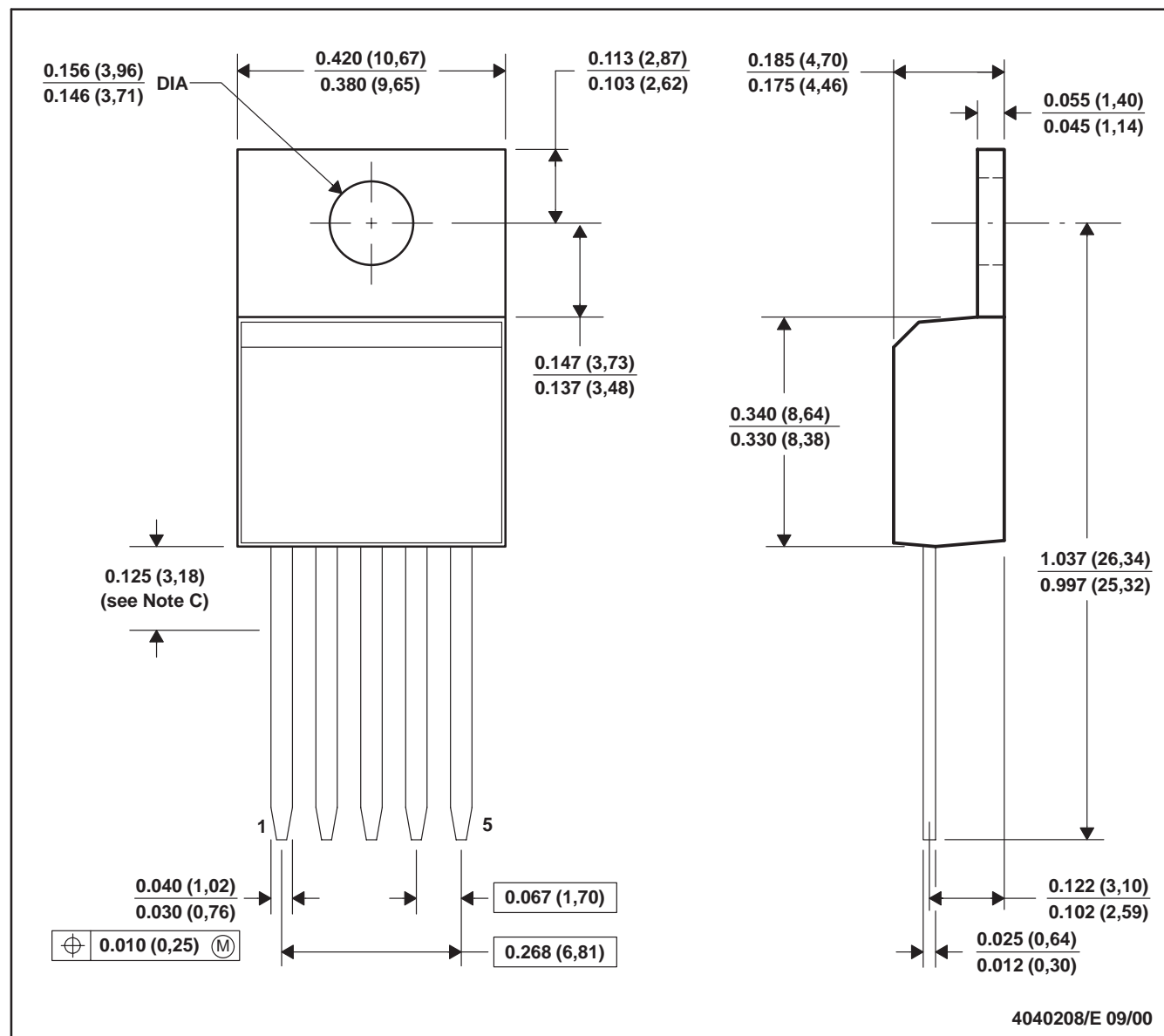




A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-012 variation AA.

## KC (R-PSFM-T5)

## PLASTIC FLANGE-MOUNT



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Lead dimensions are not controlled within this area.  
 D. All lead dimensions apply before solder dip.  
 E. The center lead is in electrical contact with the mounting tab.

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