- **Fully Integrated Dual Clock Synthesizer and 16-Bit Pixel Port True-Color RAMDAC**
- **Two Phase-Locked-Loop (PLL) Synthesizers Provide Independently Controlled Video and Memory Clock Outputs**
- **Functionally Interchangeable with STG1703**
- **On-Chip PLL Clock Reference Requires Single External Crystal**
- **16-Bit Pixel Port Supports VGA High-Color and True-Color Standards Up to 170 MHz**
- **Programmable Power-Down Features**
- **On-Chip Cyclic Redundancy Check (CRC) Test**

description

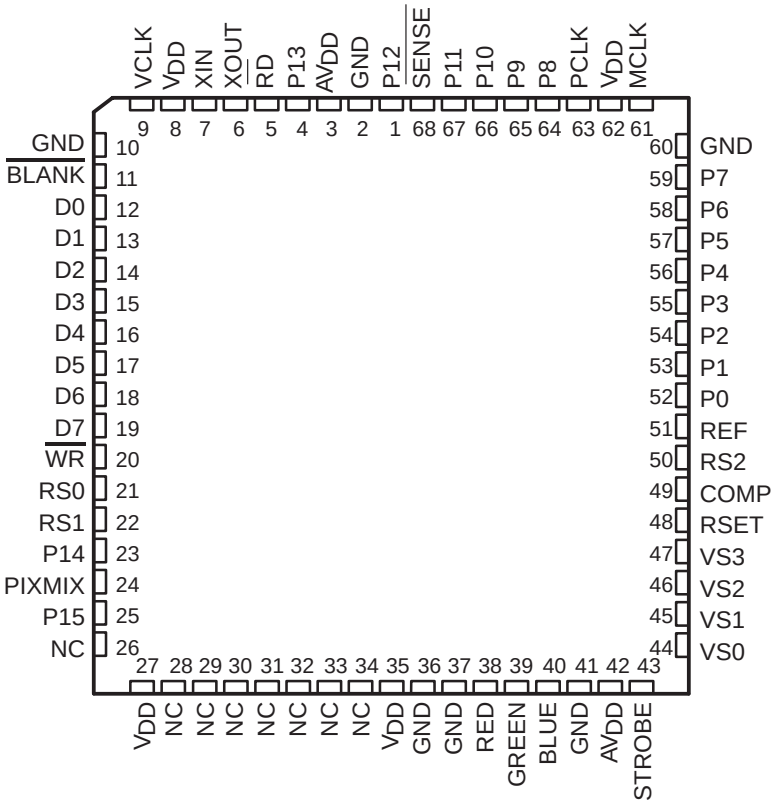
The TVP3703 is a super video graphics array (SVGA) compatible, true-color CMOS RAMDAC with integrated clock synthesizers that can provide the memory and pixel clock signals for a PC graphics subsystem. The video clock can be one of two VGA base frequencies or fourteen Video Electronics Standards Association (VESA) standard frequencies which can also be reprogrammed through the standard micro port interface.

The memory clock output is also user programmable at frequencies up to 80 MHz. The pixel modes supported by the TVP3703 include:

- Serializing 16-bit pixel port providing 170 MHz, 8-bit and 73 MHz, 24-bit packed pixel modes using an internal PLL
- 16-bit pixel port providing faster, high-color/true-color operation up to the 110 MHz sampling rate
- 8-bit pixel port providing standard SVGA and high-color/true-color modes up to the 110 MHz sampling rate

The 68 terminal FN package is designed to be interchangeable with the STG1703.

FN PACKAGE
(TOP VIEW)

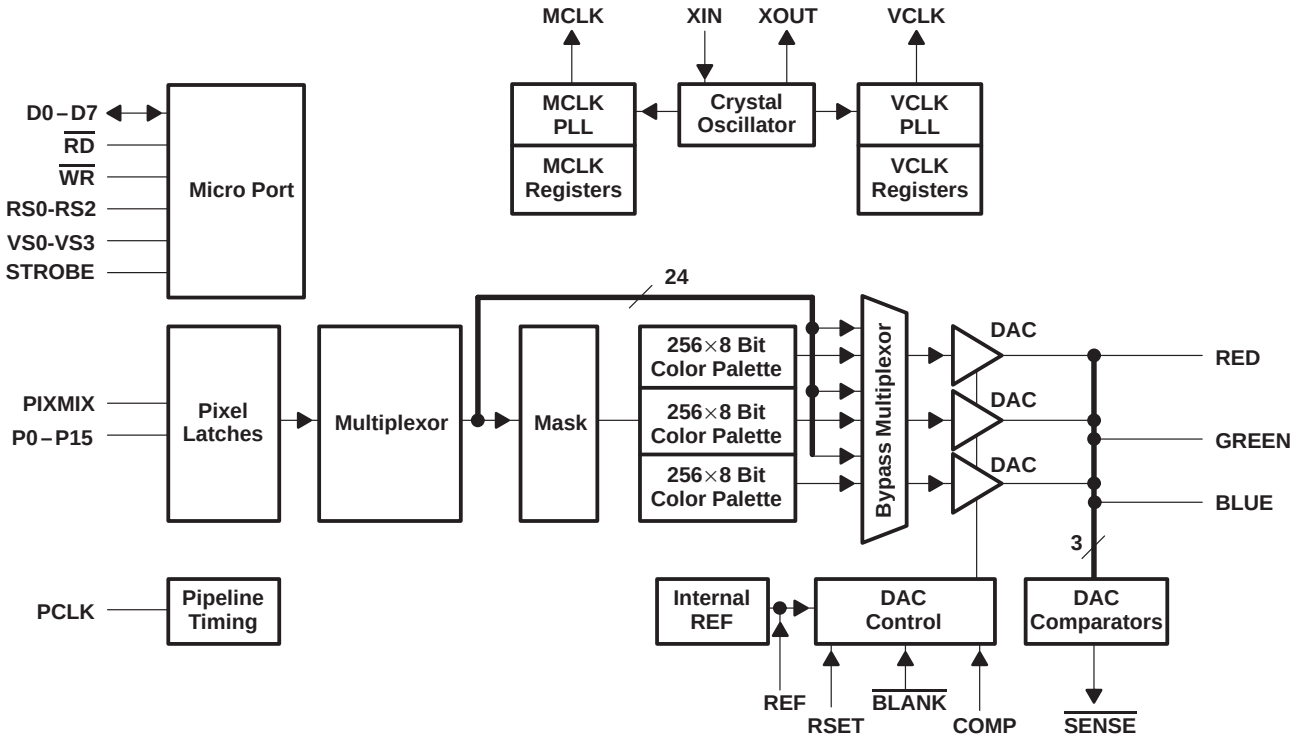


NC – No internal connection

applications

- Screen resolutions (noninterlaced)
  - 1600 × 1280, 8-bit/pixel, 60 Hz
  - 1280 × 1024, 16-bit/pixel, 60 Hz
  - 1024 × 768, 16-bit/pixel, 85 Hz
  - 1024 × 768, 24-bit/pixel, packed, 70 Hz
  - 800 × 600, 24-bit/pixel, unpacked, 72 Hz
- True-color desktop, PC add-in cards

functional block diagram



Terminal Functions

micro port

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{RD}$, $\overline{WR}$	5, 20	I	Read enable and write enable. $\overline{RD}$ or $\overline{WR}$ control the timing of read and write operations on the micro port. Most of the operations on the micro port can take place asynchronously to the pixel stream being processed by the color palette. Various minimum periods between operations are specified (in terms of pixel clocks) to allow this asynchronous behavior. $\overline{RD}$ and $\overline{WR}$ should not be low at the same time.
RS0–RS2	21, 22, 50	I	Register select. RS0–RS2 specify which internal register is to be accessed. The RS0–RS2 inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$). Information on register access and contents is given in the micro port section. The additional RS2 signal allows access to the extended features without the need for performing an indirect access sequence.
D0–D7	12–19	I/O	Input/output data. Data transfers between the 8-bit wide program data bus and the registers within the TVP3703 under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle, the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of $\overline{RD}$ signifies the end of a read cycle, after which the program data bus ceases to carry the contents of the register addressed and goes to a high impedance state.
VS0–VS3	44–47	I	Video clock PLL select.VS0–VS3 select the frequency (default or user programmed) of the video clock PLL. VS0–VS3 are ignored if the video clock frequency is selected by register control.
STROBE	43	I	Strobe input.The falling edge of STROBE latches VS0–VS3.

pixel port

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PCLK	63	I	Pixel clock. The rising edge of PCLK controls the sampling of data on P0–P15, $\overline{BLANK}$, and PIXMIX in all modes.
P0–P15	1, 4, 23, 25, 52–59, 64–67	I	Pixel data word. The selected pixel mode determines how this pixel data is interpreted.
PIXMIX	24	I	Pixel mode select. PIXMIX controls the switching between primary and secondary pixel modes when the extended pixel modes are selected (PIXMIX = 0 selects primary mode).
$\overline{BLANK}$	11	I	Blank in. A low value sampled on $\overline{BLANK}$, after the pipeline delay, turns the DAC outputs off.

DAC interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RED, GREEN, BLUE	38–40	O	DAC video outputs. These signals are designed to drive a doubly terminated 75-Ω load.
REF	51	I	External 1.235-V reference voltage. An external bypass capacitor should be connected from REF to GND.
RSET	48	I	A precision resistor placed between RSET and GND sets the full-scale DAC current. The required resistor value can be calculated from: $R_{set}\ (\Omega) = \frac{(2.1 \times V_{ref})}{I_O}$ where V_{ref} is the external or internal reference voltage and I_O is the required DAC full-scale output current. R_{set} is typically 147 Ω for VGA (see application information section).
COMP	49	I	External compensation capacitor connection for DACs.
$\overline{\text{SENSE}}$	68	O	Sense out. $\overline{\text{SENSE}}$ is a logical 0 if one or more of the DAC outputs exceeds the internal DAC comparator trip voltage (which is midway between the DAC full scale and GND potentials).

frequency synthesizer interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
XOUT	6	O	Crystal output and input connections. A series-resonant crystal must be connected between XOUT and XIN to provide the reference clock for the PLLs.
XIN	7	I	
VCLK	9	O	Video clock PLL out
MCLK	61	O	Memory clock PLL out

power supply

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
V_{DD}	8, 27, 35, 62		Digital power
AV_{DD}	3, 42		Analog power for the DACs and PLL.
GND	2, 10, 36, 37, 41, 60		Common ground rail for all circuitry.
NC	26, 28–34		No internal connection. For future upgrade to a 24-bit pixel port the controller. Outputs P16–P23 can be routed to terminals 26, 28–34 respectively.

detailed description

micro port

The TVP3703 micro port (see Table 1) is an extension of the standard VGA micro port and powers up with a register configuration compatible with standard and high-color VGA. There are two methods for accessing the register set of the TVP3703 – direct register space (RS) access and indirect access.

direct RS access

This feature supports direct RS mapping to eight address locations that access the VGA color palette, pixel command register, and an indexed register. The index low/high registers increment after every access to the indexed register.

direct RS access (continued)

Table 1. Direct RS Micro Port Accesses

RS(2–0)	VGA REGISTER
000	Address register (palette write)
001	Palette color value
010	Pixel mask/indirect access
011	Address register (palette read)
100	Index low byte
101	Indexed register
110	Pixel command register
111	Index high byte

indirect access

The indexed register space can also be accessed by a special mechanism of successive reads to the mask register location 2h, as shown in Table 2. Reads from RS location 2h cause a state counter to be advanced by one. Five successive reads of RS location 2h returns the mask register contents four times followed by the pixel command register value.

If the indexed register space is not enabled, the next access is directed to the pixel mask (state 1 in Table 2). States 3 to 4 require three reads from the pixel mask register and, when the pixel command register is written to enable the indexed register space, the next access is again directed to the mask register (the next state after state 5 is state 1).

The indirect access sequence can now enter states 6 and 7 to access the lower and higher byte of the index register respectively. Subsequent reads or writes to location 2h access the register space pointed to by the index register. After each indexed register access, the index register increments automatically. In this way, the entire indexed register space can be moved as a block without the need to keep writing to the index register.

At any point in the above sequence, a read or write to any location other than 2h resets the state counter to state 1.

On power up, the indirect access is truncated through the default setting of pixel command register bit 4 so that the TVP3703 is identified by existing video basic input/output system (BIOS) code as a fast ATT20C490 RAMDAC.

Table 2. Indirect Access Sequence

CURRENT STATE†		NEXT STATE			
STATE	REGISTER MAPPED AT RS = 2h	READ FROM RS = 2h AND INDEX SPACE ENABLED	READ FROM RS = 2h AND INDEX SPACE DISABLED (DEFAULT)	WRITE TO RS = 2h	READ/WRITE TO OTHER RS LOCATION
1	Pixel mask	2	2	1	1
2	Pixel mask	3	3	1	1
3	Pixel mask	4	4	1	1
4	Pixel mask	5	5	1	1
5	Pixel command	6	1	1	1
6	Index low byte	7		7	1
7	Index high byte	8		8	1
8	Indexed register	8‡		8‡	1

† Power-up state is state 1.
‡ Increment index register after access

indexed register space

The TVP3703 indexed register space including the indexes, register contents, and values is shown in Table 3.

Table 3. Indexed Register Space

INDEX	INDEX REGISTER CONTENTS†		VALUE‡
00 00h	Company ID = 97h		
00 01h	Device ID = 03h		
00 02h	Reserved (see Note 1)		
00 03h	Primary pixel mode select		
00 04h	Secondary pixel mode select		
00 05h	Pipeline timing control		
00 06h	Soft reset		
00 07h	Power management A		
00 08h	Power management B		
00 09h – 00 1Fh	Reserved (see Note 1)		
00 20h	VCLK V0 parameters low	(3Dh)	25.175
00 21h	VCLK V0 parameters high	(47h)	
00 22h	VCLK V1 parameters low	(55h)	28.332
00 23h	VCLK V1 parameters high	(49h)	
00 24h	VCLK V2 parameters low	(41h)	40.0
00 25h	VCLK V2 parameters high	(2Ah)	
00 26h	VCLK V3 parameters low	(26h)	72.0
00 27h	VCLK V3 parameters high	(06h)	
00 28h	VCLK V4 parameters low	(36h)	50.0
00 29h	VCLK V4 parameters high	(26h)	
00 2Ah	VCLK V5 parameters low	(29h)	77.0
00 2Bh	VCLK V5 parameters high	(06h)	
00 2Ch	VCLK V6 parameters low	(26h)	36.0
00 2Dh	VCLK V6 parameters high	(26h)	
00 2Eh	VCLK V7 parameters low	(43h)	44.90
00 2Fh	VCLK V7 parameters high	(29h)	
00 30h	VCLK V8 parameters low	(59h)	130.00
00 31h	VCLK V8 parameters high	(08h)	
00 32h	VCLK V9 parameters low	(41h)	120.00
00 33h	VCLK V9 parameters high	(06h)	
00 34h	VCLK V10 parameters low	(41h)	80.0
00 35h	VCLK V10 parameters high	(0Ah)	
00 36h	VCLK V11 parameters low	(56h)	31.50
00 37h	VCLK V11 parameters high	(48h)	
00 38h	VCLK V12 parameters low	(43h)	110.0
00 39h	VCLK V12 parameters high	(07h)	
00 3Ah	VCLK V13 parameters low	(59h)	65.0
00 3Bh	VCLK V13 parameters high	(28h)	
00 3Ch	VCLK V14 parameters low	(28h)	75.0
00 3Dh	VCLK V14 parameters high	(06h)	
00 3Eh	VCLK V15 parameters low	(40h)	94.50
00 3Fh	VCLK V15 parameters high	(08h)	
00 40h	MCLK M0 parameters low	(3Dh)	45.0
00 41h	MCLK M0 parameters high	(28h)	
00 42h	MCLK M1 parameters low	(51h)	66.0
00 43h	MCLK M1 parameters high	(27h)	
00 44h	MCLK M2 parameters low	(2Ah)	70.0
00 45h	MCLK M2 parameters high	(07h)	
00 46h	MCLK M3 parameters low	(36h)	80.0
00 47h	MCLK M3 parameters high	(08h)	
00 48h	Clock synthesizer control	(00h)	
00 49h – FF D5h	Reserved (see Note 1)		
FF D6h	CRC Test		
FF D7h	CRC low byte		
FF D8h	CRC high byte		
FF D9h	Red, green, blue (RGB) DAC input data test		
FF DAh – FF FFh	Reserved (see Note 1)		

† Register power-up values for given synthesizer frequencies are shown in parentheses.
‡ Synthesizer frequencies given for $f_{I(XIN)}$ = 14.31818 MHz
NOTE 1: Do not write to reserved locations

register content descriptions

A write to any register containing reserved bits should always write 0s to the reserved bits (the exception being bit 7 of power management register A). On reads, all reserved bits should be masked out.

The values of register bits that are reset on power-up are listed in the reset value columns below.

PIXEL COMMAND REGISTER (RS0 – RS2 = 110)			
BIT	**VALUE**	**FUNCTION**	**RESET VALUE**
7–5	000	8-bit color	000
	001	Reserved	
	010	Reserved	
	011	Reserved	
	100	Reserved	
	101	15-bit direct color	
	110	16-bit direct color	
	111	24-bit direct color	
4		1 = Enable extended register space	0
3		1 = Enable extended pixel modes	0
2		1 = Add 7.5 IRE† blanking pedestal	0
1		1 = Micro port interface to RAM is 8-bit not 6-bit	0
0		1 = Sleep mode (micro port and palette RAM still enabled, see power management features section)	0

† Institute of Radio Engineers

INDEX LOW AND HIGH BYTE REGISTERS (RS0 – RS2 = 100, RS0 – RS2 = 111)		
BIT	**FUNCTION**	**RESET VALUE**
7–0	Low/high byte of 16-bit index	0

COMPANY ID REGISTER (Index 0000h)			
BIT	**VALUE**	**FUNCTION**	**RESET VALUE**
7–0	97h	Texas Instruments	Read only

DEVICE ID REGISTER (Index 0001h)			
BIT	**VALUE**	**FUNCTION**	**RESET VALUE**
7–0	03h	TVP3703	Read only

PIXEL MODE SELECT REGISTERS (Primary and Secondary) (Indexes 0003h, 0004h)					
BIT	**VALUE**	**FUNCTION**	**MAX PCLK (MHz)**	**MAX VIDEO RATE (MHz)**	**RESET VALUE**
7–0	00h	8-bit indexed color	110	110	Not Reset
	01h	15-bit direct color or 8-bit indexed color	110	110	
	02h	15-bit direct color	110	110	
	03h	16-bit 5–6–5 direct color	110	110	
	04h	24-bit direct color	110	55	
	05h	Double 8-bit indexed color	67.5	135	
	06h	16-bit 5–6–5 direct color (2 × 8-bit input)	110	55	
	07h	8-bit indexed color (2 × 4-bit input)	110	55	
	08h	15-bit direct color (2 × 4-bit input)	110	55	
	09h	Double 24-bit direct color	85	56.5	
	0Ah–FFh	Reserved			

PIPELINE TIMING CONTROL REGISTER (Double 8-bit and 24-bit modes only) (Index 0005h)
The TVP3703 uses an internal PLL and timing control circuitry to automatically adjust pipeline. There are no register bits to program, since the device accounts for all desired frequency ranges.

SOFT RESET REGISTER (Index 0006h)		
BIT	**FUNCTION**	**RESET VALUE**
7–1	Reserved	0
0	1 = Reset all registers to power-on default state	0

register content descriptions (continued)

POWER MANAGEMENT REGISTER A (Index 0007h)			
BIT	**FUNCTION**	**RESET VALUE**	**SLEEP MODE†**
7	Reserved (write 1)	1	1
6	Reserved (write 0)	0	1
5	1 = Power-down palette RAM	0	0
4	Reserved (write 0)	0	1
3	Reserved	1	1
2–0	Reserved (write 0)	0	1

† Indicates the effect of selecting sleep mode (the power management register is not modified).

POWER MANAGEMENT REGISTER B (Index 0008h)		
BIT	**FUNCTION**	**RESET VALUE**
7–3	Reserved	Not reset
2	1 = Power-down crystal oscillator	0
1	1 = Power-down VCLK generator	0
0	1 = Power-down MCLK generator	0

PLL PARAMETERS LOW REGISTERS (Indexes 0020h, 0022h, . . . 0046h)		
BIT	**FUNCTION**	**RESET VALUE**
7	VCLK/MCLK source select 0 (see Table 4)	See Table 3
6–0	M value	

PLL PARAMETERS HIGH REGISTERS (Indexes 0021h, 0023h, . . . 0047h)		
BIT	**FUNCTION**	**RESET VALUE**
7	VCLK/MCLK source select 1 (see Table 4)	See Table 3
6–5	N2 value	
4–0	N1 value	

Table 4. VCLK/MCLK Source Select (PLL parameters high and low registers – bit 7)

SOURCE SELECT 1	SOURCE SELECT 0	VCLK/MCLK FUNCTION	PLL USED
0	0	$f_O = \frac{M + 2}{(N1 + 2) \times 2^{N2}} \times f_{I(XIN)}$	Yes‡
0	1	Reserved	
1	0	$f_O = \frac{f_{I(XIN)}}{2^{N2}}$	No
1	1	$f_O = f_{I(XIN)}$ direct	No

‡ See power management features section.

CLOCK SYNTHESIZER CONTROL REGISTER (Index 0048h)		
BIT	**FUNCTION**	**RESET VALUE**
7	Reserved	0
6	0 = Select VCLK by terminals VS0–VS3 1 = Select VCLK by bits 3–0	0
5–4	MCLK select (M0–M3)	0
3–0	VCLK select (V0–V15) if enabled by bit 6	0

CRC TEST REGISTER (Index FFD6h)			
BIT	**VALUE**	**FUNCTION**	**RESET VALUE**
7–6	0 0	Blue selection	Not reset
	0 1	Green selection	
	1 0	Red selection	
	1 1	None selected	
5–3	0 0 0 ⋮ 1 1 1	Bit 0 selected ⋮ Bit 7 selected	Not reset
2	1 → 0	Transition initializes start of CRC	1
1	0	Use pixel bus input	
	1	Use self-test-generated patterns	
0	0	Reserved	

CRC LOW BYTE (Bits 7–0) (Index FFD7h)		
BIT	**FUNCTION**	**RESET VALUE**
7–0	Low byte of CRC value	Not reset

CRC HIGH BYTE (Bits 15–8) (Index FFD8h)		
BIT	**FUNCTION**	**RESET VALUE**
7–0	High byte of CRC value	Not reset

programming the PLL clock generators

The conditions shown in the following equations must be followed when programming the PLL clock generators.

$$\left(\frac{f_{I(XIN)} \times 10^{-6}}{2} - 2\right) \le N1 \le \left(f_{I(XIN)} \times 10^{-6} - 2\right) \quad (1)$$

Where:

$0 \le N1 \le 31$ and N1 must be an integer

$$\left(\frac{64 \times 10^6}{f_{I(XIN)}}(N1 + 2) - 2\right) \le M \le \left(\frac{135 \times 10^6}{f_{I(XIN)}}(N1 + 2) - 2\right) \quad (2)$$

Where:

$0 \le M \le 127$ and M must be an integer

$$2^{N2} = \frac{f_{I(XIN)}(M + 2)}{f_O(N1 + 2)} \quad (3)$$

Where:

$0 \le N2 \le 3$ and N2 must be integer

power management features

Two power reduction options are available on the TVP3703.

1. Bit 0 of the pixel command register (sleep mode) provides a default power-down mode in which the following sections of the device are powered down:
   - All pixel multiplexor modes
   - All post-RAM logic
   - The triple DAC
   - The mask logic

   Micro port and palette-RAM power is maintained to allow read and write access to the internal registers or palette locations. A typical value of I_{DD} in sleep mode is listed in the electrical characteristics section.
2. The power management register, located in the indexed register space (index 0007h), allows selective power down of the device.

use of the hardware CRC feature

The TVP3703 hardware CRC feature supports testing of the entire pixel data path from the pixel port through to the DAC inputs at full video rates up to 170 MHz on the TVP3703. Each of the three colors (red, green and blue) are tested independently. CRCs are accumulated during active display, with accumulation being gated by the $\overline{\text{BLANK}}$ signal.

A TVP3703 CRC can be accumulated in either active screen or self-test-pattern generation mode and is controlled by bit 1 of the CRC test register (index FFD6h). To use the pattern generated CRC feature, perform the following test procedure:

1. Set the mode and verify the PIXMIX signal is low.
2. Set the proper values in the CRC test register for the desired CRC mode. Set $\overline{\text{BLANK}}$ low. Wait for ten PCLKS cycles.
3. Set bit 2 of the CRC test register to 1 and bit 1 to 0.

use of the hardware CRC feature (continued)

4. Set $\overline{\text{BLANK}}$ high.
5. Run for ten PCLK cycles.
6. Set $\overline{\text{BLANK}}$ low.
7. Run for 1200 dot clock cycles.
8. Set 0x5555 on pixel bus input.
9. Run for 20 PCLK cycles.
10. Set 0x0000 on the pixel bus input.
11. Run for three PCLK cycles.
12. Set bit 2 of the CRC test register to 0 and bit 1 to 1.
13. Wait for > 240 PCLK cycles.
14. Wait 1200 dot clock cycles.
15. Read the CRC low and high byte registers for the CRC result.

The CRC technique allows an authoritative check to be performed between the intended display and the actual display at full video rates. For a given image (which can be an application's image or a specially prepared test screen), theoretically derived CRC values are calculated for each RGB color, which are then compared with the TVP3703 hardware CRC values. Alternatively, the CRC value from a known good screen can be used as the reference.

The CRC facility on the TVP3703 can be used to validate correct operation of:

- The TVP3703 device in isolation
- The TVP3703 device designed into, and working in, a VGA board
- The DRAM, controller, and data path on the VGA board
- The disk and bus operation of the host PC
- MS-Windows™ (and device drivers) on the PC

The horizontal and vertical synchronization waveforms or timings do not affect hardware CRC accumulation. Any discrepancy between the calculated and TVP3703 hardware accumulated CRC values indicates a problem in the device or system being used.

The CRC logic on the TVP3703 is normally powered down. To perform a CRC test, bit 2 of the CRC test register (index FFD6h) should be reset to 0 and returned to 1 afterwards to return to the default condition.

The CRC mechanism does not check the DAC outputs (i.e., what is physically being displayed on the monitor); these can be tested using the TVP3703 $\overline{\text{SENSE}}$ output (generally readable as a register bit on the VGA controller).

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identification of the TVP3703

One of the two following sequences of micro port accesses identifies the existence of the TVP3703 in a graphics system:

OPERATION	RESULT
Read any valid register other than pixel mask (e.g., read I/O location 03C7h)	Resets the indirect access sequence
Read pixel mask (I/O location 03C6h) four times	Provides indirect access procedure
Write pixel mask with 10h	Provides indirect access to pixel command register, enabling indexed registers. This also resets the indirect procedure.
Read pixel mask five times	Provides indirect access procedure
Write pixel mask twice with 00h	Provides indirect access procedure setting the index registers to 0
Read pixel mask	Returns company ID (97h)
Read pixel mask	Returns device ID (03h)

or:

OPERATION	RESULT
Write zero to RS(2–0) = 4h	Sets the index low byte to zero
Write zero to RS(2–0) = 7h	Sets the index high byte to zero
Read RS(2–0) = 5h	Returns company ID (97h)
Read RS(2–0) = 5h	Returns device ID (03h)

pixel port

The rising edge of PCLK latches all of the pixels. Modes requiring more than one word per pixel accumulate the least significant bytes of the pixel first. $\overline{\text{BLANK}}$ going high always identifies the first word within a pixel. The VGA, SVGA, and extended pixel modes are listed in Tables 5 and 6.

Table 5. VGA and SVGA Modes

SVGA MODE†	PIXEL WORD LATCHED	USE OF PIXEL INPUT TERMINALS‡															
		P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
8-bit indexed	single P(7–0)	X	X	X	X	X	X	X	X	P7	P6	P5	P4	P3	P2	P1	P0
15-bit direct (5–5–5)	first P(7–0)	X	X	X	X	X	X	X	X	G5	G4	G3	B7	B6	B5	B4	B3
	second P(7–0)	X	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	G7	G6
16-bit direct (5–6–5)	first P(7–0)	X	X	X	X	X	X	X	X	G4	G3	G2	B7	B6	B5	B4	B3
	second P(7–0)	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	G7	G6	G5
24-bit direct (8–8–8)	first P(7–0)	X	X	X	X	X	X	X	X	B7	B6	B5	B4	B3	B2	B1	B0
	second P(7–0)	X	X	X	X	X	X	X	X	G7	G6	G5	G4	G3	G2	G1	G0
	third P(7–0)	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	R2	R1	R0

† Pipe delay for all modes = 3 PCLK + 7 dot clocks
‡ Unspecified bits = 0

pixel port (continued)

Table 6. Extended Pixel Modes

SVGA MODE†		PIXEL WORD LATCHED	USE OF PIXEL INPUT TERMINALS															
			P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
00h	8-bit indexed	single P(7–0)	X	X	X	X	X	X	X	X	P7	P6	P5	P4	P3	P2	P1	P0
01h	15-bit mixed	single P(15–0)	0 or 1	X R7	X R6	X R5	X R4	X R3	X G7	X G6	P7 G5	P6 G4	P5 G3	P4 B7	P3 B6	P2 B5	P1 B4	P0 B3
02h	15-bit direct	single P(15–0)	X	R7	R6	R5	F4	F3	G7	G6	G5	G4	G3	B7	B6	B5	B4	B3
03h	16-bit direct	single P(15–0)	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3
04h	24-bit direct	first P(15–0)	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		second P(15–0)	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	R2	R1	R0
05h	Double 8-bit indexed‡,§	single P(15–0)	P7	P6	P5	P4	P3	P2	P1	P0	P7	6	P5	P4	P3	P2	P1	P0
			second displayed pixel								first displayed pixel							
06h	16-bit direct (5–6–5)	first P(7–0)	X	X	X	X	X	X	X	X	G4	G3	G2	B7	B6	B5	B4	B3
		second P(7–0)	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	G7	G6	G5
07h	8-bit indexed	first P(3–0)	X	X	X	X	X	X	X	X	X	X	X	X	P3	P2	P1	P0
		second P(3–0)	X	X	X	X	X	X	X	X	X	X	X	X	P7	P6	P5	P4
08h	15-bit direct (5–5–5)	first P(7–0)	X	X	X	X	X	X	X	X	G5	G4	G3	B7	B6	B5	B4	B3
		second P(7–0)	X	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	G7	G6
09h	Double 24-bit direct§	first P(15–0)	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
														first displayed pixel				
		second P(15–0)	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
			second displayed pixel															
		third P(15–0)	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0

† Pipe delay for mode = 3 PCLK + 7 dot clocks
‡ Unspecified bits = 0
§ Modes 5 (05h) and 9 (09h) use PLL, DAC CLK = 2 × PCLK or 2/3 PCLK respectively.

primary and secondary pixel mode combinations

Writing to the pixel command register enables the extended pixel modes. A primary pixel mode and a secondary pixel mode are defined for the TVP3703. The TVP3703 switches between these two modes on the fly under control of the PIXMIX terminal.

The PIXMIX terminal and the pixel terminals are sampled on PCLK. If the primary or secondary pixel mode format requires two PCLK edges to build a whole pixel, then PIXMIX should only change state on every second PCLK edge after $\overline{\text{BLANK}}$ has gone high at the start of a line.

When PIXMIX is not in use, the primary and secondary pixel mode select registers should be written with the same value.

The primary and secondary pixel mode combinations are listed in Table 7.

primary and secondary pixel mode combinations (continued)

Table 7. Primary and Secondary Pixel Mode Combinations

PRIMARY MODE	SECONDARY MODE									
	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h
00h	X	X	X	X						
01h	X	X	X	X						
02h	X	X	X	X						
03h	X	X	X	X						
04h					X		X	X	X	
05h						X				
06h					X		X	X	X	
07h					X		X	X	X	
08h					X		X	X	X	
09h										X

NOTE 2: Pixel switching can only be performed when the PCLK to dot clock ratios for the primary and secondary modes are the same.

programming of pixel modes using the PLL

The TVP3703 uses an internal PLL to generate the internal dot clock. This PLL automatically adjusts the PCLK to dot clock ratio based on the multiplexing mode selected. Therefore no further programming is necessary.

pixel resolution and blanking periods in mode 09h

In mode 09h (packed 24-bit), latching 16 bits of data from 3 PCLK cycles generates a group of 2 pixels. This means that the horizontal screen resolution must be an even number of pixels, and the number of PCLK cycles during active display must be a multiple of 3.

Due to the internal phase relationships between PCLK and the pixel clock generated by the internal PLL, the horizontal and vertical blanking period must also be an integral multiple of 3 PCLK cycles. This must be satisfied so that the first pixel of each line always appears at the same point horizontally on the screen, from line to line and from frame to frame.

Therefore mode 09h requires the following relationships must be satisfied:

Horizontally:

The total horizontal duration must be an integral multiple of 3 PCLKs.

i.e., $\frac{\text{HTOT}}{3}$ = integer, where HTOT = total horizontal duration in standard VGA registers.

Vertically:

The total vertical duration must be an integral multiple of 3 PCLKs.

i.e., $\frac{\text{VTOT} \times \text{HTOT}}{3}$ = integer, where VTOT = total vertical duration in standard VGA registers.

In all standard VGA systems, if the horizontal requirement is met, the vertical requirement is also met.

VGA standard controllers normally satisfy the requirements described in this section because the horizontal blanking period is specified in character widths (8 pixels wide), vertical blanking in terms of scan lines, and resolution in even pixels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 3) . . . . . 7 V
Input voltage range, V_I . . . . . –0.5 V to V_{DD}+0.5 V
Analog output short-circuit duration to any power supply or common . . . . . unlimited
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Junction temperature, T_J . . . . . 175°C
Case temperature for 10 seconds: . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltages, AV_{DD}, DV_{DD}	4.75	5	5.25	V
Reference voltage, V_{ref}	1.15	1.235	1.26	V
High-level input voltage, V_{IH}	2.4		V_{DD}+0.5	V
Low-level input voltage, V_{IL}			0.8	V
Output load resistance, R_L		37.5		Ω
FS ADJUST resistor, R_{SET}		147		Ω
Operating free-air temperature, T_A	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current, average power (see Note 4)			270	340	mA
	Supply current, average power (sleep mode) (see Note 5)			60	150	mA
	Supply current, average power (palette RAM powered down) (see Note 4)			220	250	mA
I_I	Digital input current			±100		µA
I_O	Off-state-digital output current				±50	µA
V_{OH}	High-level output voltage	I_L = –1 mA	2.4			V
V_{OL}	Low-level output voltage	I_L = 4 mA			0.4	V

NOTES: 4. Typical and maximum figures are both measured at 135 MHz, with differences due to V_{DD}, pixel mode, and part to part variations.
5. Typical figure measured at 35 MHz, with differences due to V_{DD}, pixel mode, and part to part variations.

timing requirements

micro port

PARAMETER		TVP3703-170		TVP3703-135		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(WLWH)}$	Pulse duration, $\overline{WR}$ low	50		75		ns
$t_{w(RLRH)}$	Pulse duration, $\overline{RD}$ low	50		50		ns
$t_{rec(WHWL)}$	Recovery time preceding a write (see Notes 6 and 7)	$3\times t_{c(CHCH)}$		$3\times t_{c(CHCH)}$		ns
$t_{rec(RHRL)}$	Recovery time preceding a read (see Notes 6 and 7)	$6\times t_{c(CHCH)}$		$6\times t_{c(CHCH)}$		ns
$t_{su(SVL)}$	Setup time, RS0-RS2	10		10		ns
$t_{h(LSX)}$	Hold time, RS0-RS2	4		4		ns
$t_{su(DVWH)}$	Setup time, write data	10		10		ns
$t_{h(WHDX)}$	Hold time, write data	10		10		ns

NOTES: 6. $t_{c(CHCH)}$ (PCLK period) is specified in the pixel port timing requirements table.
7. Access recovery times are specified as the time before a particular access because the worst case access (reading a red palette color value) can occur after either reading a blue palette color value or after writing to the address register (read mode).

PLL frequency select

PARAMETER		TVP3703-170		TVP3703-135		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(SHSL)}$	Pulse duration, STROBE high	50		50		ns
$t_{w(SLSH)}$	Pulse duration, STROBE low	50		50		ns
$t_{su(SVSL)}$	Setup time, VS0–VS3 (see Note 8)	20		30		ns
$t_{h(SLSX)}$	Hold time, VS0–VS3 (see Note 8)	20		30		ns

NOTE 8: The VS0–VS3 latches are transparent when STROBE is at logic 1.

pixel port

PARAMETER		TVP3703-170		TVP3703-135		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(CHCH)}$	PCLK cycle time (pixel mode 05h – double 8-bit, indexed)	11.7		14.8		ns
	PCLK cycle time (pixel mode 09h – double 24-bit, direct)	9.08		9.08		ns
	PCLK cycle time (all other pixel modes)	9.08		9.08		ns
$t_{w(CLCH)}$	Pulse duration, PCLK low	2.9		4		ns
$t_{w(CHCL)}$	Pulse duration, PCLK high	2.9		3		ns
$t_{su(PVCH)}$	Setup time, pixel data (see Note 9)	2		2		ns
$t_{h(CHPX)}$	Hold time, pixel data (see Note 9)	2		2		ns

NOTE 9: The pixel address input to the color palette should be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must also be met during the blanking period).

switching characteristics

micro port

PARAMETER		TVP3703-170		TVP3703-135		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(RLQX)}$	Delay time, output turn on	5		5		ns
$t_{a(RLQV)}$	Access time, read enable		40		40	ns
$t_{h(RHQX)}$	Hold time, output	5		5		ns
$t_{d(RHQZ)}$	Delay time, output turn off		20		20	ns

pixel port

PARAMETER		TVP3703-170			TVP3703-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	Analog output skew		1			1		ns

frequency synthesis

PARAMETER		TVP3703-170			TVP3703-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$f_{I(XIN)}$	XIN crystal frequency range		14.3			14.3		MHz
	Internal VCO frequency	64		170	64		135	MHz
f_O	VCLK output frequency (C_L = 15 pF)			110			110	MHz
	MCLK output frequency (C_L = 15 pF)			80			80	MHz
	Synthesizer lock time			5			5	ms

operating characteristics

DAC

PARAMETER		TVP3703-170			TVP3703-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution		8			8		bits
	DAC operating frequency			170			135	MHz
	Output current, black level pedestal (see Note 10)	0.95	1.44	1.9	0.95	1.44	1.9	mA
	Output current, white relative to black (see Note 10)	16.74	17.62	18.50	17.6	17.62	20.4	mA
	DAC-to-DAC matching (see Notes 10 and 11)		±2%	±5%		±2%	±5%	
E_L	Integral linearity error (see Note 10)			±1			±1	LSB
E_D	Differential linearity error (see Note 10)			±1			±1	LSB
	DAC output compliance (see Note 10)	−1		1.2	−1		1.2	V
	DAC output impedance		50			50		kΩ
t_r	Rise time (black to white level) (see Notes 10, 12, and 13)		3			1	3	ns
t_s	Settling time (black to white) (see Notes 10, 12, and 14)		5			10		ns
	Glitch energy (see Notes 10 and 12)		50			50		pVs
	Comparator trip voltage		340			340		mV
I_{ref}	Reference input current		100			100		µA
	Internal reference voltage		1.235			1.235		V
	Internal reference voltage accuracy	1.15	1.235	1.27	1.15	1.235	1.27	V

NOTES: 10. V_{ref} = 1.235 V and R_{SET} = 147 Ω
11. About the midpoint of the distribution of the three DACs
12. 37.5 Ω and 30 pF load
13. Measured between 10% and 90% of full scale transition.
14. Settling to within 2% of frame sync delay (fsd)

timing diagrams

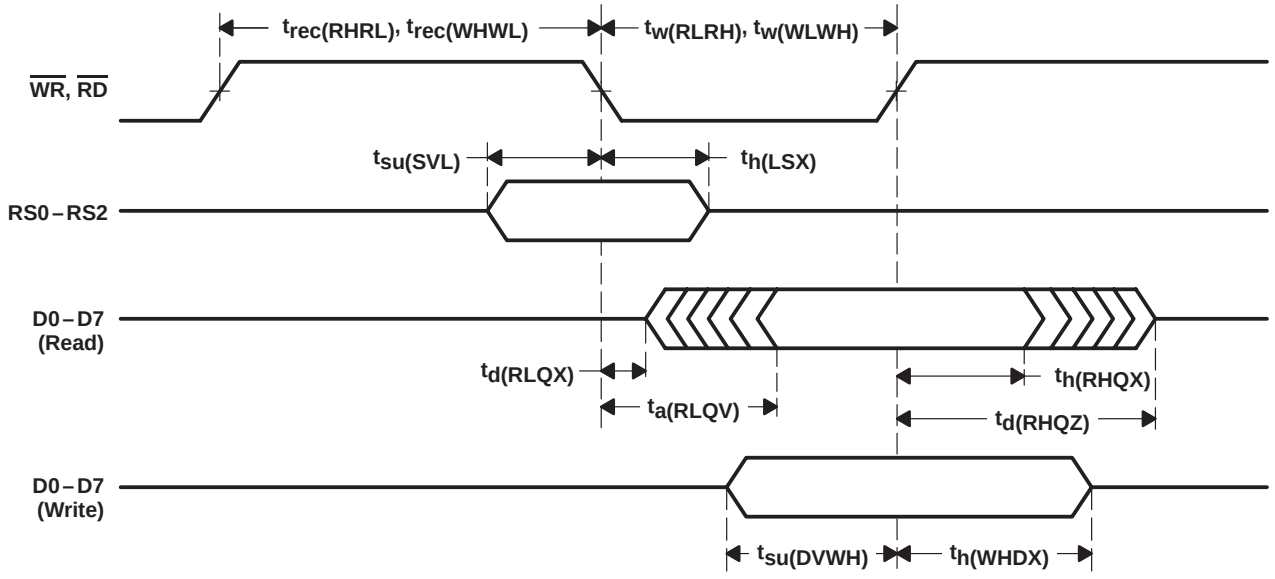


Figure 1. Micro Port Read/Write Cycle Timing

timing diagrams (continued)

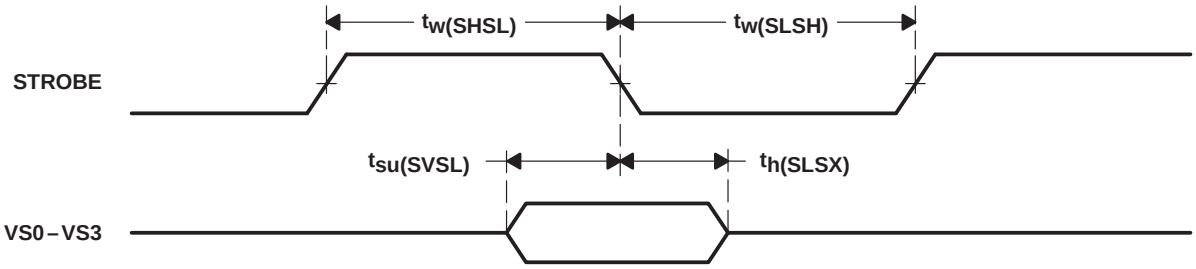


Figure 2. PLL Frequency Select Write Cycle Timing

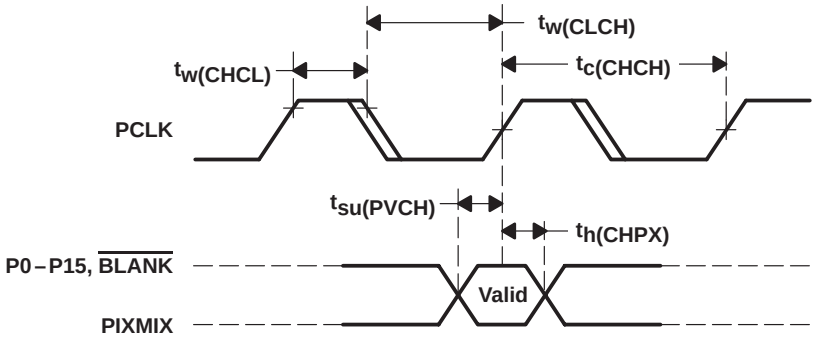


Figure 3. Pixel Port Timing

APPLICATION INFORMATION

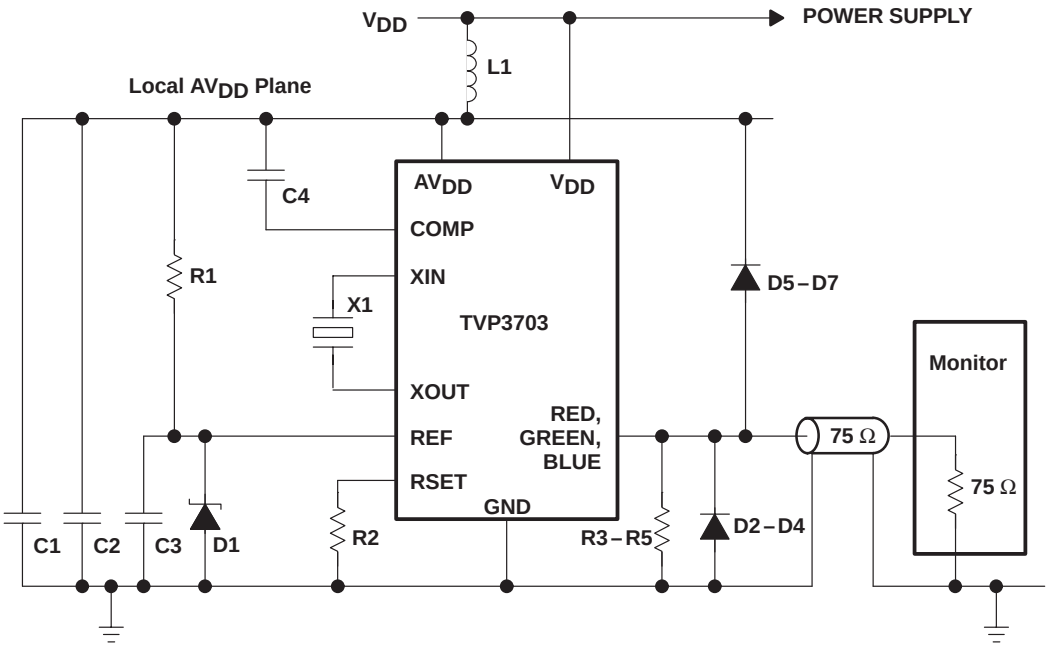


Figure 4. Analog Interface – Recommended Circuit in Internal Voltage Reference Mode

Table of Parts for Recommended Circuit (see Figure 4)

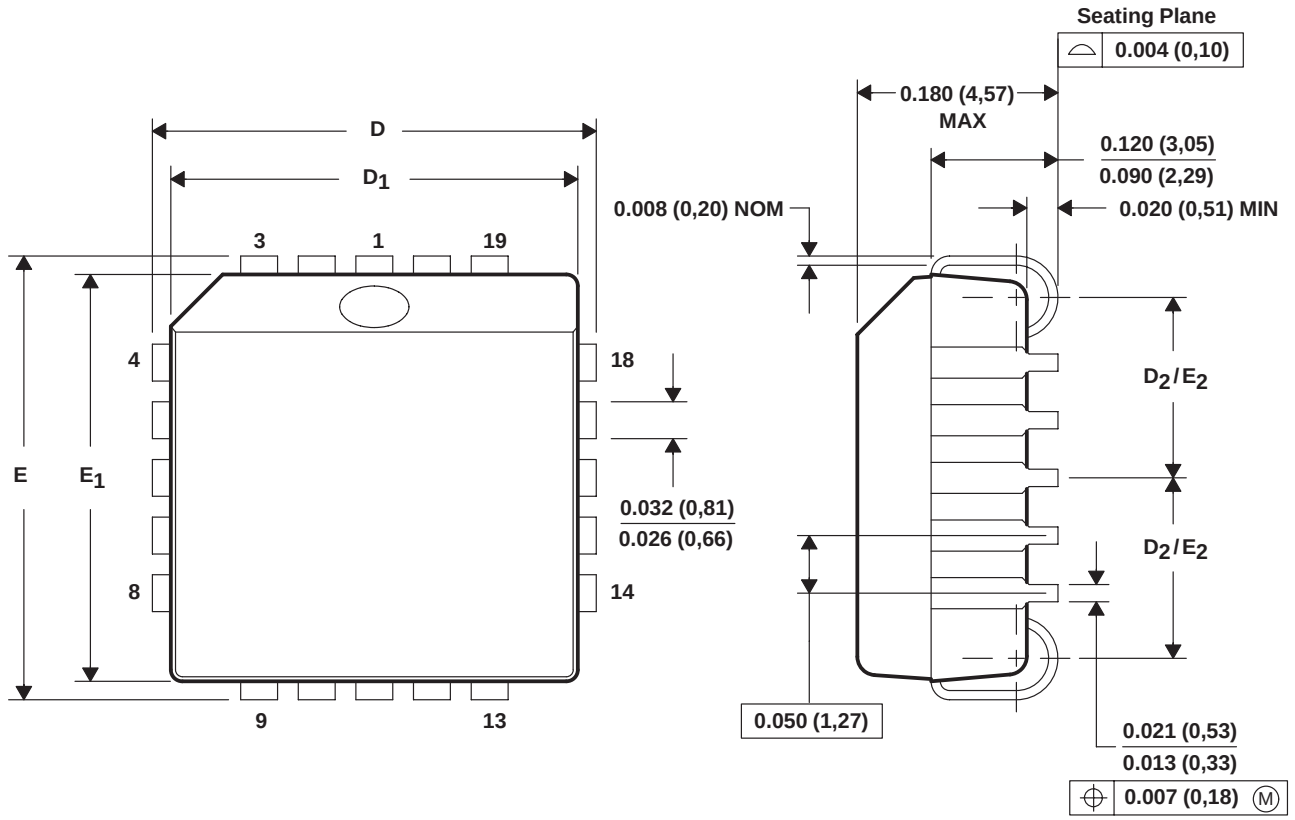
PART NUMBER	VALUE	DESCRIPTION
C1	47 µF	Capacitor
C2† – C3‡	100 nF	Surface-mount capacitor
C4†	100 nF	Surface-mount capacitor
R1§	1 kΩ	5% resistor
R2†	147 Ω	1% resistor
R3 – R5†	75 Ω	1% resistor
D1§	LM385BZ-1.2	Voltage reference
D2 – D7	1N4148	Diode
L1	1 µH	Inductor
X1	14.31818 MHz	Crystal

† Place these components as close to the palette DAC as possible.
‡ Placing this component between REF and AV_{DD} does not affect performance.
§ Omit these components when using the TVP3703 in internal voltage reference mode.

MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS**	D/E		D_1/E_1		D_2/E_2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B–10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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