

TLP554

ISOLATED LINE RECEIVER
SIMPLEX/MULTIPLEX DATA TRANSMISSION
COMPUTER-PERIPHERAL INTERFACE
MICROPROCESSOR SYSTEM INTERFACES
DIGITAL ISOLATION FOR A/D,D/A CONVERSION

The TOSHIBA TLP554 a photocoupler which combines a GaAlAs IRED as the emitter and an integrated high gain, high speed photodetector.

The output of the detector circuit is an open collector, Schottky Clamped transistor.

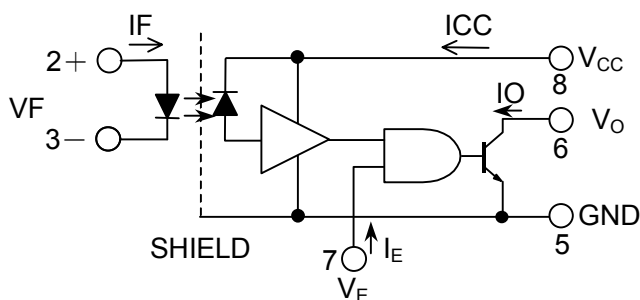
A Faraday shield integrated on the photodetector chip reduces the effects of capacitive coupling between the input LED emitter and the high gain stages of the detector. This provides an effective common mode transient immunity of 1000V/us.

- Input Current Threshold : $I_F = 5\text{mA (Max.)}$
- Switching Speed : 10MBd (TYP, @NRZ)
- Common mode transient immunity : $\pm 1000\text{V/us (Min)}$
- Guaranteed Performance Over Temperature : $0 \sim 70^\circ\text{C}$
- Isolation Voltage : 2500Vrms (Min)
- UL Recognized : UL1577, File No. E67349

TRUTH TABLE (Positive Logic)

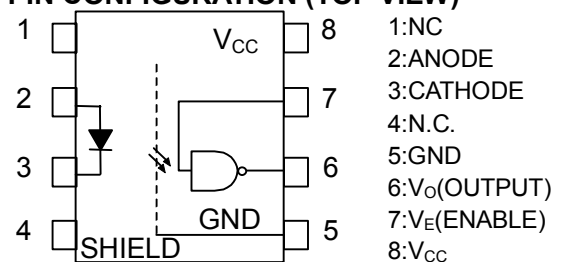
INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

SCHEMATIC

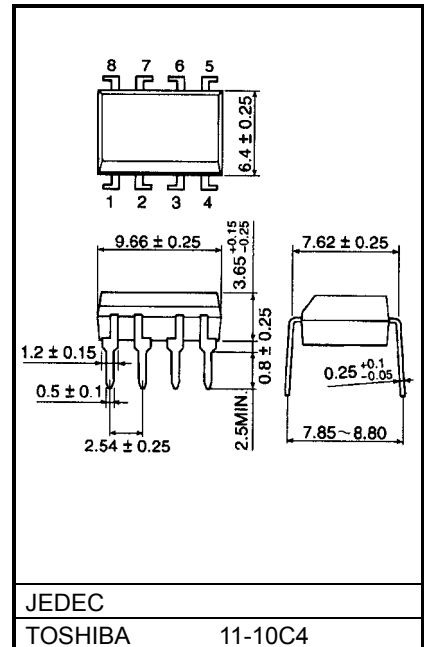


A 0.1μF bypass capacitor must be connected Between pins 8 and 5. (See Note 1)

PIN CONFIGURATION (TOP VIEW)



Unit: mm



Weight: 0.54 g

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Low Level input Voltage	VFL	-3	0	1.0	V
High Level input current	IFH	6.3*	—	20	mA
Supply Voltage	VCC	4.5	5	5.5	V
High-Level Enable Voltage	VEH	2.0	—	VCC	V
Low-Level Enable Voltage	VEL	0	—	0.8	V
Fan Out(TTL Load)	N	—	—	8	—
Operating Temperature	Topr	0	—	70	°C

*6.3mA condition permits at least 20% CTR degradation

Initial switching threshold is 5.0mA or less.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	I _F	20	mA
	Reverse Voltage	V _R	5	V
DETECTOR	Output Current	I _O	25	mA
	Output Voltage	V _O	-0.5~7	V
	Supply Voltage (Note 2)	VCC	7	V
	Enable Voltage (Note 3)	VE	5.5	V
	Output Power Dissipation	P _O	40	mW
Storage Temperature Range		T _{stg}	-55~125	°C
Operating Temperature Range		T _{opr}	-40~85	°C
Lead Soldering Temperature (10 s) (Note 4)		T _{sol}	260	°C
Isolation Voltage (AC, 1 minute, R.H.≤ 60%) (Note 5)		BV _S	2500	Vrms

(Note 1) The V_{CC} supply voltage to each TLP554 isolator must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins each device.

(Note 2) 1 Minute Maximum.

(Note 3) Not to exceed VCC by more than 500mV.

(Note 4) 2mm below seating plane.

(Note 5) Device considered a two-terminal device : Pins 1,2,3 and 4 shorted together, and Pins 5, 6,7 and 8 shorted together.

ELECTRICAL CHARACTERISTICS (Ta = 0~70°C , VCC=4.5~5.5V , VFL≤1.0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN.	TYP.*	MAX.	UNIT
Forward Voltage		V _F	I _F = 10 mA , Ta=25°C			1.65	1.80	V
Temperature Coefficient of Forward Voltage		ΔV _F /ΔTa	I _F = 10 mA ,		—	-2.0	—	mV/°C
Input Reverse Current		I _R	V _R =5V, Ta=25°C		—	—	10	μA
Input Capacitance		C _T	V = 0 , f = 1MHz , Ta=25°C		—	45	—	pF
High-Level Output Current		IOH	V _F = 1.0V V _O = 5.5V V _E = 2.0V	Ta=0~70°C	—	10	250	μA
				Ta=25°C	—	0.5	10	
Low-Level Output Voltage		VOL	I _F =5mA , V _E =2.0V , IOL=13mA		—	0.4	0.6	V
High Level input current		IFH	IOL=13mA , V _E =2.0V , VOL=0.6V		—	—	5	mA
Supply Current	High Level	ICCH	VCC=5.5V V _E =0.5V	I _F =0mA	—	7	15	mA
	Low Level	ICCL		I _F =10mA	—	12	19	
Enable Current	High Level	IEH	VCC=5.5V	V _E =2.0V	—	-1.0	—	mA
	Low Level	IEL		V _E =0.5V	—	-1.6	-2.0	
Enable Voltage	High Level	VEH	— (Note 6)		2.0	—	—	V
	Low Level	VEL	—		—	—	0.8	
Capacitance (Input-Output)		CS	V _S =0 , f=1MHz , Ta=25°C		—	0.6	—	pF
Resistance (Input-Output)		RS	V _S =500V , Ta=25°C , R.H. ≤60%		5 × 10 ¹⁰	10 ¹⁴	—	Ω

(*)All typ.values are at Ta=25°C

(Note 6) No pull up resistor required as the device has an internal pull up resistor.

SWITCHING CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{cc}=5\text{V}$)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Propagation Delay Time	L→H	tpLH	1	RL=350Ω	IF=7.5→0mA	—	60	120	ns
	H→L	tpHL		CL=15pF	IF=0→7.5mA	—	60	120	
Output Rise Time(10-90%)		tr		IF=7.5→0 / 0→7.5mA		—	30	—	ns
Output Fall Time(10-90%)		tf		RL=350Ω, CL=15pF		—	30	—	
Enable Propagation Delay Time		tELH	2	RL=350Ω	VE=0.5→3.0V	—	25	—	ns
		tEHL		CL=15pF	VE=3.0→0.5V	—	25	—	
Common Mode Transient Immunity at Hight Level Outout		CM _H	3	VCM=400V	IF=0mA VO(Min)=2.0V	1000	10000	—	V/μs
Common Mode Transient Immunity at Low Level Outout		CM _L		RL=350Ω (Note 7)	IF=7.5mA VO(Max)=0.8V	-1000	-10000	—	

(Note 7) CM_H: The maximum tolerable rate of rise of the common mode voltage to ensure

the output will remain in the high state(i.e., VOUT>2.0V)

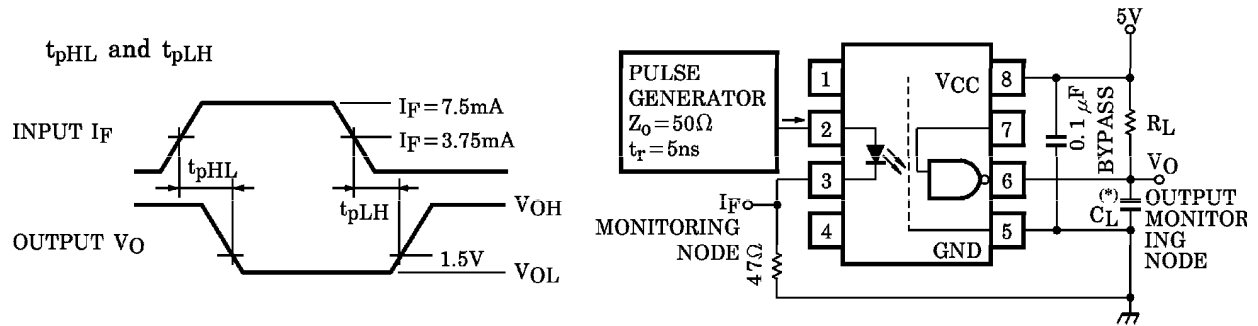
CM_L: The maximum tolerable rate of fall of the common mode voltage to ensure

the output will remain in the low output state(i.e., VOUT<0.8V)

Measured in volts per microsecond(V/μs).

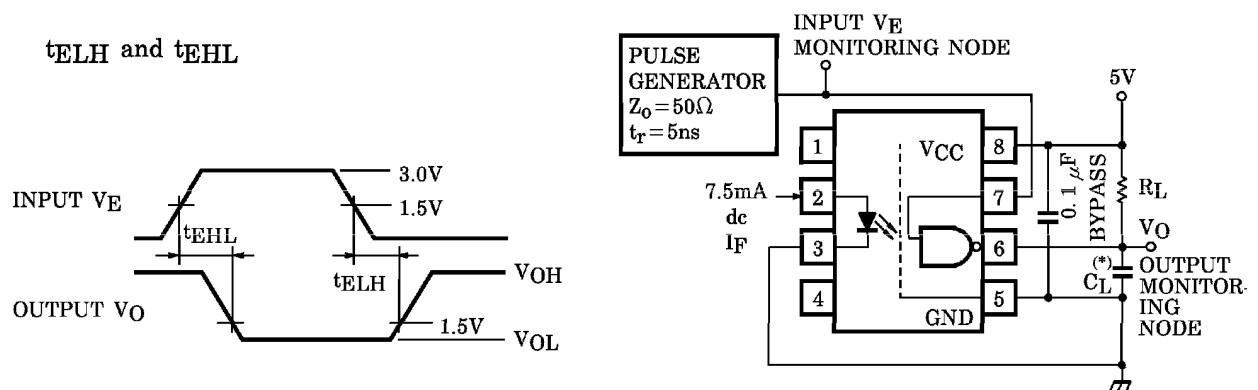
(Note 8) Maximum electrostatic discharge voltage for any pins:180V(C=200pF,R=0)

TEST CIRCUIT 1.



(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

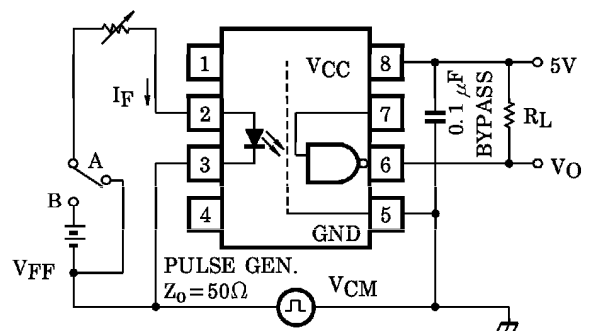
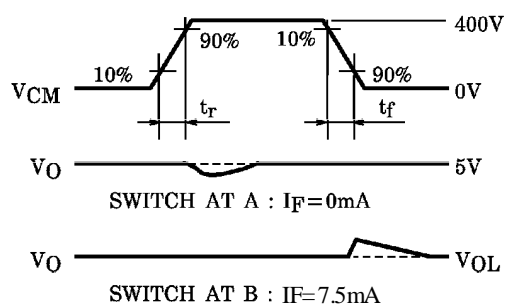
TEST CIRCUIT 2.

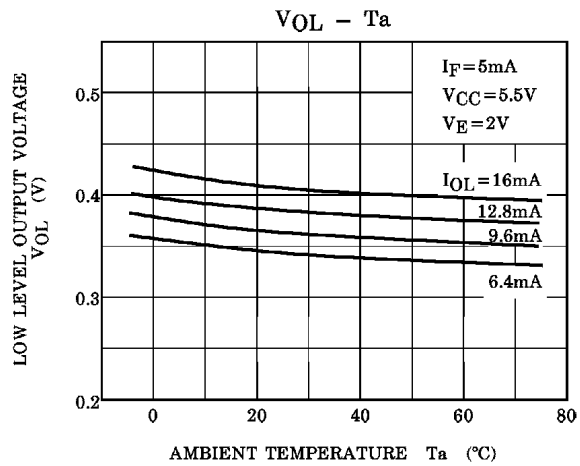
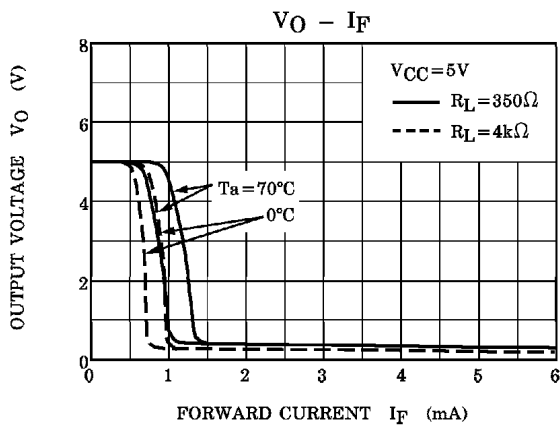
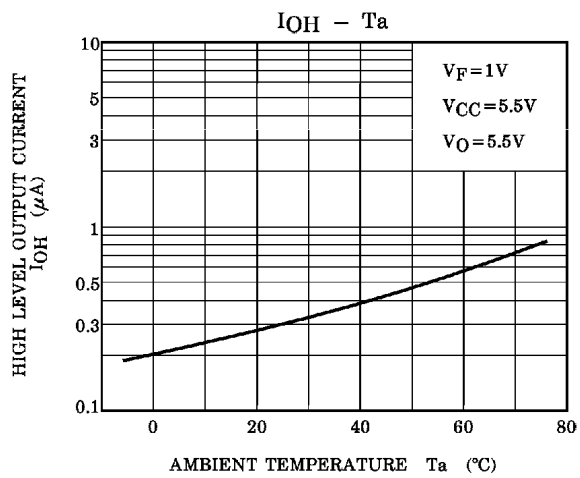
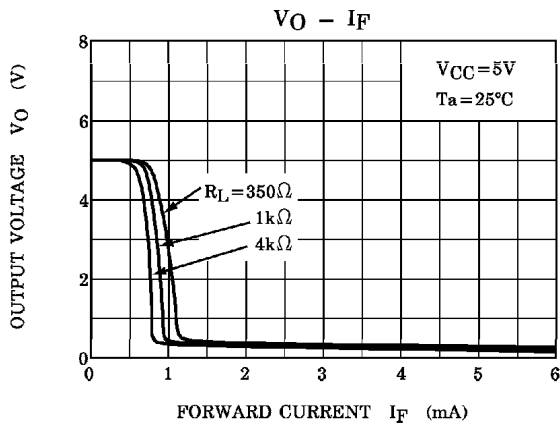
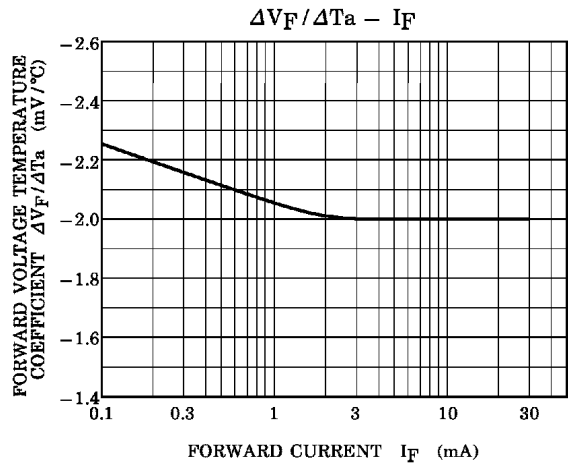
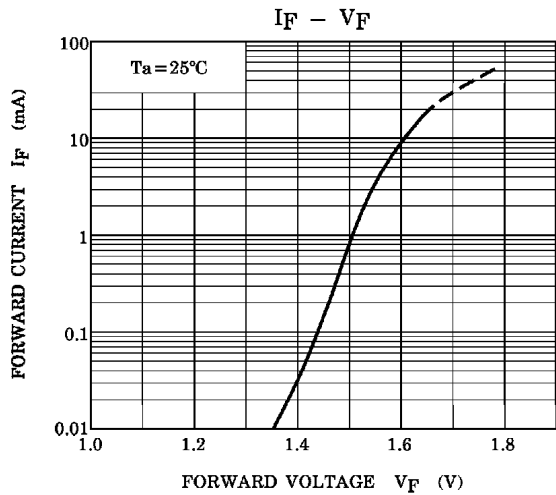


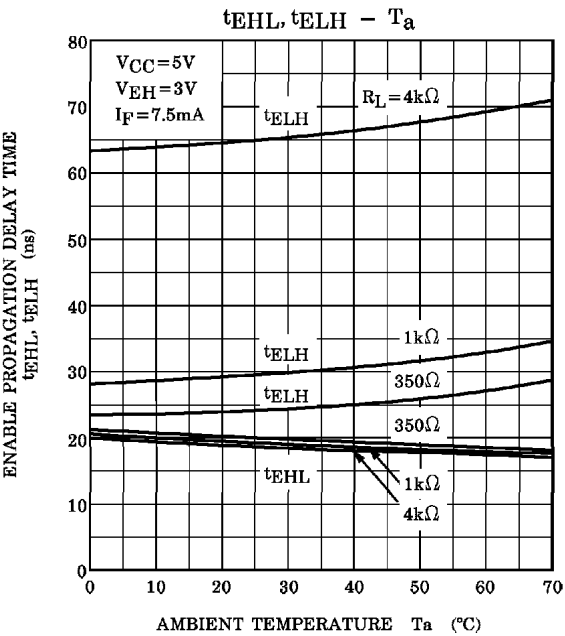
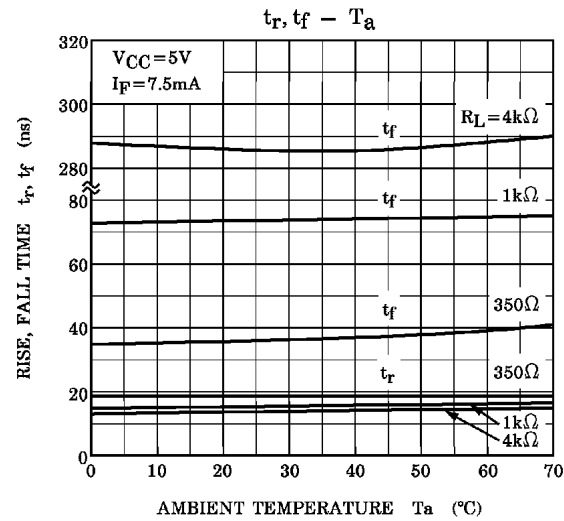
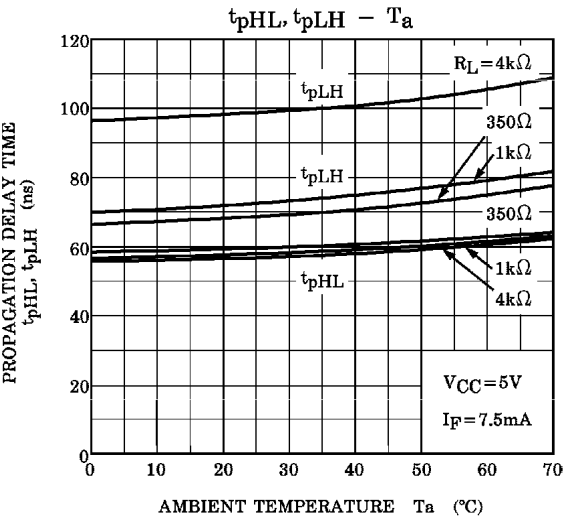
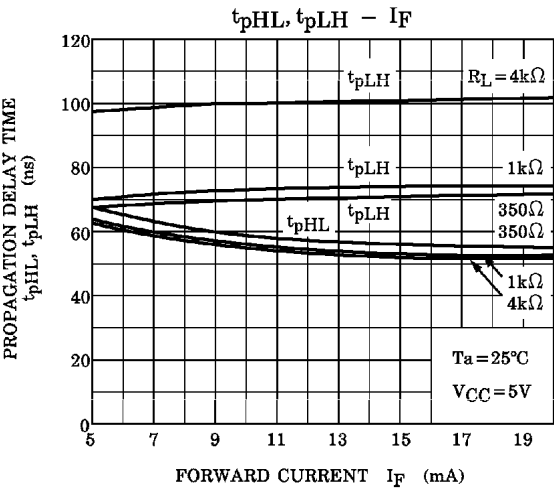
(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 3.

Transient Immunity and Typ. Waveforms.







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