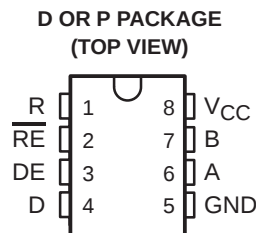


- Bidirectional Transceiver
- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Skew . . . 6 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirements . . . 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Driver Output Capacity . . .  $\pm 60$  mA
- Thermal-Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedances . . . 12 k $\Omega$  Min
- Receiver Input Sensitivity . . .  $\pm 200$  mV Max
- Receiver Input Hysteresis . . . 120 mV Typ
- Fail Safe . . . High Receiver Output With Inputs Open
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection
- Interchangeable With National DS3695 and DS3695A



## description

The TL3695 differential bus transceiver is designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

The TL3695 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a directional control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . This port features wide positive and negative common-mode voltage ranges, making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# TL3695 DIFFERENTIAL BUS TRANSCEIVER

SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

### AVAILABLE OPTIONS

| T <sub>A</sub> | PACKAGED DEVICES  |                 |
|----------------|-------------------|-----------------|
|                | SMALL OUTLINE (D) | PLASTIC DIP (P) |
| 0°C to 70°C    | TL3695D           | TL3695P         |

The D package is available taped and reeled. Add the suffix R to device type (e.g., TL3695DR).

### Function Tables

#### DRIVER

| INPUT<br>D | ENABLE<br>DE | OUTPUTS |   |
|------------|--------------|---------|---|
|            |              | A       | B |
| H          | H            | H       | L |
| L          | H            | L       | H |
| X          | L            | Z       | Z |

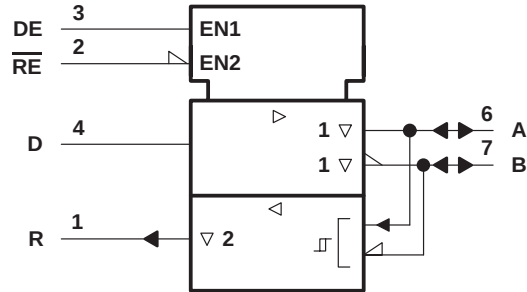
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

#### RECEIVER

| DIFFERENTIAL INPUTS<br>A – B            | ENABLE<br>RE | OUTPUT<br>R |
|-----------------------------------------|--------------|-------------|
| $V_{ID} \geq 0.2\text{ V}$              | L            | H           |
| $-0.2\text{ V} < V_{ID} < 0.2\text{ V}$ | L            | ?           |
| $V_{ID} \leq -0.2\text{ V}$             | L            | L           |
| X                                       | H            | Z           |
| Inputs open                             | L            | H           |

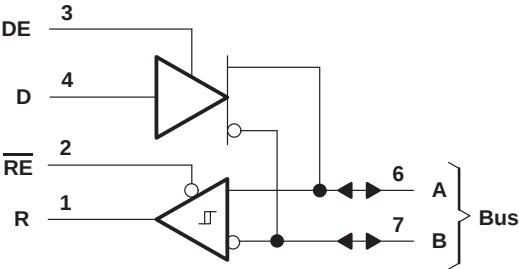
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

### logic symbol†

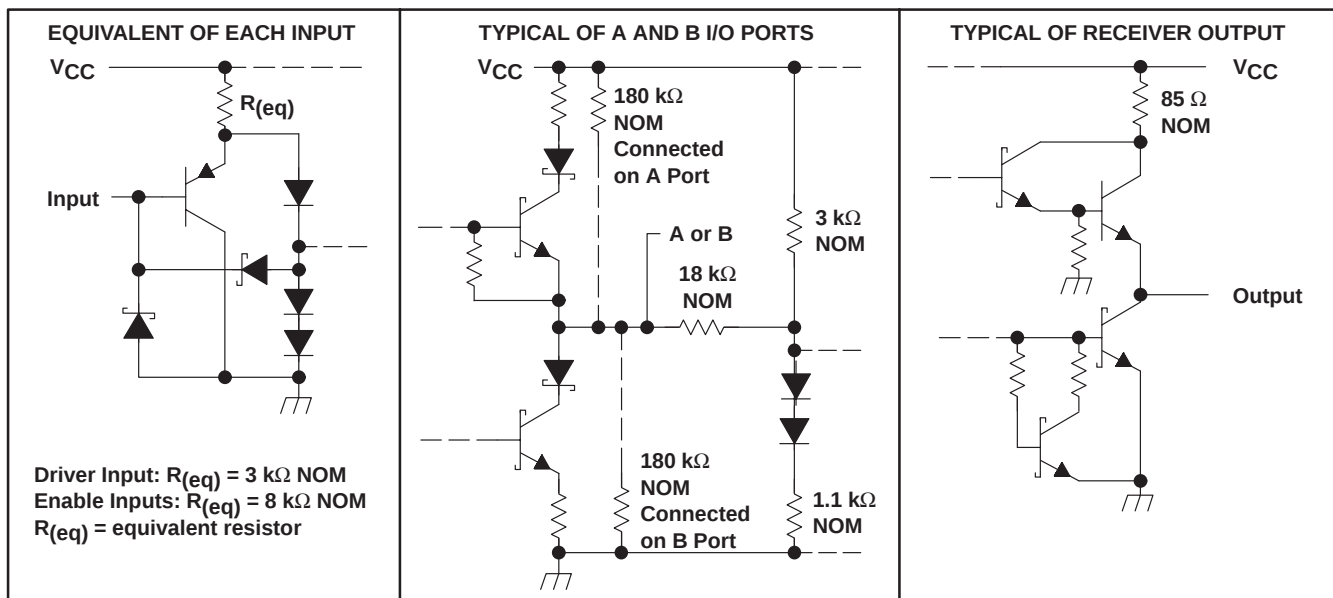


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



## schematic of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                  |                |
|------------------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)                            | 7 V            |
| Voltage range at any bus terminal                                | –10 V to 15 V  |
| Enable input voltage, $V_I$                                      | 5.5 V          |
| Operating free-air temperature range, $T_A$                      | 0°C to 70°C    |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 97°C/W         |
| PW package                                                       | 85°C/W         |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds     | 260°C          |
| Storage temperature range, $T_{stg}$                             | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.  
2. The package thermal impedance is calculated in accordance with JESD 51.

# TL3695

## DIFFERENTIAL BUS TRANSCEIVER

SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

### recommended operating conditions

|                                                                                            |                            | MIN  | NOM | MAX  | UNIT |
|--------------------------------------------------------------------------------------------|----------------------------|------|-----|------|------|
| Supply voltage, V <sub>CC</sub>                                                            |                            | 4.75 | 5   | 5.25 | V    |
| Voltage at any bus terminal (separately or common mode), V <sub>I</sub> or V <sub>IC</sub> |                            | 12   |     |      | V    |
|                                                                                            |                            | −7   |     |      |      |
| High-level Input voltage, V <sub>IH</sub>                                                  | D, DE, and $\overline{RE}$ | 2    |     |      | V    |
| Low-level Input voltage, V <sub>IL</sub>                                                   | D, DE, and $\overline{RE}$ | 0.8  |     |      | V    |
| Differential input voltage, V <sub>ID</sub> (see Note 3)                                   |                            | ±12  |     |      | V    |
| High-level output current, I <sub>OH</sub>                                                 | Driver                     | −60  |     |      | mA   |
|                                                                                            | Receiver                   | −400 |     |      | μA   |
| Low-level output current, I <sub>OL</sub>                                                  | Driver                     | 60   |     |      | mA   |
|                                                                                            | Receiver                   | 8    |     |      |      |
| Operating free-air temperature, T <sub>A</sub>                                             |                            | 0    |     | 70   | °C   |

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

## DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                           | TEST CONDITIONS <sup>†</sup>                   | MIN                                    | TYP <sup>‡</sup> | MAX  | UNIT |
|-------------------------------------------------------------------------------------|------------------------------------------------|----------------------------------------|------------------|------|------|
| V <sub>IK</sub> Input clamp voltage                                                 | I <sub>I</sub> = –18 mA                        |                                        |                  | –1.5 | V    |
| V <sub>O</sub> Output voltage                                                       | I <sub>O</sub> = 0                             | 0                                      |                  | 6    | V    |
| V <sub>OD1</sub>   Differential output voltage                                      | I <sub>O</sub> = 0                             | 1.5                                    |                  | 5    | V    |
| V <sub>OD2</sub>   Differential output voltage                                      | R <sub>L</sub> = 100 Ω, See Figure 1           | 1/2 V <sub>OD1</sub> or 2 <sup>§</sup> |                  |      | V    |
|                                                                                     | R <sub>L</sub> = 54 Ω, See Figure 1            | 1.5                                    | 2.5              | 5    | V    |
| V <sub>OD3</sub> Differential output voltage                                        | V <sub>test</sub> = –7 V to 12 V, See Figure 2 | 1.5                                    |                  | 5    | V    |
| Δ V <sub>OD</sub>   Change in magnitude of differential output voltage <sup>¶</sup> | R <sub>L</sub> = 54 Ω, See Figure 1            |                                        |                  | ±0.2 | V    |
| V <sub>OC</sub> Common-mode output voltage                                          |                                                |                                        |                  | 3    | V    |
| Δ V <sub>OC</sub>   Change in magnitude of common-mode output voltage <sup>¶</sup>  |                                                |                                        |                  | ±0.2 | V    |
| I <sub>O</sub> Output current                                                       | Output disabled, See Note 4                    | V <sub>O</sub> = 12 V                  |                  | 1    | mA   |
|                                                                                     |                                                | V <sub>O</sub> = –7 V                  |                  | –0.8 |      |
| I <sub>IH</sub> High-level input current                                            | V <sub>I</sub> = 2.4 V                         |                                        |                  | 20   | μA   |
| I <sub>IL</sub> Low-level input current                                             | V <sub>I</sub> = 0.4 V                         |                                        |                  | –200 | μA   |
| I <sub>OS</sub> Short-circuit output current <sup>#</sup>                           | V <sub>O</sub> = –6 V                          |                                        |                  | –250 | mA   |
|                                                                                     | V <sub>O</sub> = 0                             |                                        |                  | –150 |      |
|                                                                                     | V <sub>O</sub> = V <sub>CC</sub>               |                                        |                  | 250  |      |
|                                                                                     | V <sub>O</sub> = 8 V                           |                                        |                  | 250  |      |
| I <sub>CC</sub> Supply current                                                      | No load                                        | Outputs enabled                        | 23               | 50   | mA   |
|                                                                                     |                                                | Outputs disabled                       | 19               | 35   |      |

<sup>†</sup> The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

<sup>§</sup> The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.

<sup>¶</sup> Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

<sup>#</sup> Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER                                              | TEST CONDITIONS                                                                 | MIN | TYP <sup>‡</sup> | MAX | UNIT |
|--------------------------------------------------------|---------------------------------------------------------------------------------|-----|------------------|-----|------|
| t <sub>d(OD)</sub> Differential-output delay time      | C <sub>L1</sub> = C <sub>L2</sub> = 100 pF, R <sub>L</sub> = 60 Ω, See Figure 3 |     | 8                | 22  | ns   |
| Skew ( t <sub>d(ODH)</sub> – t <sub>d(ODL)</sub>  )    |                                                                                 |     | 1                | 8   | ns   |
| t <sub>t(OD)</sub> Differential output transition time |                                                                                 |     | 8                | 18  | ns   |
| t <sub>PZH</sub> Output enable time to high level      | C <sub>L</sub> = 100 pF, R <sub>L</sub> = 500 Ω, See Figure 4                   |     |                  | 50  | ns   |
| t <sub>PZL</sub> Output enable time to low level       | C <sub>L</sub> = 100 pF, R <sub>L</sub> = 500 Ω, See Figure 5                   |     |                  | 50  | ns   |
| t <sub>PHZ</sub> Output disable time from high level   | C <sub>L</sub> = 15 pF, R <sub>L</sub> = 500 Ω, See Figure 4                    |     | 8                | 30  | ns   |
| t <sub>PLZ</sub> Output disable time from low level    | C <sub>L</sub> = 15 pF, R <sub>L</sub> = 500 Ω, See Figure 5                    |     | 8                | 30  | ns   |

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

# TL3695

## DIFFERENTIAL BUS TRANSCEIVER

SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

### SYMBOL EQUIVALENTS

| DATA-SHEET PARAMETER | TIA/EIA-422-B               | TIA/EIA-485-A                          |
|----------------------|-----------------------------|----------------------------------------|
| $V_O$                | $V_{0a}, V_{0b}$            | $V_{0a}, V_{0b}$                       |
| $ V_{OD1} $          | $V_0$                       | $V_0$                                  |
| $ V_{OD2} $          | $V_t (R_L = 100 \Omega)$    | $V_t (R_L = 54 \Omega)$                |
| $ V_{OD3} $          |                             | $V_t$ (test termination measurement 2) |
| $V_{test}$           |                             | $V_{tst}$                              |
| $\Delta  V_{OD} $    | $   V_t  -  \bar{V}_t   $   | $   V_t  -  \bar{V}_t   $              |
| $V_{OC}$             | $ V_{os} $                  | $ V_{os} $                             |
| $\Delta  V_{OC} $    | $  V_{os} - \bar{V}_{os}  $ | $  V_{os} - \bar{V}_{os}  $            |
| $I_{OS}$             | $  I_{sa}  ,   I_{sb}  $    |                                        |
| $I_O$                | $  I_{xa}  ,   I_{xb}  $    | $I_{ia}, I_{ib}$                       |

### RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

| PARAMETER                                            | TEST CONDITIONS                                                                         | MIN                      | TYP <sup>†</sup> | MAX      | UNIT          |
|------------------------------------------------------|-----------------------------------------------------------------------------------------|--------------------------|------------------|----------|---------------|
| $V_{IT+}$ Positive-going input threshold voltage     | $V_O = 2.7 \text{ V}$ , $I_O = -0.4 \text{ mA}$                                         |                          |                  | 0.2      | V             |
| $V_{IT-}$ Negative-going input threshold voltage     | $V_O = 0.5 \text{ V}$ , $I_O = 8 \text{ mA}$                                            | $-0.2^{\ddagger}$        |                  |          | V             |
| $V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) | $V_{OC} = 0$                                                                            |                          | 70               |          | mV            |
| $V_{IK}$ Enable-input clamp voltage                  | $I_I = -18 \text{ mA}$                                                                  |                          |                  | -1.5     | V             |
| $V_{OH}$ High-level output voltage                   | $V_{ID} = 200 \text{ mV}$ or inputs open,<br>$I_{OH} = -400 \mu\text{A}$ , See Figure 6 | 2.4                      |                  |          | V             |
| $V_{OL}$ Low-level output voltage                    | $V_{ID} = -200 \text{ mV}$ ,<br>See Figure 6                                            | $I_{OL} = 16 \text{ mA}$ |                  | 0.5      | V             |
|                                                      |                                                                                         | $I_{OL} = 8 \text{ mA}$  |                  | 0.45     |               |
| $I_{OZ}$ High-impedance-state output current         | $V_O = 0.4 \text{ V}$ to $2.4 \text{ V}$                                                |                          |                  | $\pm 20$ | $\mu\text{A}$ |
| $I_I$ Line input current                             | Other input = 0,<br>See Note 5                                                          | $V_I = 12 \text{ V}$     |                  | 1        | mA            |
|                                                      |                                                                                         | $V_I = -7 \text{ V}$     |                  | -0.8     |               |
| $I_{IH}$ High-level enable-input current             | $V_{IH} = 2.7 \text{ V}$                                                                |                          |                  | 20       | $\mu\text{A}$ |
| $I_{IL}$ Low-level enable-input current              | $V_{IL} = 0.4 \text{ V}$                                                                |                          |                  | -100     | $\mu\text{A}$ |
| $r_I$ Input resistance                               |                                                                                         | 12                       |                  |          | k $\Omega$    |
| $I_{OS}$ Short-circuit output current <sup>§</sup>   | $V_O = 0$                                                                               | -15                      |                  | -85      | mA            |
| $I_{CC}$ Supply current                              | No load                                                                                 | Outputs enabled          | 23               | 50       | mA            |
|                                                      |                                                                                         | Outputs disabled         | 19               | 35       |               |

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

<sup>§</sup> Duration of the short circuit should not exceed one second for this test.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range,  $C_L = 15 \text{ pF}$

| PARAMETER                                                   | TEST CONDITIONS                                               | MIN | TYP† | MAX | UNIT |
|-------------------------------------------------------------|---------------------------------------------------------------|-----|------|-----|------|
| $t_{PLH}$ Propagation delay time, low- to high-level output | $V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$ ,<br>See Figure 7 |     | 14   | 37  | ns   |
| $t_{PHL}$ Propagation delay time, high- to low-level output |                                                               |     | 14   | 37  | ns   |
| $t_{PZH}$ Output enable time to high level                  | See Figure 8                                                  |     | 7    | 20  | ns   |
| $t_{PZL}$ Output enable time to low level                   |                                                               |     | 7    | 20  | ns   |
| $t_{PHZ}$ Output disable time from high level               | See Figure 8                                                  |     | 7    | 16  | ns   |
| $t_{PLZ}$ Output disable time from low level                |                                                               |     | 8    | 16  | ns   |

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION

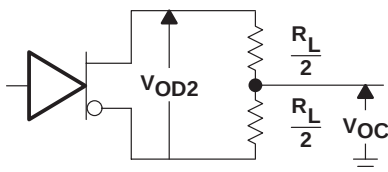


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

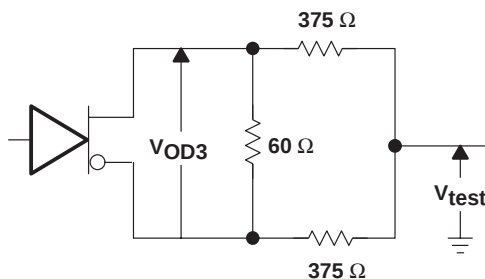
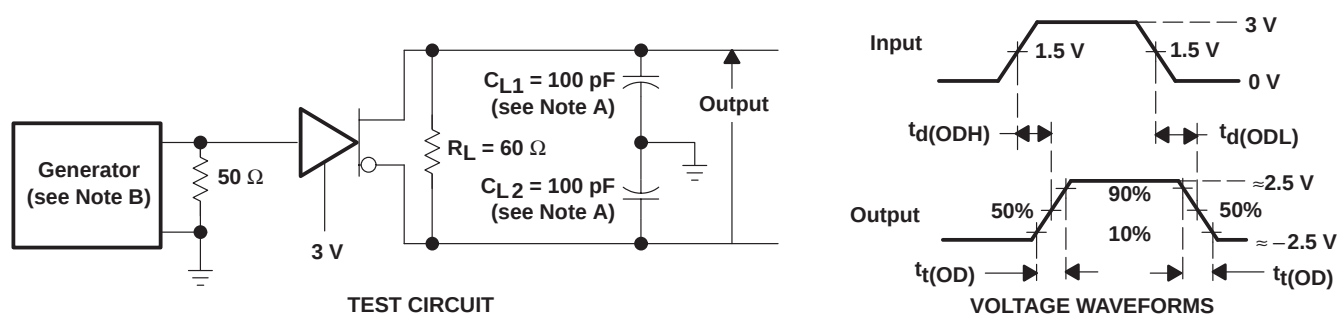


Figure 2. Driver  $V_{OD3}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .

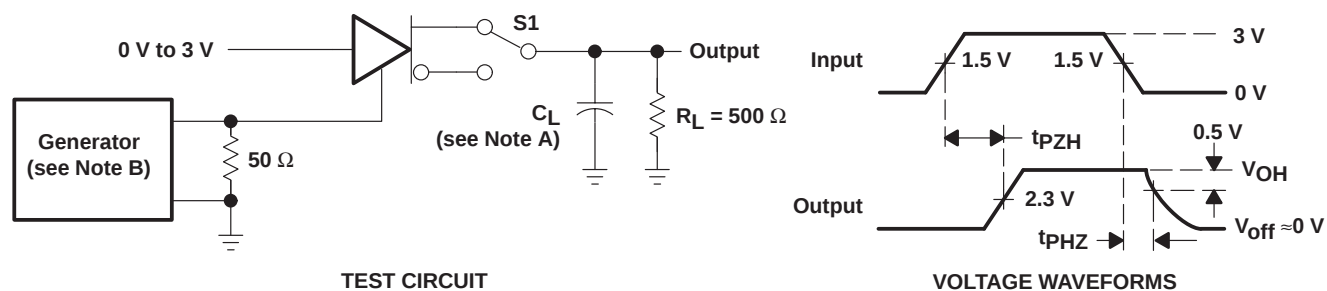
Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms

# TL3695

## DIFFERENTIAL BUS TRANSCEIVER

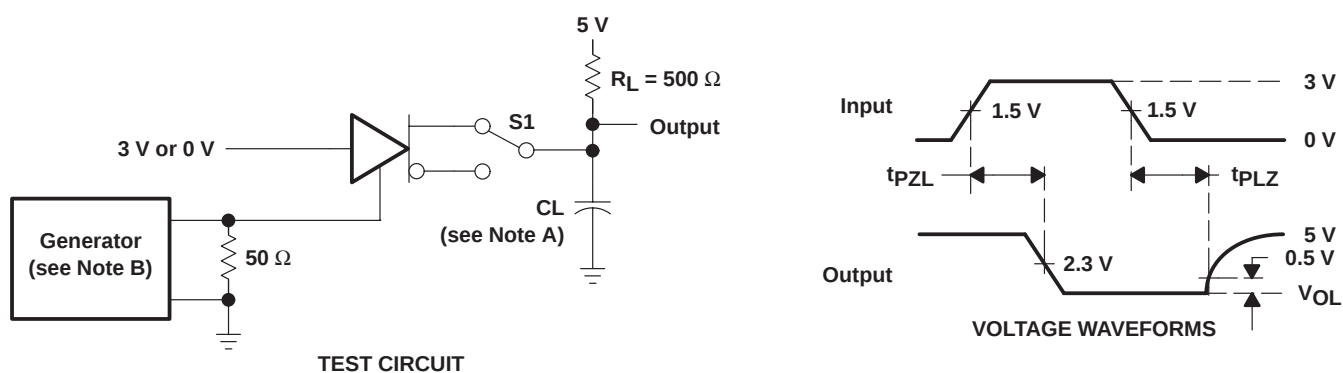
SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

Figure 4. Driver Test Circuit and Voltage Waveforms



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

Figure 5. Driver Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION

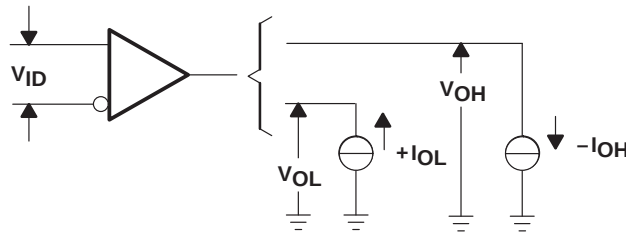
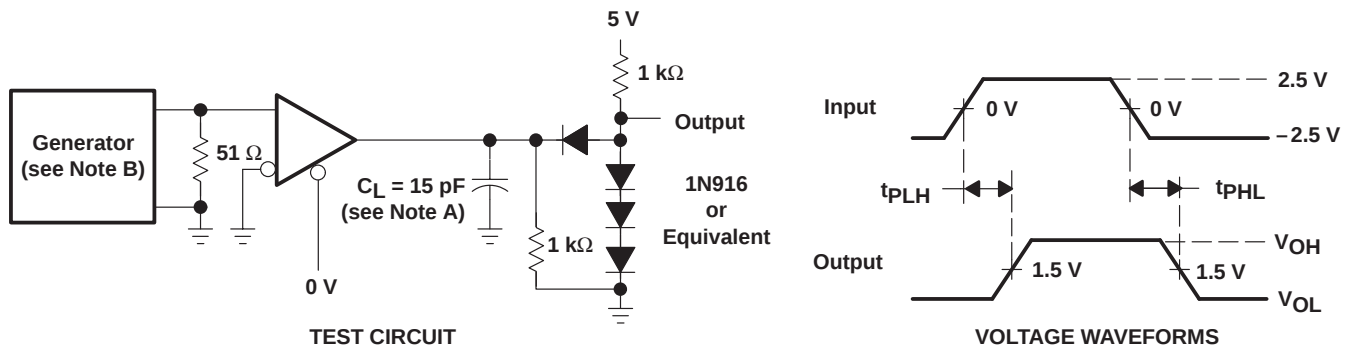


Figure 6. Receiver  $V_{OH}$  and  $V_{OL}$



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

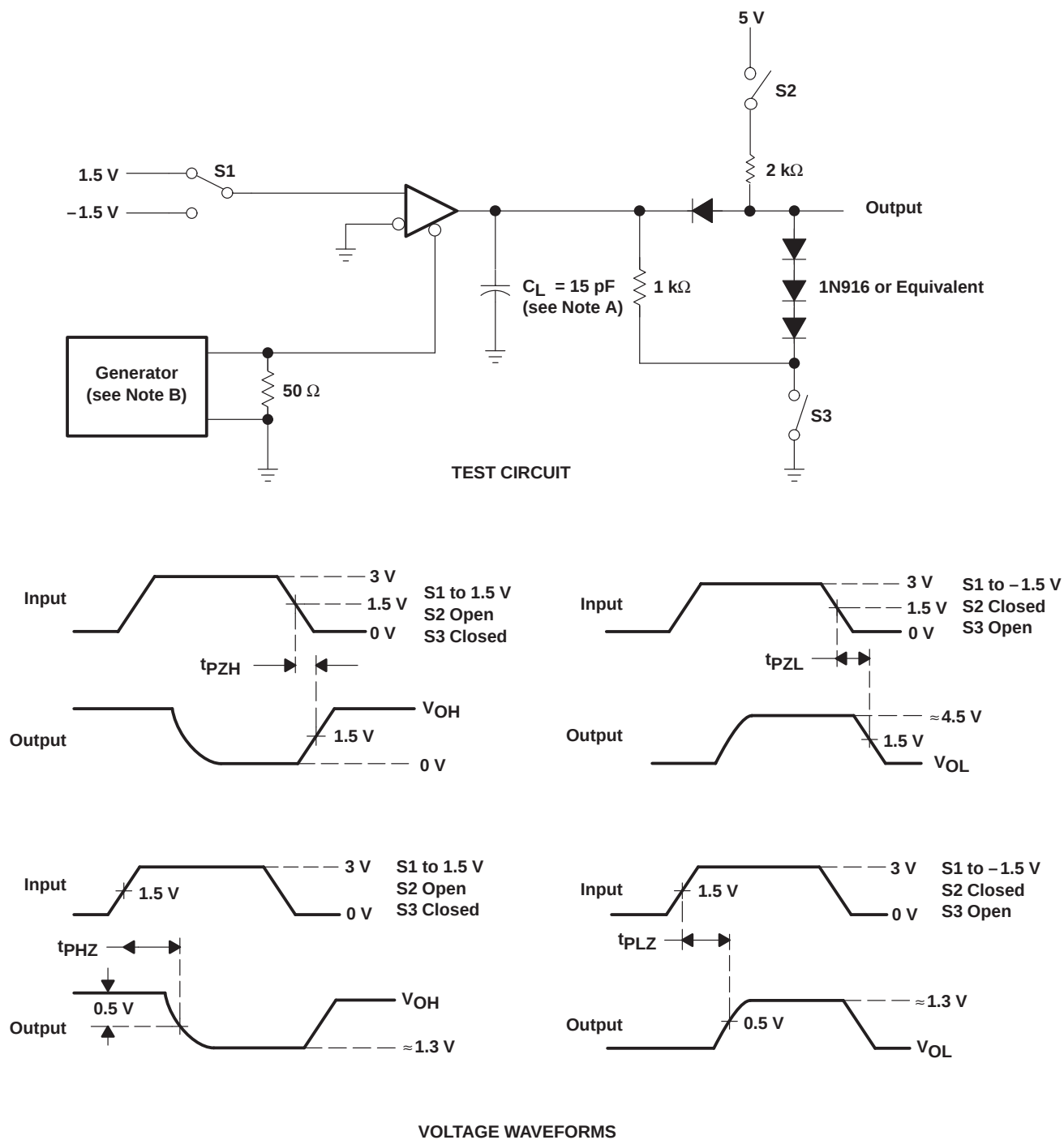
Figure 7. Receiver Test Circuit and Voltage Waveforms

# TL3695

## DIFFERENTIAL BUS TRANSCEIVER

SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

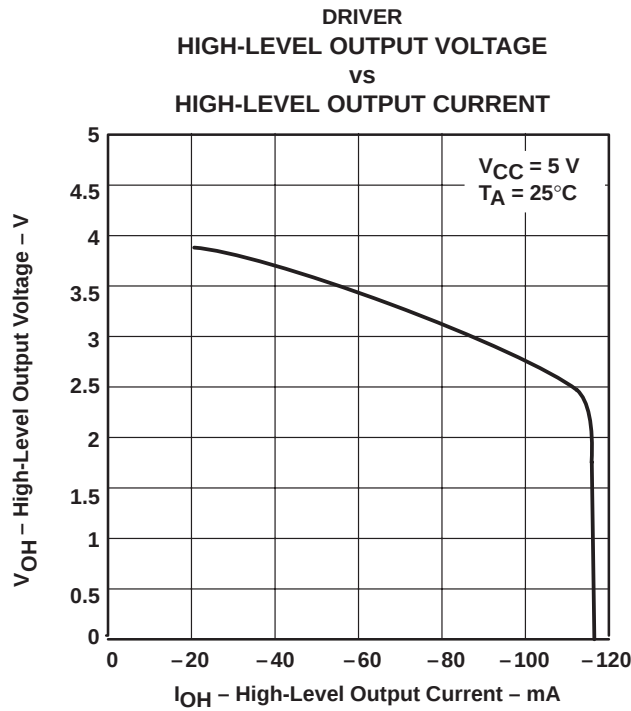


Figure 9

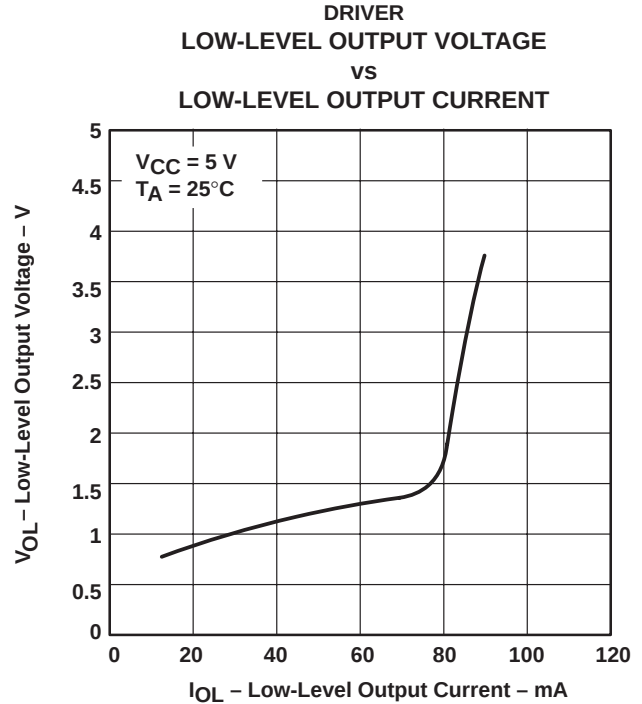


Figure 10

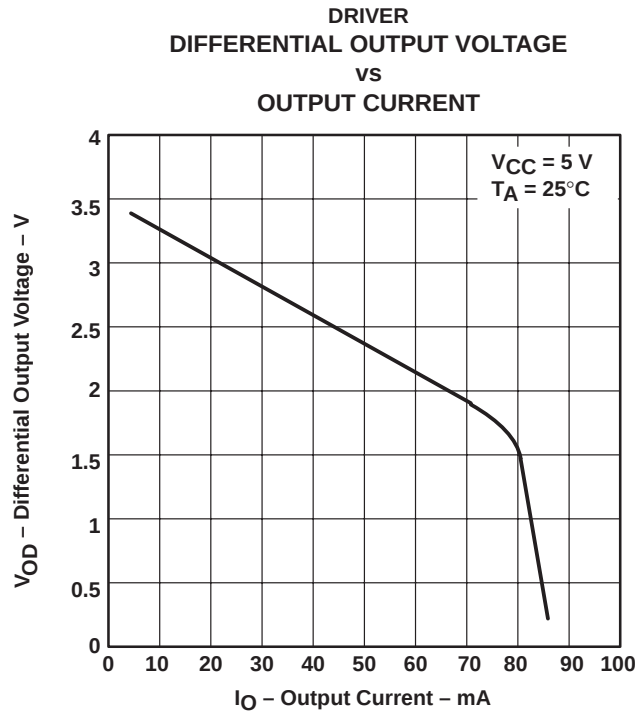


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TL3695  
DIFFERENTIAL BUS TRANSCEIVER

SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

TYPICAL CHARACTERISTICS†

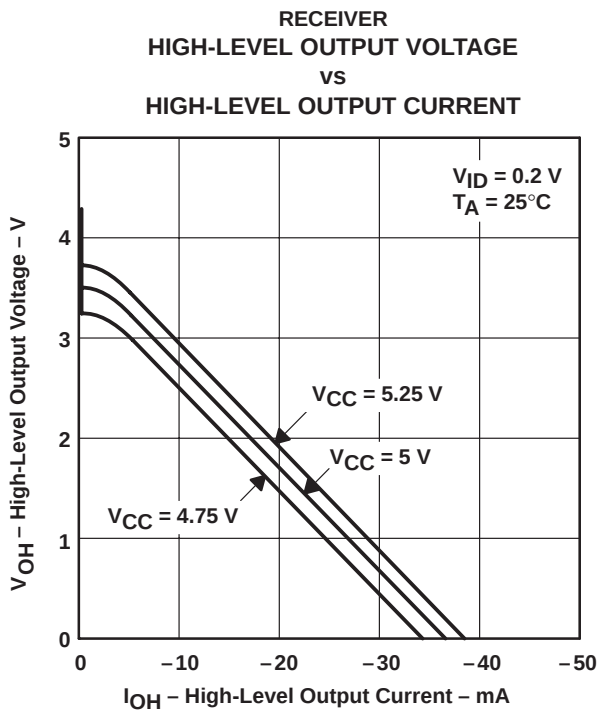


Figure 12

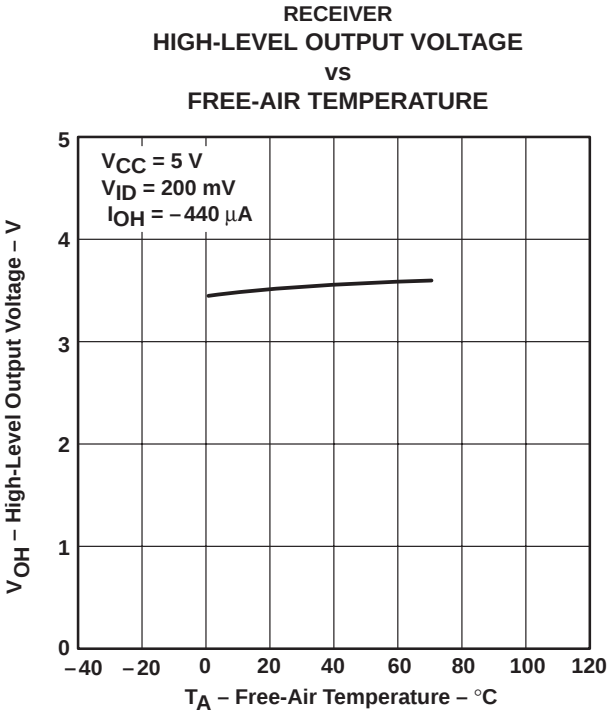


Figure 13

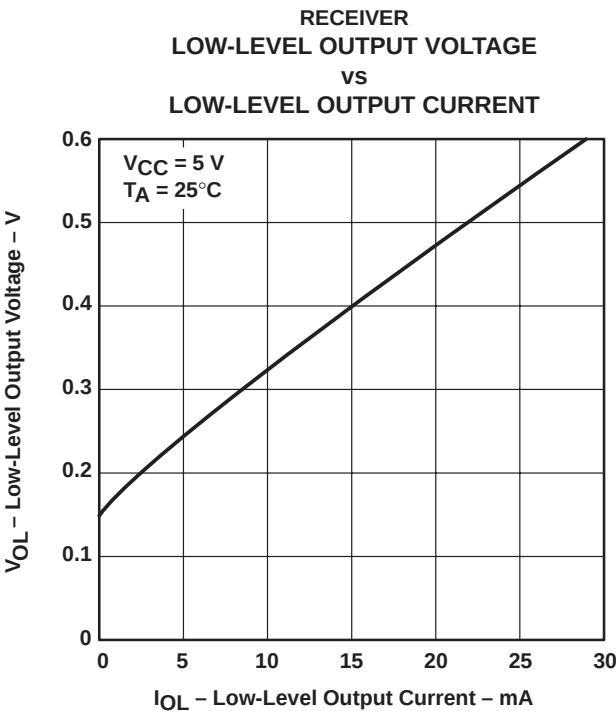


Figure 14

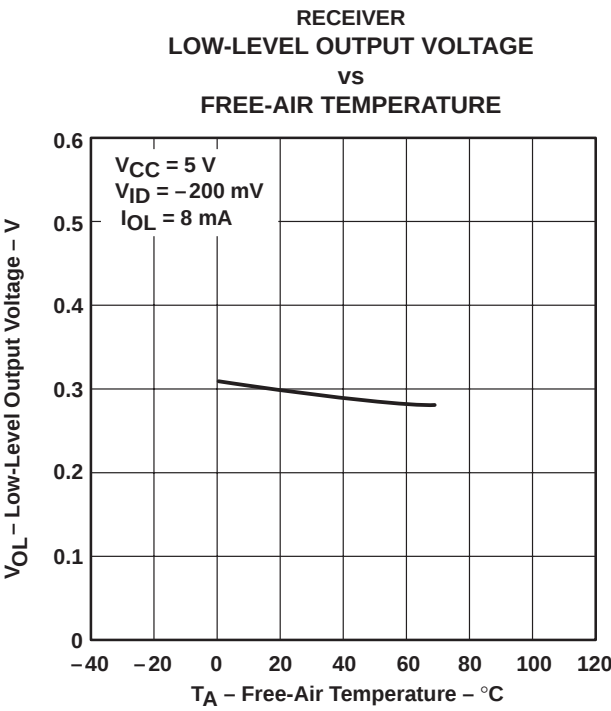


Figure 15

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

## TYPICAL CHARACTERISTICS†

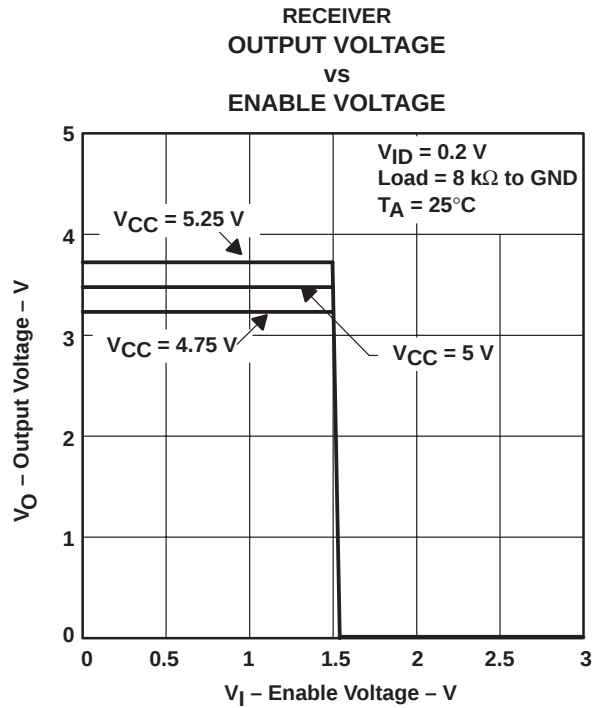


Figure 16

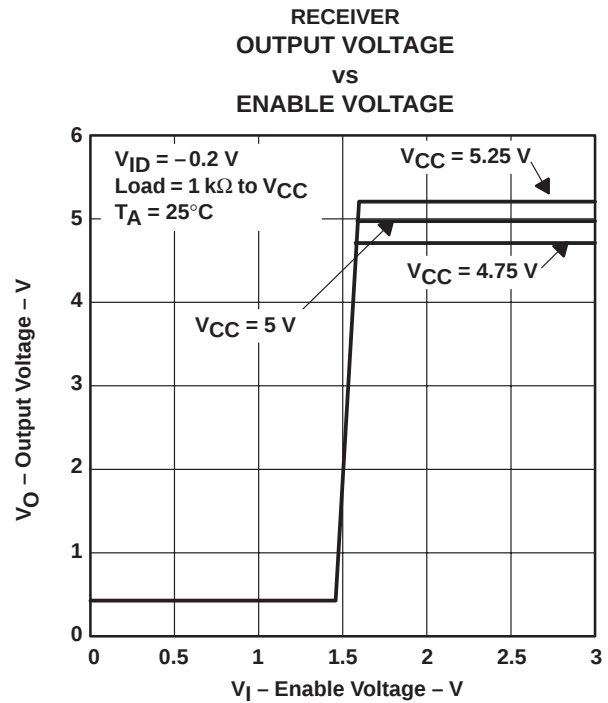
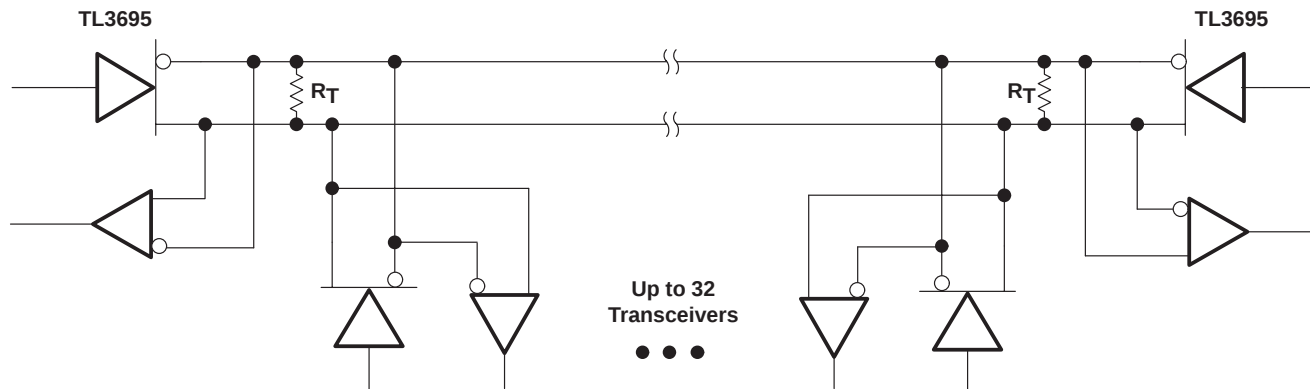


Figure 17

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

## APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

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