

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62318AP, TD62318AF

4CH LOW INPUT ACTIVE HIGH-CURRENT DARLINGTON SINK DRIVER

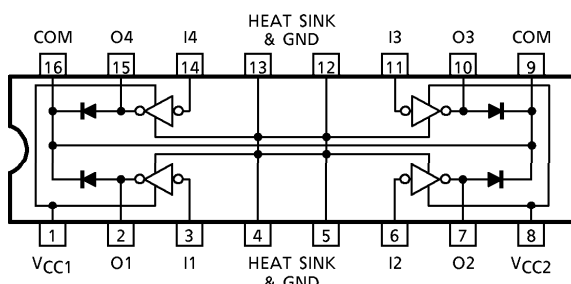
The TD62318AP, TD62318AF are non-inverting transistor array which are comprised of four NPN darlington output stages and PNP input stages. These devices are low level input active driver and are suitable for operation with TTL, 5V CMOS and 5V Microprocessor which have sink current output drivers. Applications include relay, hammer, lamp and stepping moter drivers.

FEATURES

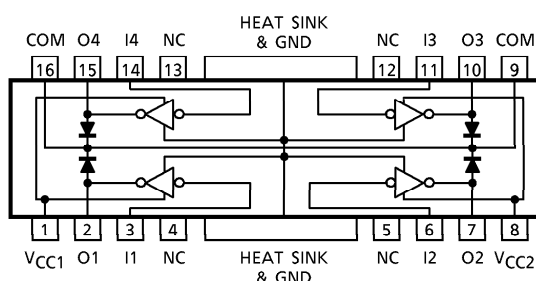
- Output current (single output) 700mA (Max.)
- High sustaining voltage output 50V (Min.)
- Output clamp diodes
- Input compatible with TTL and 5V CMOS
- Low level active inputs
- Standard supply voltage
- Two V_{CC} terminals V_{CC1} , V_{CC2} (separated)
- GND and SUB terminal = heat sink
- Package type-AP : DIP-16pin
- Package type-AF : PFP-16pin

PIN CONNECTION (TOP VIEW)

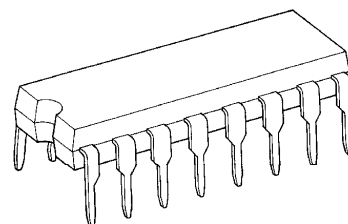
TD62318AP



TD62318AF

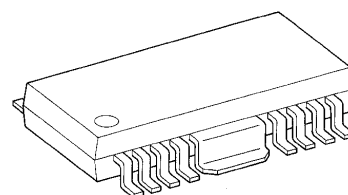


TD62318AP



DIP16-P-300-2.54A

TD62318AF

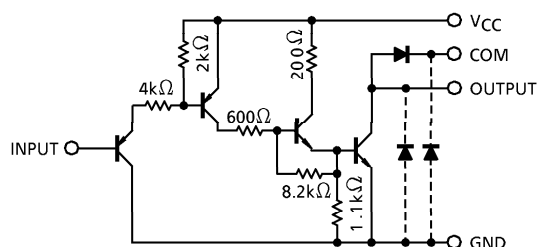


HSOP16-P-300-1.00

Weight

DIP16-P-300-2.54A : 1.11g (Typ.)
HSOP16-P-300-1.00 : 0.50g (Typ.)

SCHEMATICS (EACH DRIVER)



(Note) The input and output parasitic diodes cannot be used as clamp diodes.

961001EBA2

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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	– 0.5~17	V
Output Sustaining Voltage	V _{CE (SUS)}	– 0.5~50	V
Output Current	I _{OUT}	700	mA / ch
Input Current	I _{IN}	– 10	mA
Input Voltage	V _{IN}	– 0.5~30	V
Clamp Diode Reverse Voltage	V _R	50	V
Clamp Diode Forward Current	I _F	700	mA
Power Dissipation	P _D	1.47 / 2.7 (Note 1)	W
		0.9 / 1.4 (Note 2)	
Operating Temperature	T _{opr}	– 40~85	°C
Storage Temperature	T _{stg}	– 55~150	°C

(Note 1) On Glass Epoxy (50×50×1.6mm Cu 50%)

(Note 2) On Glass Epoxy (60×30×1.6mm Cu 30%)

RECOMMENDED OPERATING CONDITIONS (Ta = – 40~85°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{CC}		4.5	—	5.5	V
Output Sustaining Voltage	V _{CE (SUS)}		0	—	50	V
Output Current	I _{OUT}	DC 1 circuit, Ta = 25°C	0	—	570	mA / ch
		T _{pw} = 25ms	0	—	570	
		Duty = 10%	0	—	570	
		Duty = 50%	0	—	570	
		4 circuits	0	—	570	
		Ta = 85°C	0	—	570	
		T _j = 120°C	0	—	480	
Input Voltage	V _{IN}		0	—	15	V
Input Voltage	Output On	V _{IN (ON)}	0	—	V _{CC} – 3.6	V
	Output Off	V _{IN (OFF)}	V _{CC} – 1.6	—	5.5	
Clamp Diode Reverse Voltage	V _R		—	—	50	V
Clamp Diode Forward Current	I _F		—	—	500	mA
Power Dissipation	AP	Ta = 85°C (Note 1)	—	—	1.4	W
	AF	Ta = 85°C (Note 2)	—	—	0.7	

(Note 1) On Glass Epoxy (50×50×1.6mm Cu 50%)

(Note 2) On Glass Epoxy (60×30×1.6mm Cu 30%)

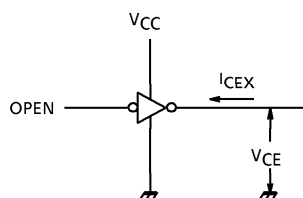
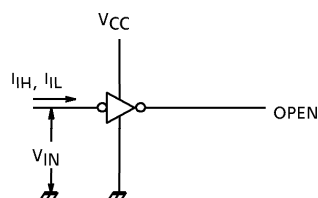
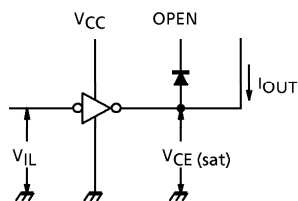
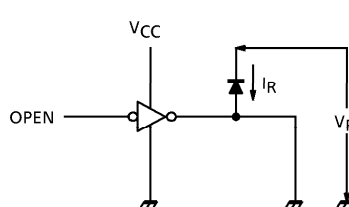
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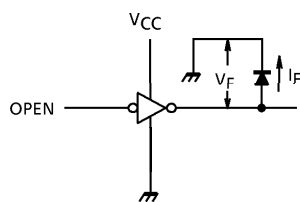
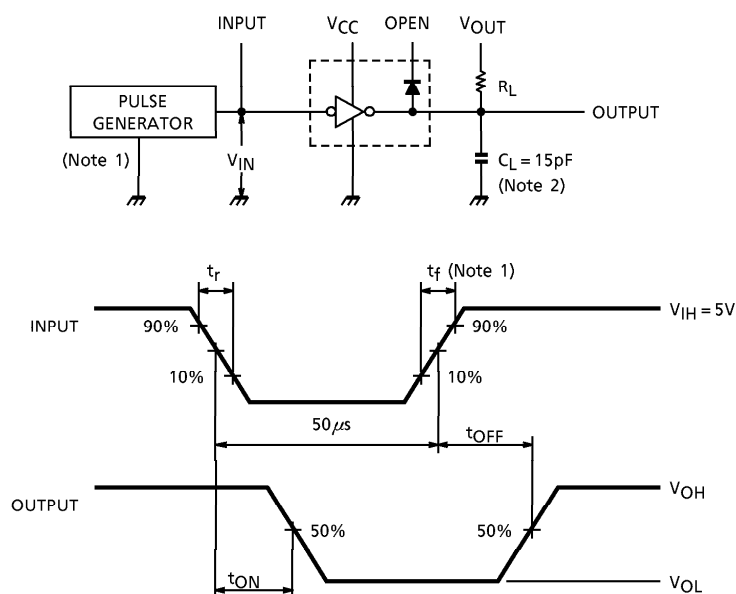
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ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	—		$V_{CC} - 1.6$	—	25	V
	"L" Level	V_{IL}			0	—	$V_{CC} - 3.6$	
Input Current	"H" Level	I_{IH}	2		—	—	10	μA
	"L" Level	I_{IL}			—	-0.05	-0.36	mA
Output Leakage Current		I_{CEX}	1	$V_{CE} = 50V, Ta = 25^{\circ}C$	—	—	50	μA
				$V_{CE} = 50V, Ta = 85^{\circ}C$	—	—	100	
Output Saturation Voltage		$V_{CE(sat)}$	3	$I_{OUT} = 0.5A, V_{CC} = 4.5V$	—	—	0.8	V
				$I_{OUT} = 0.2A, V_{CC} = 4.5V$	—	—	0.45	
Clamp Diode Reverse Current		I_R	4	$V_R = 50V, Ta = 25^{\circ}C$	—	—	50	μA
				$V_R = 50V, Ta = 85^{\circ}C$	—	—	100	
Clamp Diode Forward Voltage		V_F	5	$I_F = 500mA$	—	—	2.0	V
Supply Current	Output On	$I_{CC(ON)}$	2	$V_{CC} = 5.5V, V_{IN} = 0V$	—	35	40	mA / ch
	Output Off	$I_{CC(OFF)}$	2	$V_{CC} = 5.5V, V_{IN} = V_{CC}$	—	—	10	μA
Turn-On Delay		t_{ON}	6	$V_{OUT} = 50V, R_L = 90\Omega$	—	0.4	0.8	μs
Turn-Off Delay		t_{OFF}		$V_{CC} = 5.0V, C_L = 15pF$	—	8.0	16.0	

TEST CIRCUIT

1. I_{CEX} 2. I_{IH}, I_{IL} 3. $V_{CE(sat)}$ 4. I_R 

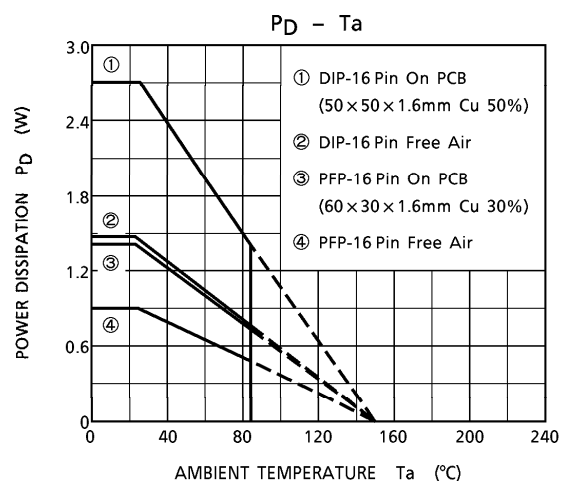
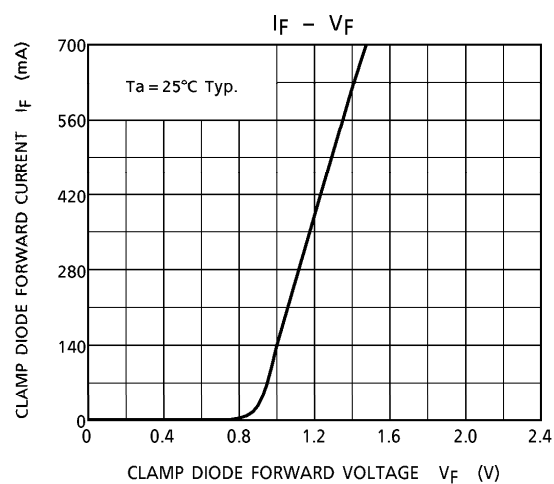
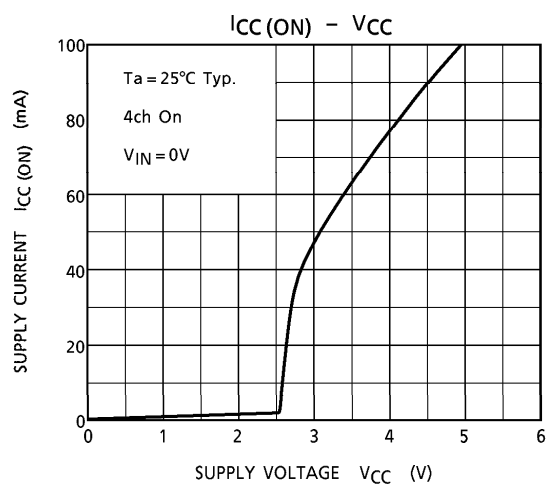
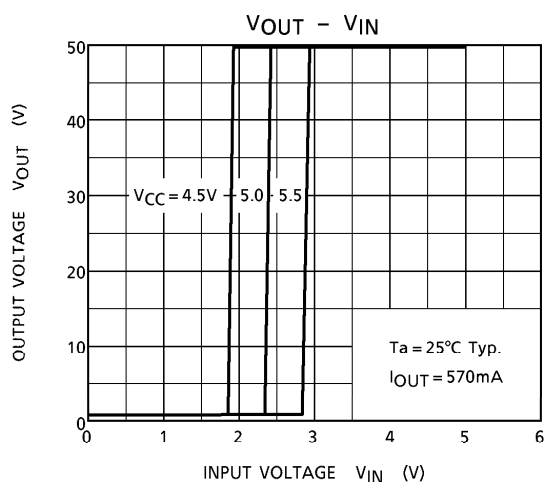
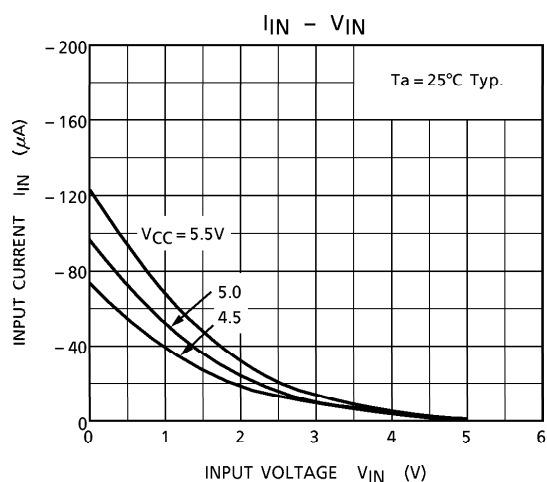
5. V_F

6. t_{ON} , t_{OFF}


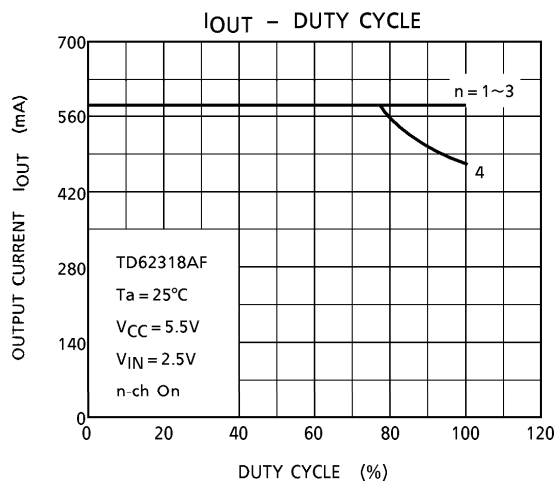
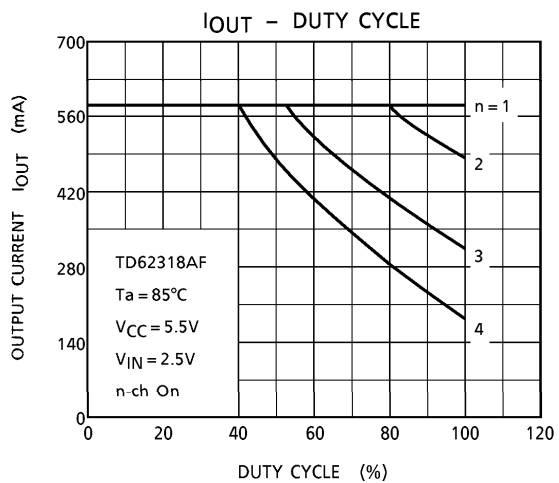
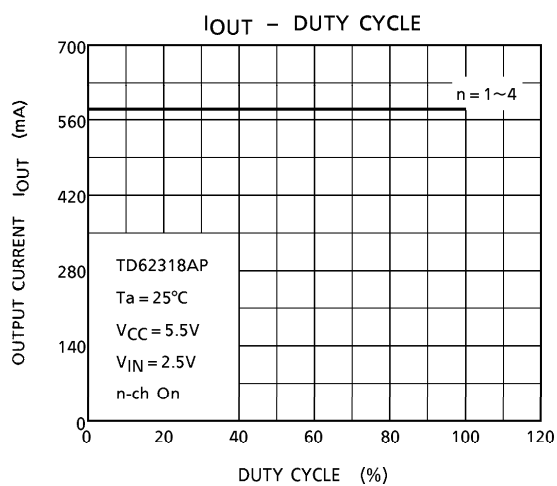
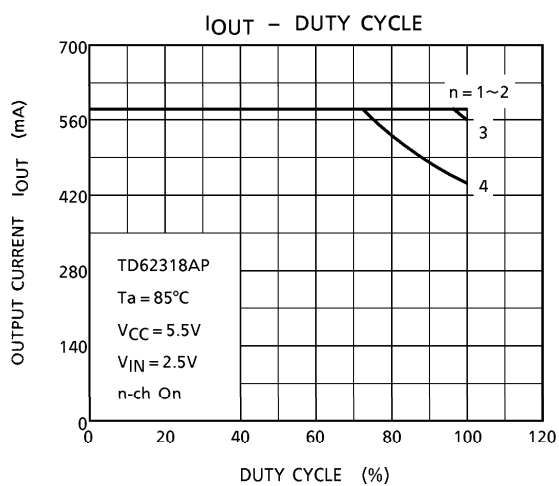
(Note 1) Pulse width $50\mu s$, duty cycle 10%
Output impedance 50Ω $t_r \leq 5ns$, $t_f \leq 10ns$

(Note 2) C_L includes probe and jig capacitance.

PRECAUTIONS for USING

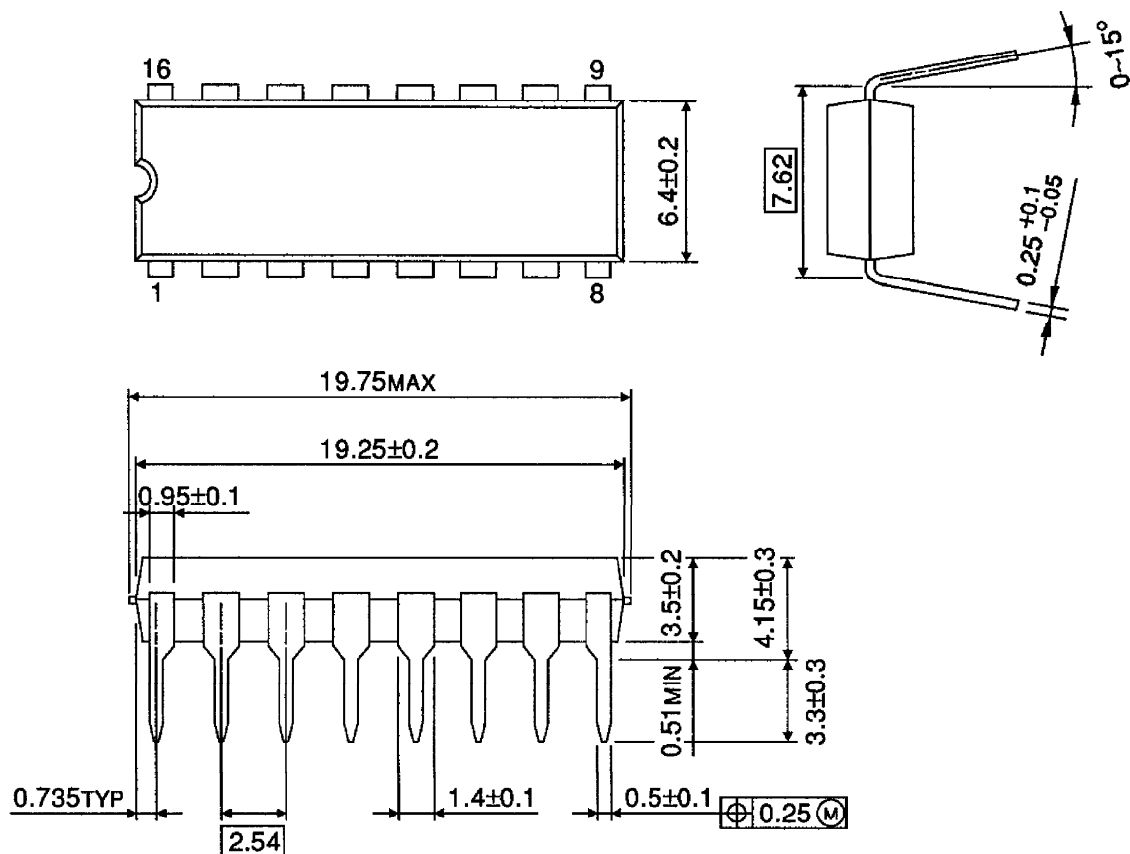
Utmost care is necessary in the design of the output line, V_{CC} , COMMON and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.





OUTLINE DRAWING
DIP16-P-300-2.54A

Unit : mm

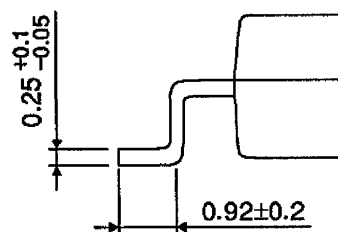
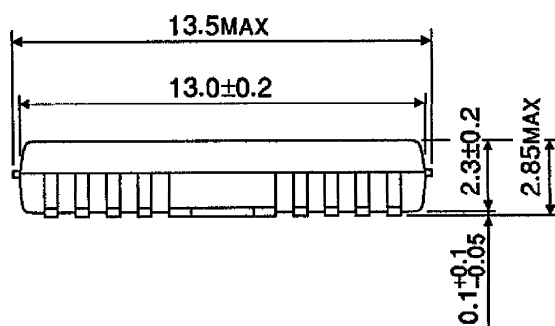
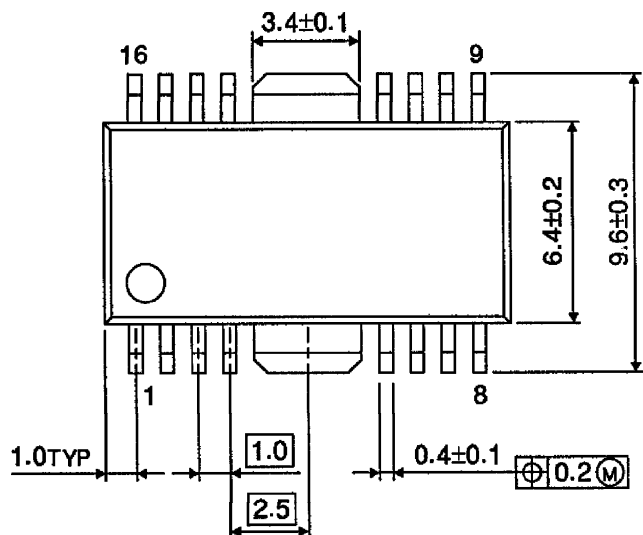


Weight : 1.11g (Typ.)

OUTLINE DRAWING

HSOP16-P-300-1.00

Unit : mm



Weight : 0.50g (Typ.)