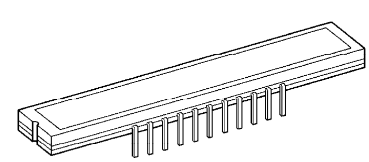
TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD2252D

The TCD2252D is a high sensitive and low dark current 2700 elements×3 line CCD color image sensor.
The sensor is designed for color scanner.
The device contains a row of 2700 elements×3 line photodiodes which provide a 12 lines/mm across a A4 size paper. The device is operated by 5V pulse, and 12V power supply.



WDIP22-G-400-2.54C

Weight : 4.5g (Typ.)

FEATURES

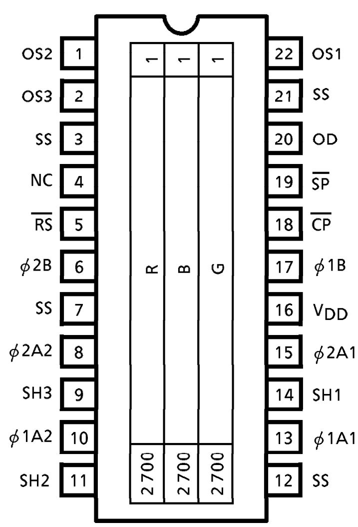
- Number of Image Sensing Elements : 2700 elements×3 line
- Image Sensing Element Size : 8μm by 8μm on 8μm centers
- Photo Sensing Region : High sensitive pn photodiode
- Distance Between Photodiode Array : 64μm (8 Lines)
- Clock : 2 phase (5V)
- Internal Circuit : Sample and Hold circuit, Clamp circuit
- Package : 22 pin DPI CERDIP package
- Color Filter : Red, Green, Blue

MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_ϕ	−0.3~8	V
Shift Pulse Voltage	V_{SH}		V
Reset Pulse Voltage	$V_{\overline{RS}}$		V
Sample and Hold Pulse Voltage	$V_{\overline{SP}}$		V
Clamp Pulse Voltage	$V_{\overline{CP}}$		V
Power Supply Voltage	V_{OD} V_{DD}	−0.3~15	V
Operating Temperature	T_{opr}	0~60	℃
Storage Temperature	T_{stg}	−25~85	℃

(Note 1) All voltage are with respect to SS terminals (Ground).

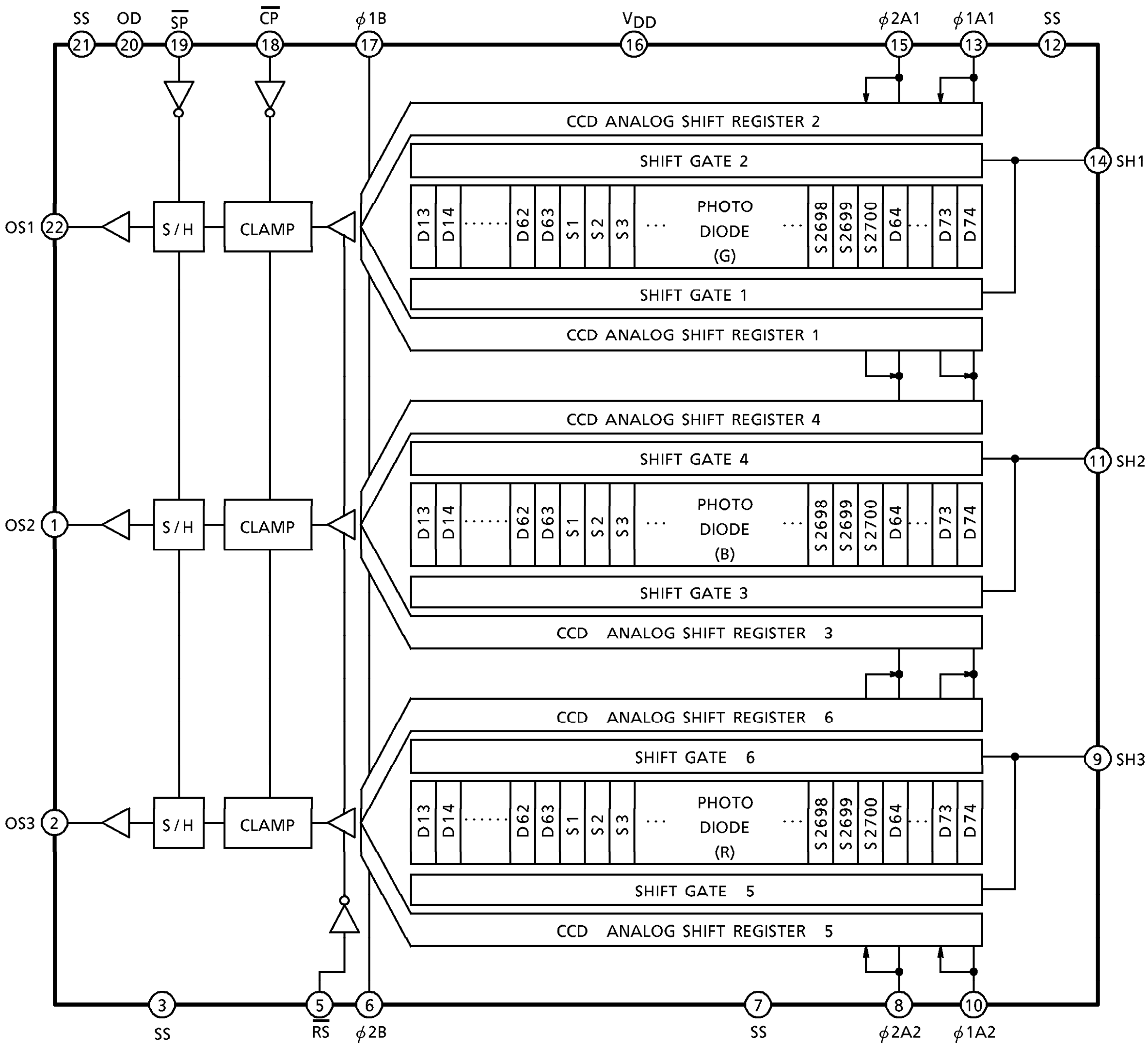
PIN CONNECTION



(TOP VIEW)

961001EBA2

CIRCUIT DIAGRAM



961001EBA2'

PIN NAMES

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS2	Signal Output 2 (Blue)	12	SS	Ground
2	OS3	Signal Output 3 (Red)	13	$\phi 1A1$	Clock 1 (phase 1)
3	SS	Ground	14	SH1	Shift Gate 1
4	NC	Non Connection	15	$\phi 2A1$	Clock 1 (phase 2)
5	$\overline{RS}$	Reset Gate	16	V_{DD}	Power (Digital)
6	$\phi 2B$	Final Stage Clock (phase 2)	17	$\phi 1B$	Final Stage Clock (phase 1)
7	SS	Ground	18	$\overline{CP}$	Clamp Gate
8	$\phi 2A2$	Clock 2 (Phase 2)	19	$\overline{SP}$	Sample and Hold Gate
9	SH3	Shift Gate 3	20	OD	Power (Analog)
10	$\phi 1A2$	Clock 2 (Phase 1)	21	SS	Ground
11	SH2	Shift Gate 2	22	OS1	Signal Output 1 (Green)

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{OD} = 12V, $V\phi = V_{\overline{RS}} = V_{SH} = V_{\overline{CP}}$ = 5V (PULSE), $f\phi$ = 0.5MHz, $f_{\overline{RS}}$ = 1.0MHz,
LOAD RESISTANCE = 100kΩ, t_{INT} (INTEGRATION TIME) = 10ms,
LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1.0mm))

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	Red	R_R	—	7.0	—	V / lx·s	(Note 2)
	Green	R_G	—	9.1	—		
	Blue	R_B	—	3.2	—		
Photo Response Non Uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Register Imbalance		RI	—	—	3	%	(Note 5)
Saturation Output Voltage		V_{SAT}	3.0	3.2	—	V	(Note 6)
Saturation Exposure		SE	—	0.35	—	lx·s	(Note 7)
Dark Signal Voltage		V_{DRK}	—	2.0	6.0	mV	(Note 8)
Dark Signal Non Uniformity		DSNU	—	4.0	8.0	mV	(Note 9)
Total Transfer Efficiency		TTE	92	—	—	%	
Output Impedance		Z_o	—	0.3	1.0	kΩ	
DC Power Dissipation		P_D	—	250	400	mW	
DC Signal Output Voltage		V_{OS}	3.0	5.5	8.0	V	(Note 10)
Random Noise		$N_{D\sigma}$	—	0.8	—	mV	(Note 11)

(Note 2) Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

(Note 3) PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta\chi}{\overline{\chi}} \times 100\ (\%)$$

Where $\overline{\chi}$ is average of total signal outputs and $\Delta\chi$ is the maximum deviation from $\overline{\chi}$. The amount of the incident light is shown below.

$$\text{Red} = \frac{1}{2}\ \text{SE}$$

$$\text{Green} = \frac{1}{2}\ \text{SE}$$

$$\text{Blue} = \frac{1}{4}\ \text{SE}$$

(Note 4) PRNU (3) is defined as maximum voltage difference between two adjacent pixels, where measured at 50mV (Typ.).

(Note 5) RI is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{RI} = \frac{\sum_{n=1}^{2699} |\chi n - \chi n+1|}{2699 \cdot \overline{\chi}} \times 100\ (\%)$$

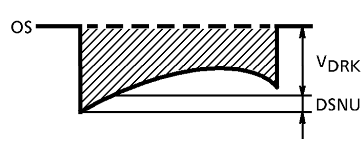
Where χn and $\chi n+1$ are signal outputs of each pixel. $\overline{\chi}$ is average of signal outputs of all effective pixels.

(Note 6) V_{SAT} is defined as minimum Saturation Output Voltage of all effective pixels.

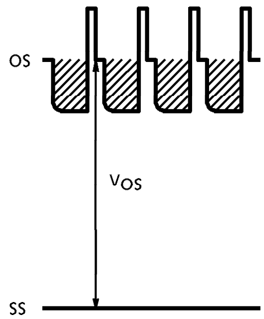
(Note 7) Definition of SE : $SE = \frac{V_{SAT}}{R_G}$ (lx·s)

(Note 8) V_{DRK} is defined as average dark signal voltage of all effective pixels.

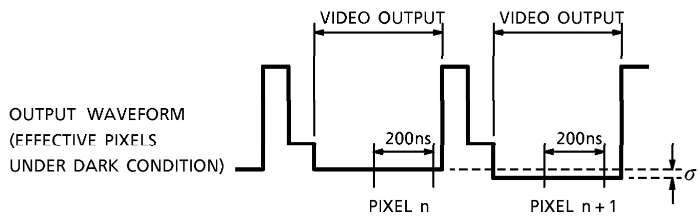
(Note 9) DSNU is defined as different voltage between V_{DRK} and V_{MDK}, when V_{MDK} is maximum dark voltage.



(Note 10) DC Signal Output Voltage is defined as follows:



(Note 11) Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
2) Each of the output levels at video output periods averaged over 200 nanosecond period to get Vn and Vn + 1.
3) Vn + 1 is subtracted from Vn to get ΔV.

   $\Delta V = Vn - Vn + 1$

4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta Vi| - \overline{\Delta V})^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma values. 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma j$$

6) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$\text{Random noise} = \frac{1}{\sqrt{2}} \overline{\sigma}$$

OPERATING CONDITION

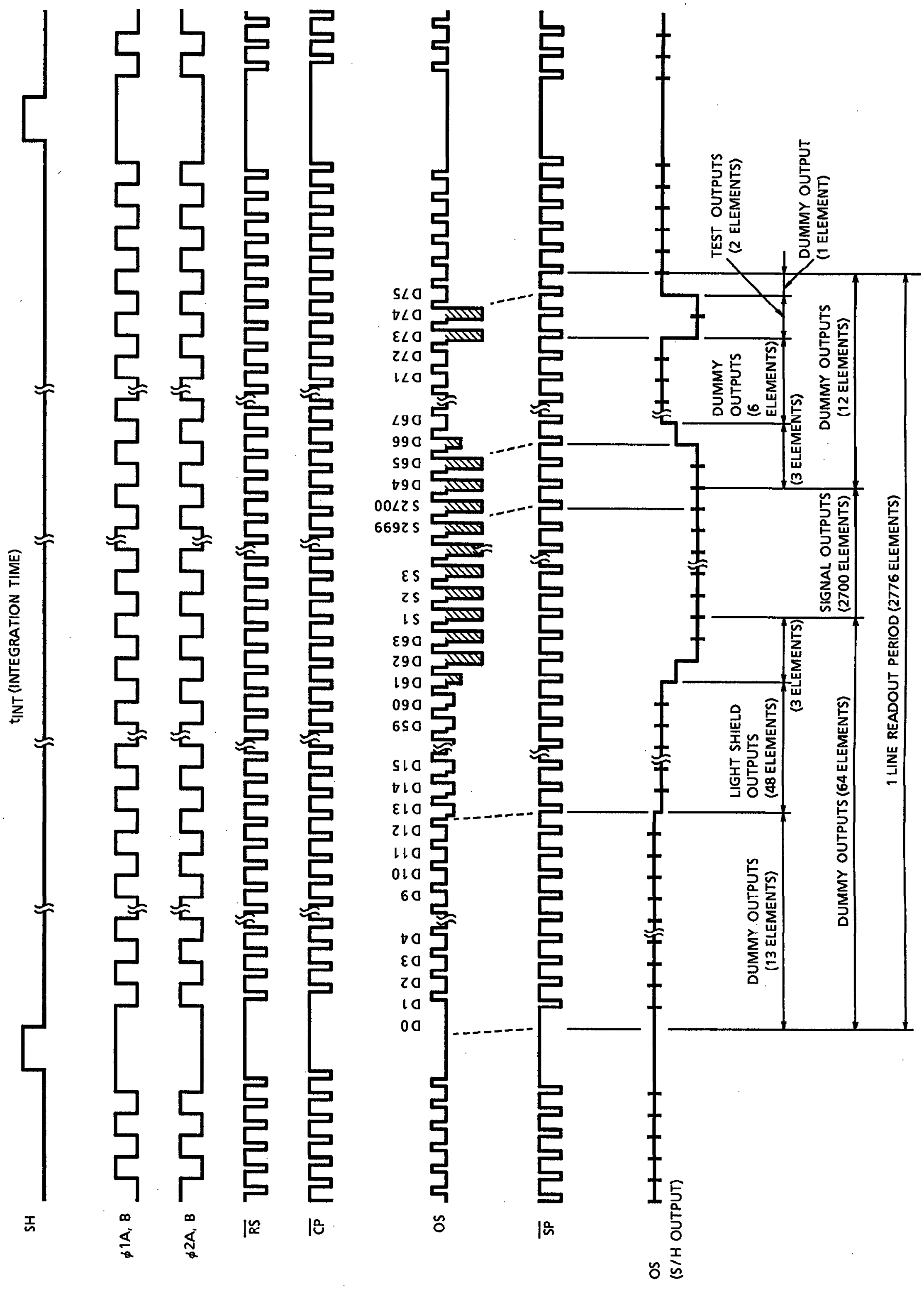
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Pulse Voltage	"H" Level	$V\phi 1A$	4.5	5.0	5.5	V	
	"L" Level	$V\phi 2A$	0	0	0.5		
Final Stage Clock Pulse Voltage	"H" Level	$V\phi 1B$	4.5	5.0	5.5	V	
	"L" Level	$V\phi 2B$	0	0	0.5		
Shift Pulse Voltage	"H" Level	V_{SH}	$V\phi A$"H"-0.5	$V\phi A$"H"	$V\phi A$"H"	V	(Note 12)
	"L" Level		0	0	0.5		
Reset Pulse Voltage	"H" Level	$V_{\overline{RS}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.5		
Sample and Hold Pulse Voltage	"H" Level	$V_{\overline{SP}}$	4.5	5.0	5.5	V	(Note 13)
	"L" Level		0	0	0.5		
Clamp Pulse Voltage	"H" Level	$V_{\overline{CP}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.5		
Power Supply Voltage		V_{OD} V_{DD}	11.4	12.0	13.0	V	

(Note 12) $V\phi A$"H" means the high level voltage of $V\phi A$ when SH pulse is high level.
(Note 13) Supply "L" Level to $\overline{SP}$ terminal when sample and hold circuit is not used.

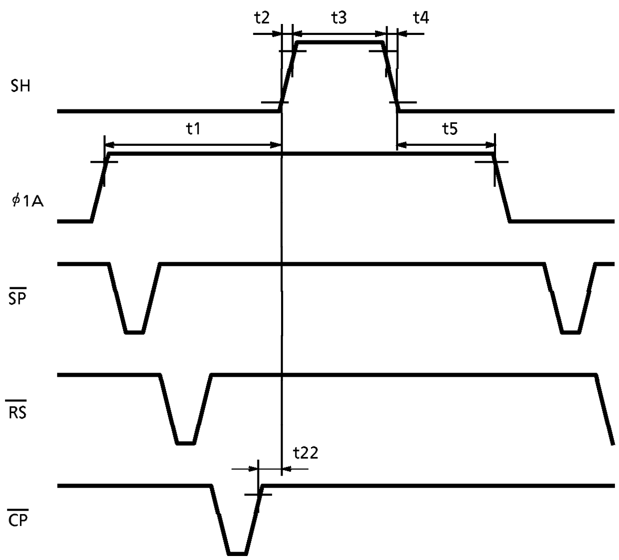
CLOCK CHARACTERISTICS (Ta = 25°C)

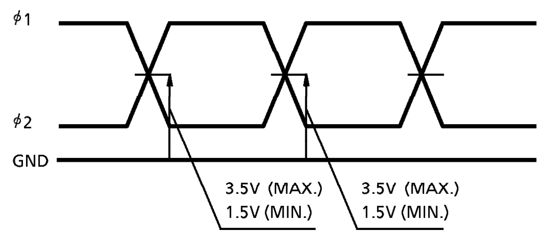
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Pulse Frequency	$f\phi$	—	0.5	2.0	MHz	
Reset Pulse Frequency	$f_{\overline{RS}}$	—	1.0	4.0	MHz	
Sample and Hold Pulse Frequency	$f_{\overline{SP}}$	—	1.0	4.0	MHz	
Clamp Pulse Frequency	$f_{\overline{CP}}$	—	1.0	4.0	MHz	
Clock Capacitance	$C\phi A$	—	350	420	pF	
Final Stage Clock Capacitance	$C\phi B$	—	10	20	pF	
Shift Gate Capacitance	C_{SH}	—	20	40	pF	
Reset Gate Capacitance	$C_{\overline{RS}}$	—	10	20	pF	
Sample and Hold Gate Capacitance	$C_{\overline{SP}}$	—	10	20	pF	
Clamp Gate Capacitance	$C_{\overline{CP}}$	—	10	20	pF	

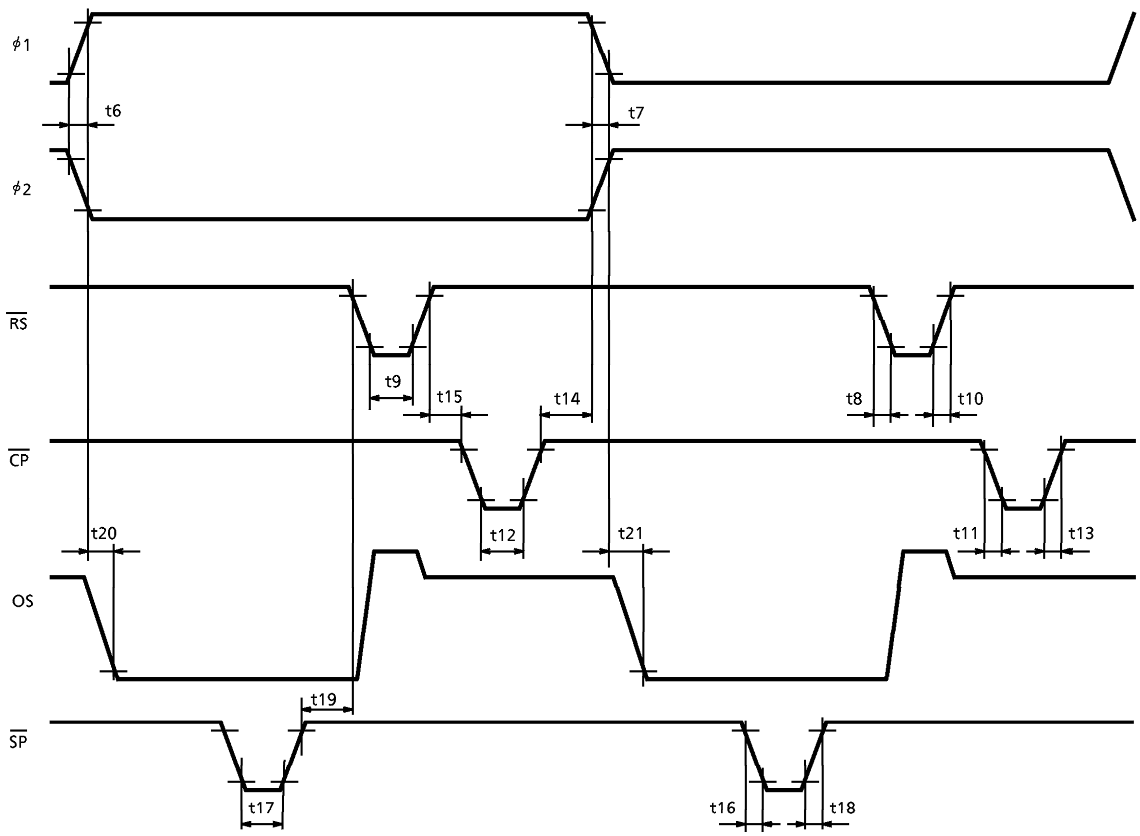
TIMING CHART



TIMING REQUIREMENTS





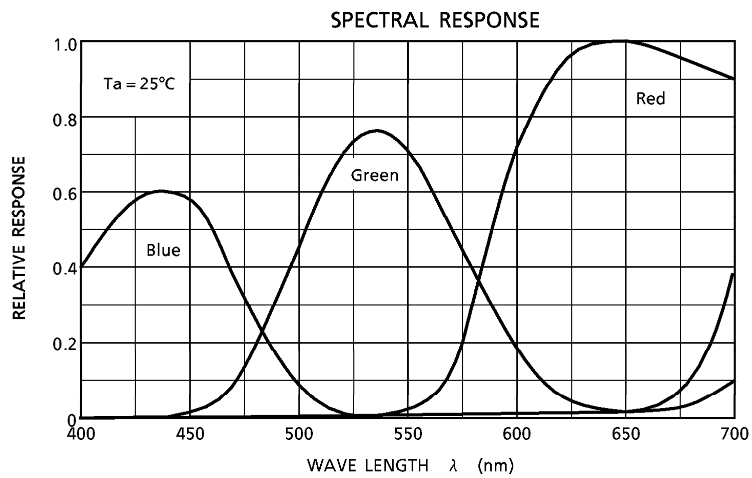


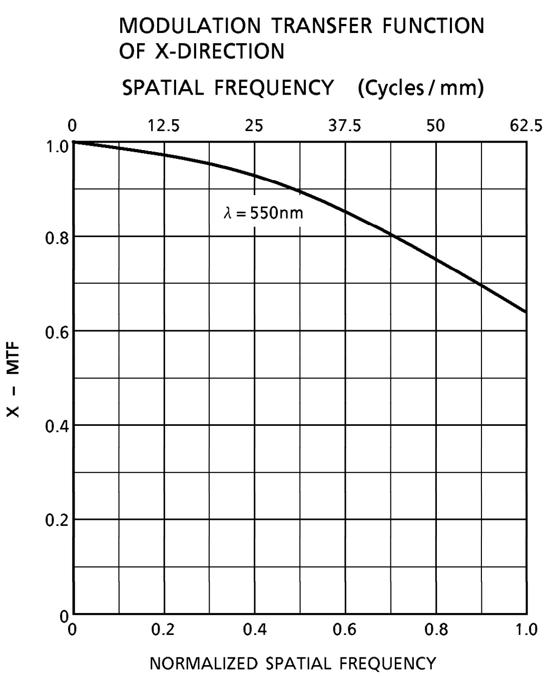
TIMING REQUIREMENTS (Cont'd)

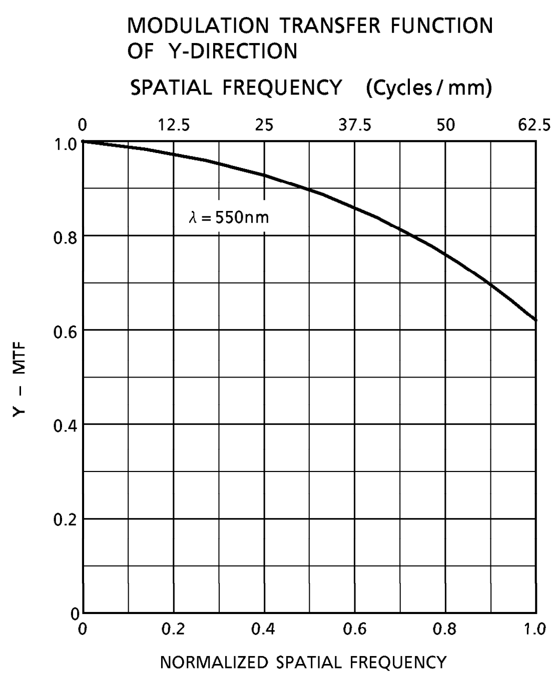
CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 14)	MAX.	UNIT
Pulse Timing of SH and ϕ1A	t1	110	1000	—	ns
	t5	200	1000	—	
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	1000	2000	—	ns
ϕ1, ϕ2 Pulse Rise Time, Fall Time	t6, t7	0	50	—	ns
$\overline{RS}$ Pulse Rise Time, Fall Time	t8, t10	0	20	—	ns
$\overline{RS}$ Pulse Width	t9	45	100	—	ns
$\overline{CP}$ Pulse Rise Time, Fall Time	t11, t13	0	20	—	ns
$\overline{CP}$ Pulse Width	t12	30	100	—	ns
Pulse Timing of ϕ1B, ϕ2B and $\overline{CP}$	t14	20	40	—	ns
Pulse Timing of $\overline{RS}$ and $\overline{CP}$	t15	60	80	—	ns
$\overline{SP}$ Pulse Rise Time, Fall Time	t16, t18	0	20	—	ns
$\overline{SP}$ Pulse Width	t17	45	100	—	ns
Pulse Timing of $\overline{RS}$ and $\overline{SP}$	t19	0	20	100	ns
Video Data Delay Time (Note 15)	t20, t21	—	80	—	ns
Pulse Timing of SH and $\overline{CP}$	t22	0	500	—	ns

(Note 14) TYP. is the case of $f_{\overline{RS}} = 1.0MHz$.
(Note 15) Load Resistance is 100kΩ.

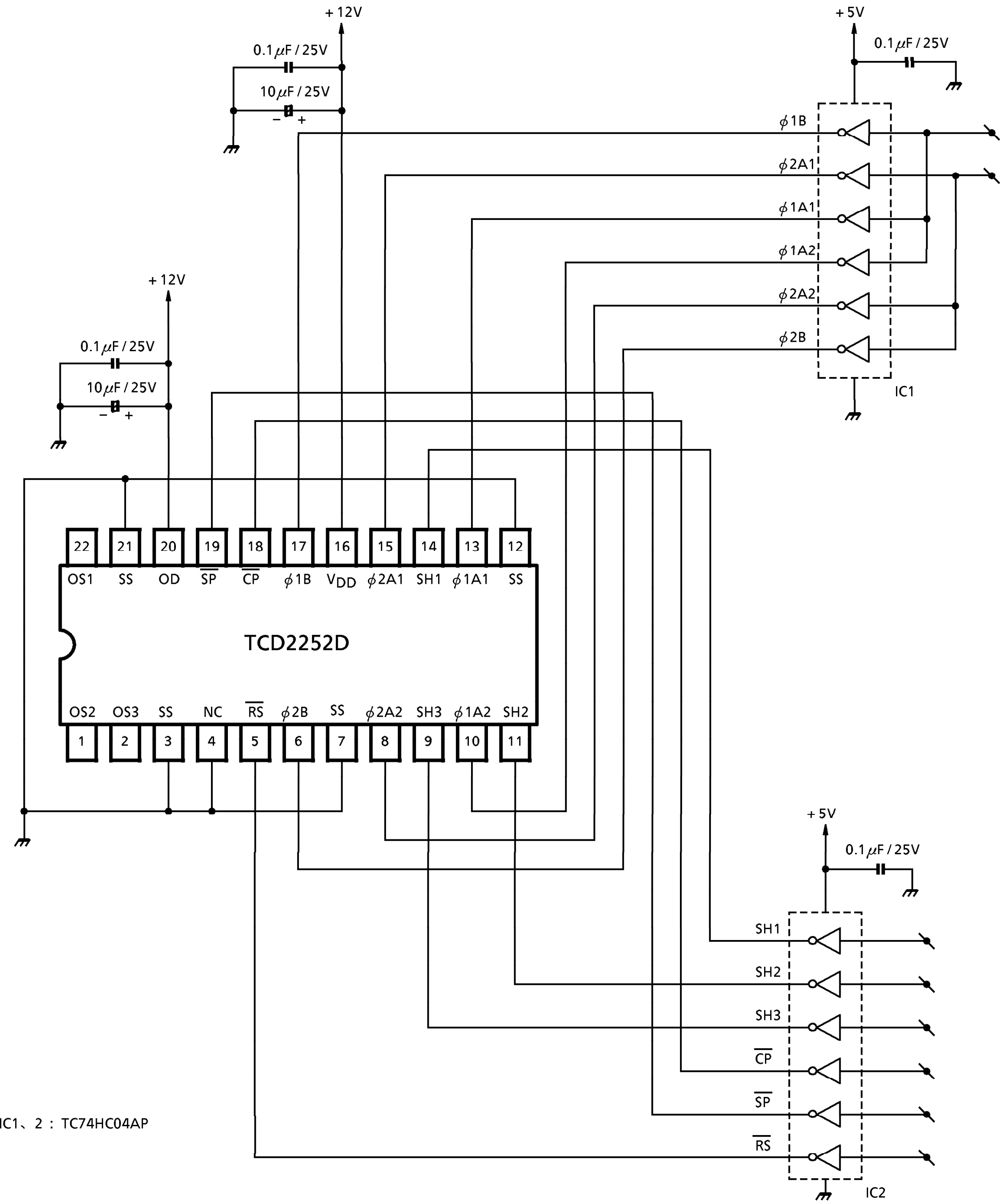
TYPICAL SPECTRAL RESPONSE







TYPICAL DRIVE CIRCUIT



IC1、2 : TC74HC04AP

CAUTION

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N_2.
   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

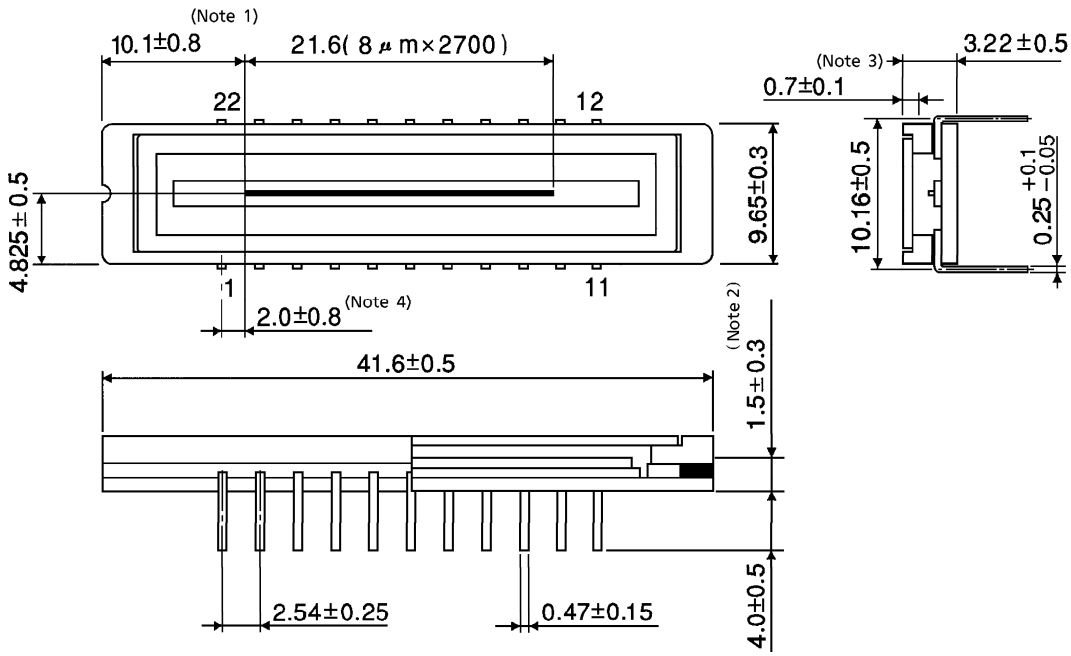
   CCD sensor is sensitive to infrared light.
   Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming
   Since this package is not strong against mechanical stress, you should not reform the lead frame.
   We recommend to use a IC-inserter when you assemble to PCB.

OUTLINE DRAWING

WDIP22-G-400-2.54C

Unit : mm



(Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
(Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note 3) GLASS THICKNES (n = 1.5)
(Note 4) No. 1 SENSOR ELEMENT (S1) TO EDGE OF NO. 1 PIN.

Weight : 4.5g (Typ.)