

32,768 WORD $\times$ 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

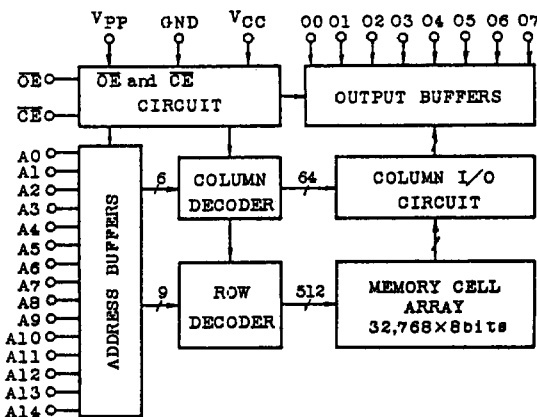
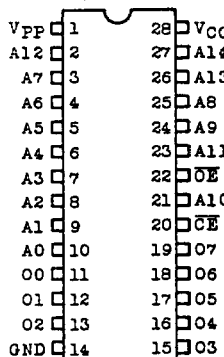
The TC54256AP/AF is a 32,768 word $\times$ 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TC54256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC57256AD's. Once programmed, the TC54256AP/AF cannot be erased because of using plastic DIP without transparent window.

FEATURES

- Peripheral circuit: CMOS
- Memory cell : N-MOS
- Low power dissipation
 - Active : 30mA/6.7MHz
 - Standby: 100 μ A
- Fast access time: 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, TC57256D/AD, One time PROM TMM24256P/AP and TC54256P
- Standard 28 pin DIP plastic package: TC54256AP
- Plastic Flat Package : TC54256AF

BLOCK DIAGRAM

PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A14	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VPP	Program Supply Voltage
VCC	VCC Supply Voltage (+5V)
GND	Ground

MODE SELECTION

	PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	VPP (1)	VCC (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read		L	L	5V	5V	Data Out	Active
Output Deselect	*	H	H			High Impedance	
Standby		H	*			High Impedance	Standby
Program		L	H	12.5V	6V	Data In	Active
Program Inhibit		H	H			High Impedance	
Program Verify	*	L	L			Data Out	

*: H or L

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MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{CC}	V _{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V _{IN}	Input Voltage	-0.6 ~ 7.0	V
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{CC} +0.5	V
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature Time	260 ± 10	°C · sec
T _{STRG}	Storage Temperature	-65 ~ 125	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3	-	0.8	
V _{CC}	V _{CC} Power Supply Voltage	4.75	5.00	5.25	
V _{PP}	V _{PP} Power Supply Voltage	V _{CC} -0.6	V _{CC}	V _{CC} +0.6	

D.C. and OPERATING CHARACTERISTICS (T_a=-40 ~ 85°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0V ~ V _{CC}		-	-	±10	μA
I _{CCO1}	Operating Current	$\overline{CE}$ =0V	f=6.7MHz	-	-	30	mA
I _{CCO2}			f=1MHz	-	-	10	
I _{CCS1}	Standby Current	$\overline{CE}$ =V _{IH}		-	-	1	mA
I _{CCS2}		$\overline{CE}$ =V _{CC} -0.2V		-	-	100	
V _{OH}	Output High Voltage	I _{OH} =-400μA		2.4	-	-	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA		-	-	0.4	V
I _{PP1}	V _{PP} Current	V _{PP} =V _{CC} ±0.6V		-	-	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} =0.4V ~ V _{CC}		-	-	±10	μA

A.C. CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	
t_{OH}	Output Data in Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	

A.C. TEST CONDITIONS

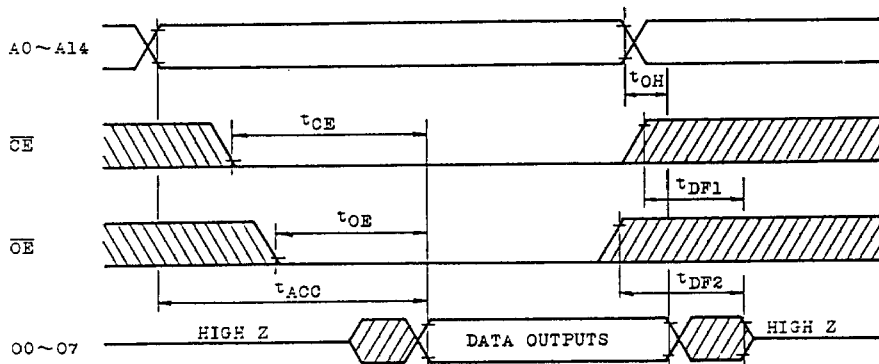
- Output Load : 1 TTL Gate and $C_L = 100\text{pF}$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V $\sim$ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE * ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



TC54256AP/AF

PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	—	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-0.3	—	0.8	
V _{CC}	V _{CC} Power Supply Voltage	5.75	6.0	6.25	
V _{PP}	V _{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Current	V _{IN} =0 ~ V _{CC}	—	—	±10	μA
V _{OH}	Output High Voltage	I _{OH} =-400μA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} =2.1mA	—	—	0.4	V
I _{CC}	V _{CC} Supply Current	—	—	—	40	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} =13.0V	—	—	50	mA
V _{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

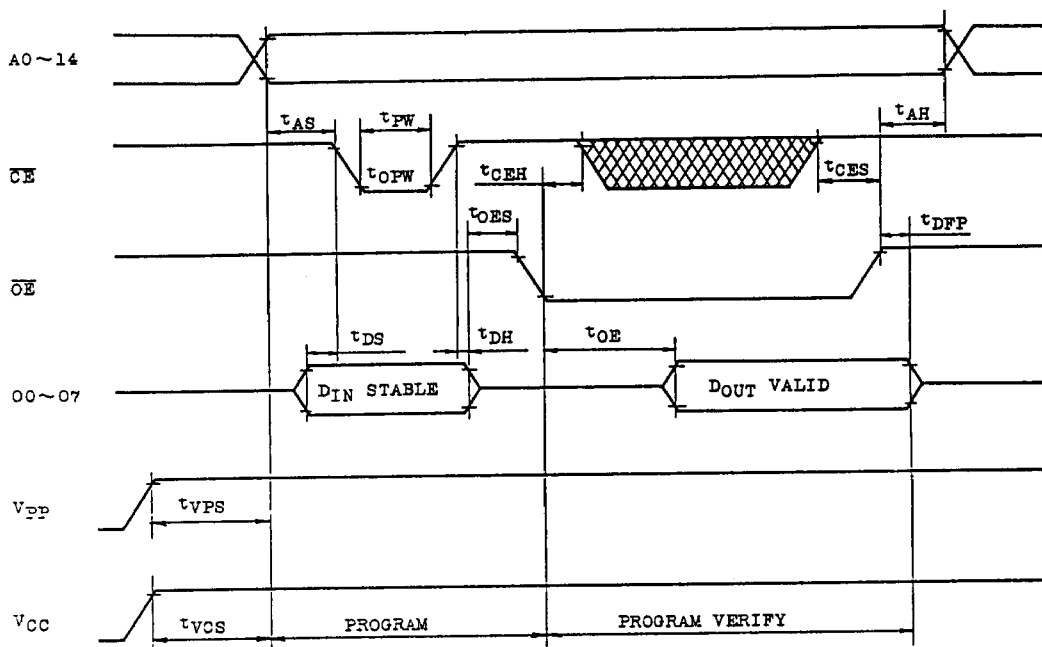
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	—	2	—	—	μs
t _{AH}	Address Hold Time	—	2	—	—	μs
t _{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t _{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t _{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t _{DS}	Data Setup Time	—	2	—	—	μs
t _{DH}	Data Hold Time	—	2	—	—	μs
t _{VPS}	V _{PP} Setup Time	—	2	—	—	μs
t _{VCS}	V _{CC} Setup Time	—	2	—	—	μs
t _{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t _{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t _{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t _{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

 $(V_{CC}=6V\pm0.25V, V_{PP}=12.5V\pm0.5V)$


- Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from socket and setting the device in socket with $V_{PP}=12.5V$ may cause permanent damage to the device.
 3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

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OPERATION INFORMATION

The TC54256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
MODE							
Read Operation ($T_a = -40 \sim 85^\circ\text{C}$)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation ($T_a = 25 \pm 5^\circ\text{C}$)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH} , L; V_{IL} , *: V_{IH} or V_{IL}

READ MODE

The TC54256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) controls the output buffers, independent of device selection. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more TC54256AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC54256AP/AF is placed in the standby mode which reduce the operating current to 100 μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54256AP/AF are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TC54256AP/AF is in the programming mode when the V_{pp} input is at 12.5V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.

The TC54256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL} .

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{pp} terminal, a TTL high level $\overline{CE}$ input inhibits the TC54256AP/AF from being programmed. Programming of two or more TC54256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{pp} terminal with $V_{CC}=6V$.

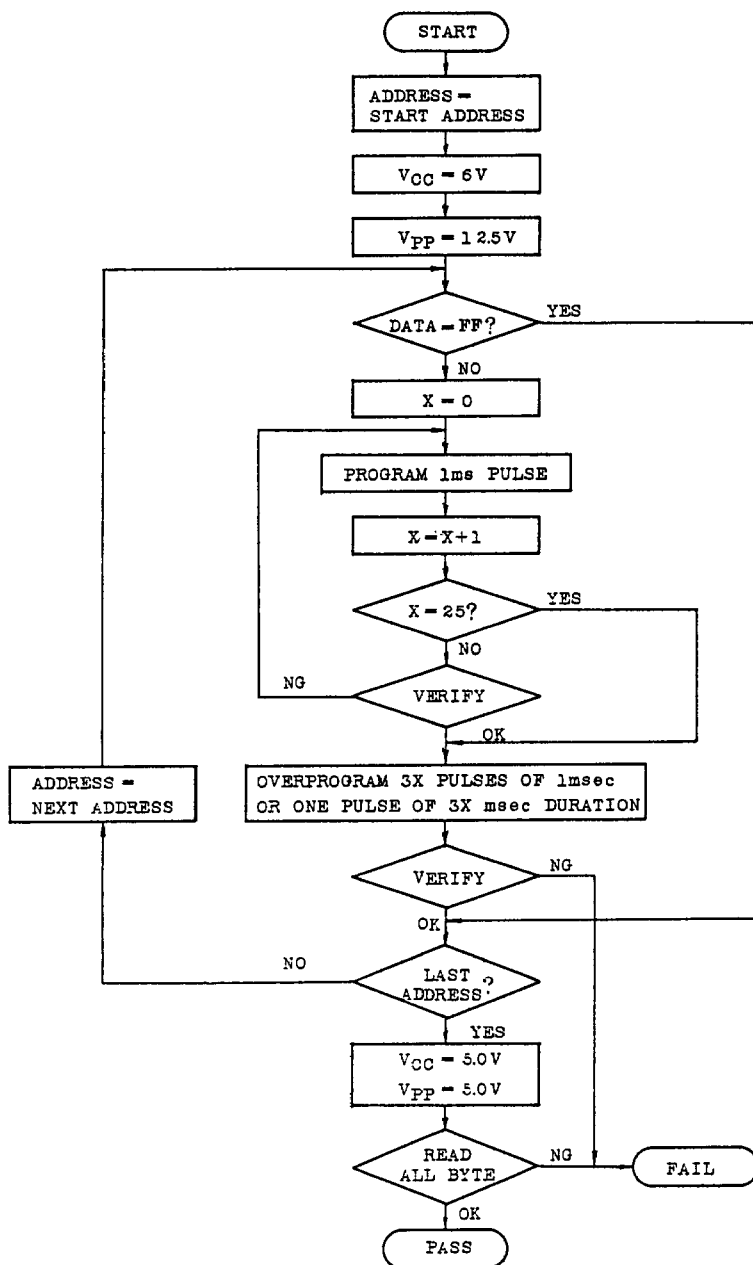
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{pp}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54256AP/AF by using this mode before program operation and automatically set program voltage (V_{pp}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this condition is manufacturer code. Device code is identified when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC54256AP/AF.

SIGNATURE \ PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V $\pm$ 0.5V

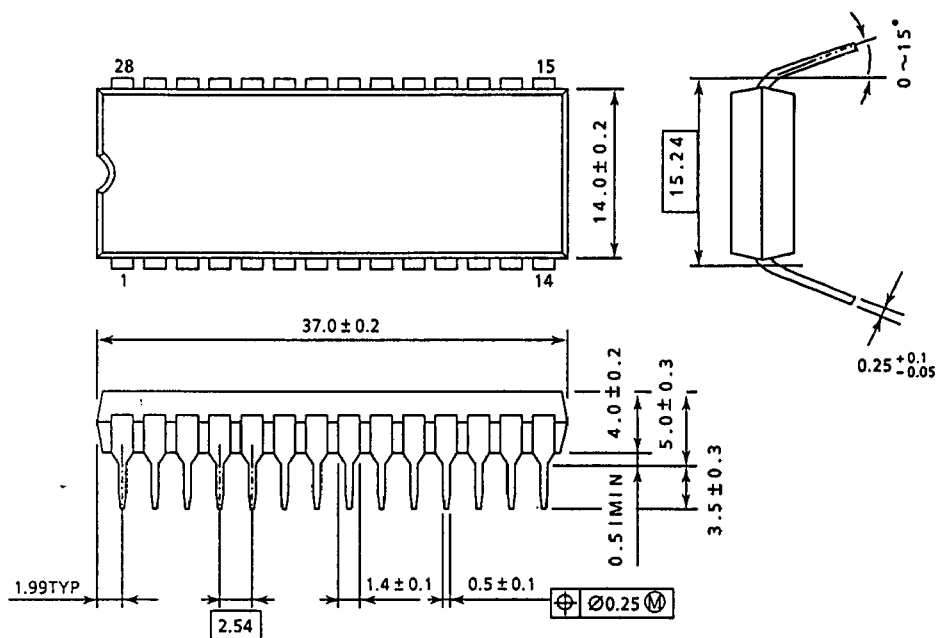
A1 ~ A8, A10 ~ A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}

TC54256AP/AF

OUTLINE DRAWINGS

DIP28-P-600

Unit: mm

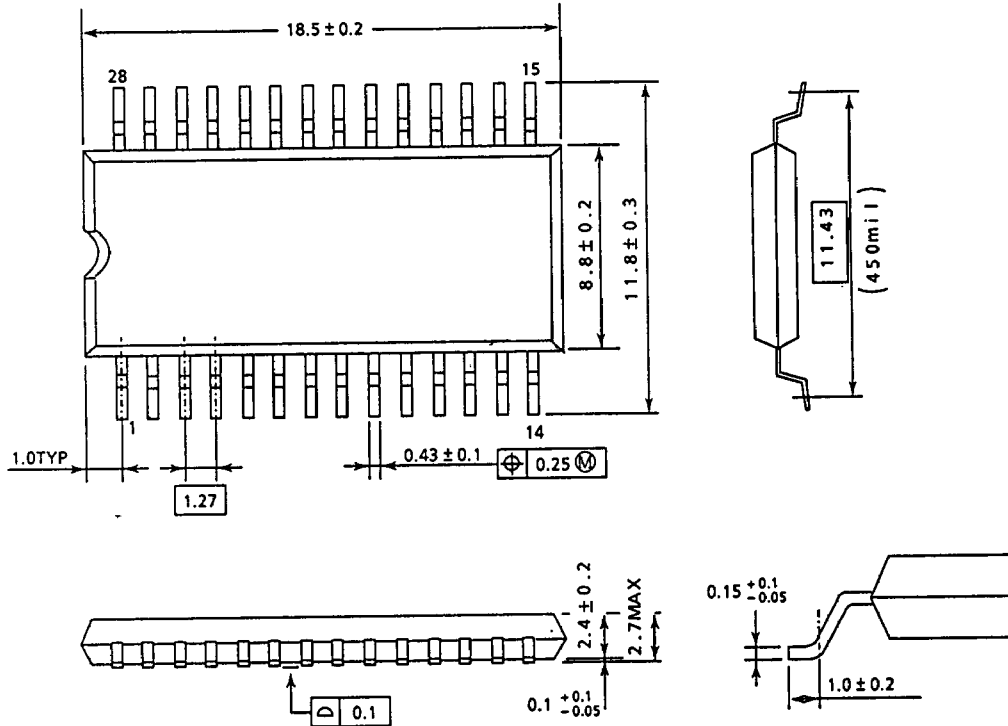


Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

SOP28-P-450

Unit : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.