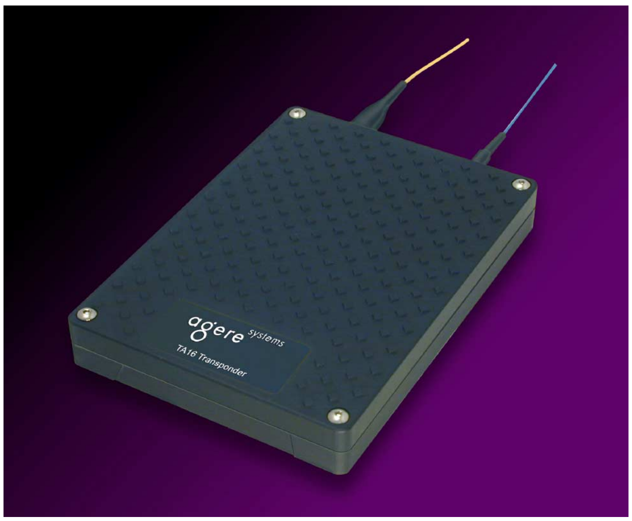
Data Sheet
March 2001

TA16-Type 2.5 Gbits/s Transponder with 16-Channel 155 Mbits/s Multiplexer/Demultiplexer



The TA16-Type transponders integrate up to 15 discrete ICs and optical components, including a 2.5 Gbits/s optical transmitter and receiver pair, all in a single, compact package.

Features

- 2.5 Gbits/s optical transmitter and receiver with 16-channel 155 Mbits/s multiplexer/demultiplexer
- Available with 1.31 µm Fabry-Perot laser transmitter and PIN receiver for intraoffice applications, and 1.31 µm or 1.55 µm DFB laser transmitters and PIN or APD receiver for short-haul to long-haul applications
- Pigtailed low-profile package
- Differential LVPECL data interface
- Operating case temperature range: 0 °C to 65 °C
- Automatic transmitter optical power control
- Laser bias monitor output
- Optical transmitter disable input
- SONET frame-detect enable
- Loss of signal, loss of sync, loss of framing alarms
- Diagnostic loopback capability
- Line loopback operation

Applications

- Telecommunications:
  - — Inter- and intraoffice SONET/SDH
  - — Subscriber loop
  - — Metropolitan area networks
- High-speed data communications

Description

The TA16 transponder performs the parallel-to-serial-to-optical transport and optical transport-to-serial-to-parallel function of the SONET/SDH protocol. The TA16 transmitter performs the bit serialization and optical transmission of SONET/SDH OC-48/STM-16 data that has been formatted into standard SONET/SDH compliant, 16-bit parallel format. The TA16 receiver performs the optical-to-electrical conversion function and is then able to detect frame and byte boundaries and demultiplex the serial data into 16-bit parallel OC-48/STM-16 format.

Note: The TA16 transponder does not perform byte-level multiplexing or interleaving.

Figure 1 shows a simplified block diagram of the TA16-type transponder. This device is a bidirectional module designed to provide a SONET or SDH compliant electro-optical interface between the SONET/SDH photonic physical layer and the electrical section layer. The module contains a 2.5 Gbits/s optical transmitter and a 2.5 Gbits/s optical receiver in the same physical package along with the electronics necessary to multiplex and demultiplex sixteen 155 Mbits/s electrical channels. Clock synthesis and clock recovery circuits are also included within the module.

In the transmit direction, the transponder module multiplexes sixteen 155 Mbits/s LVPECL electrical data signals into an optical signal at 2488.32 Mbits/s for launching into optical fiber. An internal 2.488 GHz reference oscillator is phase-locked to an external 155 MHz data timing reference.

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The optical transmitter is available with either a 1.31 µm Fabry-Perot laser for short-reach applications or 1.31 µm and 1.55 µm DFB lasers for intermediate- to long-reach applications. The optical output signal is SONET and ITU compliant for OC-48/STM-16 applications as shown in Table 4, Optical Characteristics.

In the receive direction, the transponder module receives a 2488.32 Mbits/s optical signal and converts it to an electrical signal, extracts a clock signal, and then demultiplexes the data into sixteen 155 Mbits/s differential LVPECL data signals. The optical receiver is available with either a PIN photodetector or with an APD photodetector. The receiver operates over the wavelength range of 1.1 µm to 1.6 µm and is fully compliant to SONET/SDH OC-48/STM-16 physical layer specifications as shown in Table 5, Optical Characteristics.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect reliability.

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature Range	T_C	0	75	°C
Storage Case Temperature Range	T_S	–40	85	°C
Supply Voltage	—	–0.5	5.5	V
Voltage on Any LVPECL Pin	—	0	V_{CC}	—
High-speed LVPECL Output Source Current	—	—	50	mA
Static Discharge Voltage[1]	ESD	—	500	V
Relative Humidity (noncondensing)	RH	—	85	%
Receiver Optical Input Power—Biased: APD PIN	 P_{IN} P_{IN}	 — —	 0 8	 dBm dBm
Minimum Fiber Bend Radius	—	1.25 (31.8)	—	in. (mm)

1. Human body model.

Block Diagram

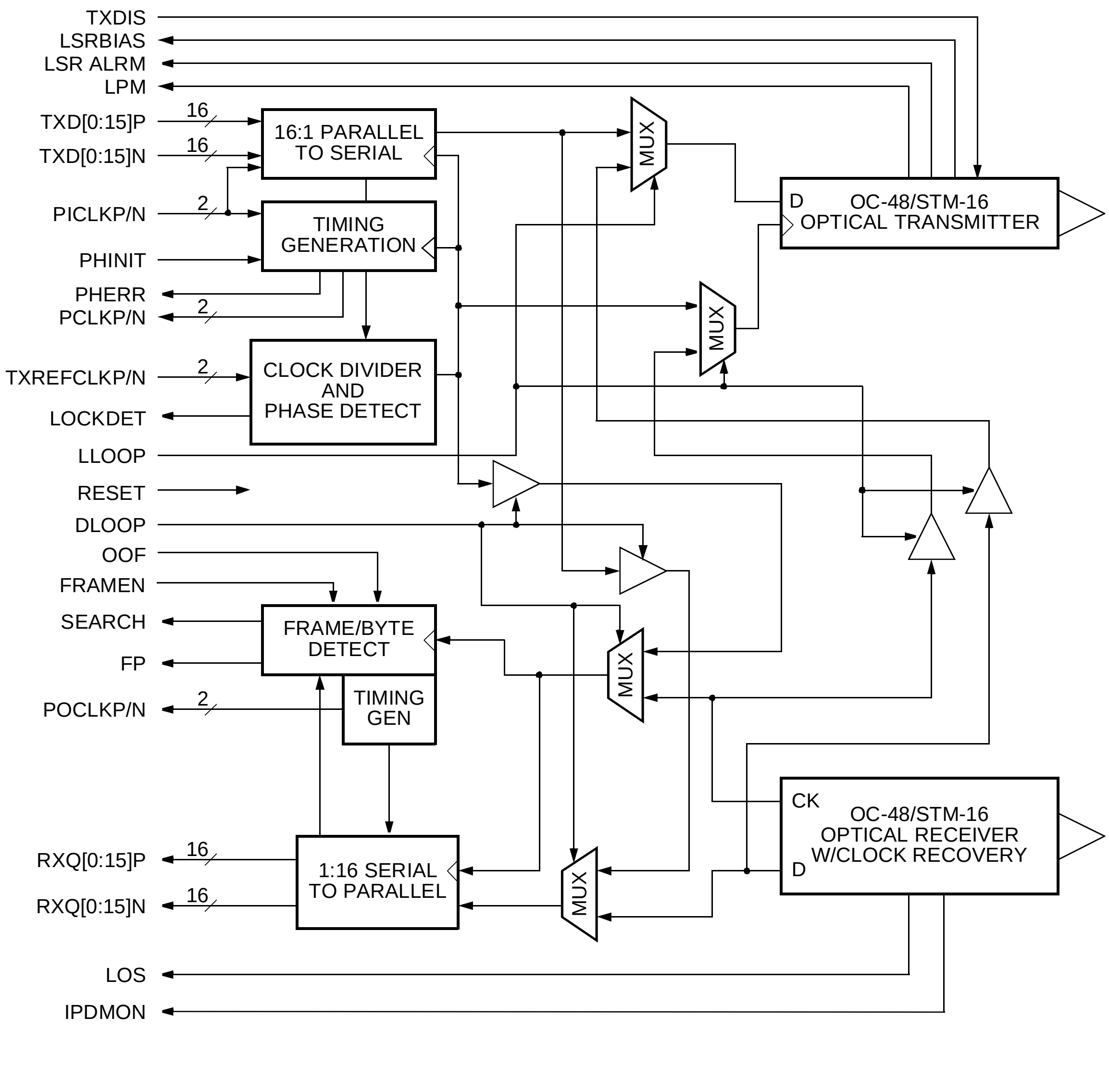

Figure 1. TA16-Type Transponder Block Diagram

Pin Information

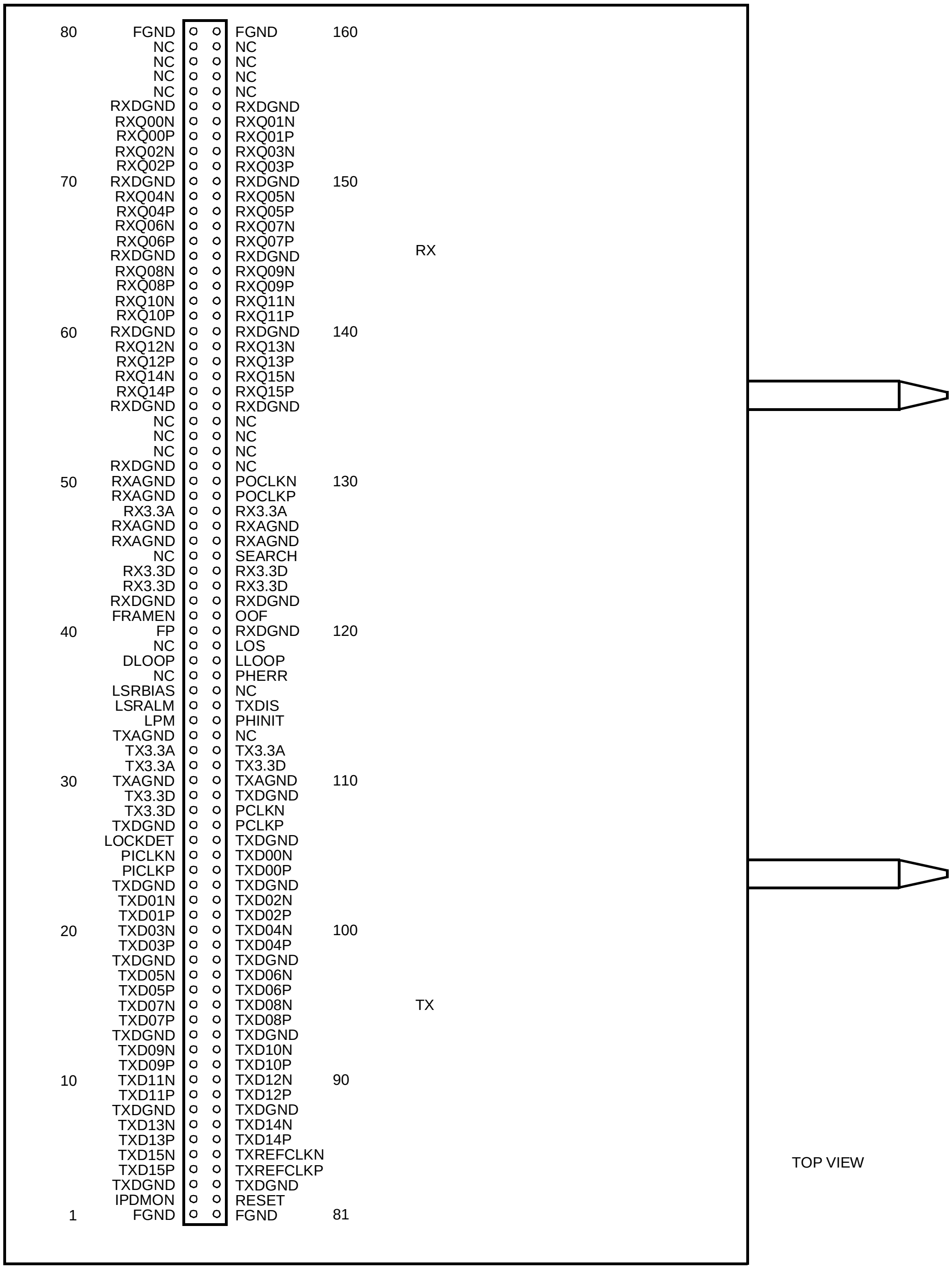

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Figure 2. TA16-Type Transponder Pinout

Pin Descriptions

Table 1. TA16-Type Transponder Pinout

Pin #	Pin Name	I/O	Logic	Description
01	FGND	I	Supply	Frame Ground[1]
02	IPDMON	O	Analog	Receiver Photodiode Current Monitor
03	TxDGND	I	Supply	Transmitter Digital Ground
04	TxD15P	I	LVPECL	Transmitter 155 Mbits/s MSB Data Input
05	TxD15N	I	LVPECL	Transmitter 155 Mbits/s MSB Data Input
06	TxD13P	I	LVPECL	Transmitter 155 Mbits/s Data Input
07	TxD13N	I	LVPECL	Transmitter 155 Mbits/s Data Input
08	TxDGND	I	Supply	Transmitter Digital Ground
09	TxD11P	I	LVPECL	Transmitter 155 Mbits/s Data Input
10	TxD11N	I	LVPECL	Transmitter 155 Mbits/s Data Input
11	TxD09P	I	LVPECL	Transmitter 155 Mbits/s Data Input
12	TxD09N	I	LVPECL	Transmitter 155 Mbits/s Data Input
13	TxDGND	I	Supply	Transmitter Digital Ground
14	TxD07P	I	LVPECL	Transmitter 155 Mbits/s Data Input
15	TxD07N	I	LVPECL	Transmitter 155 Mbits/s Data Input
16	TxD05P	I	LVPECL	Transmitter 155 Mbits/s Data Input
17	TxD05N	I	LVPECL	Transmitter 155 Mbits/s Data Input
18	TxDGND	I	Supply	Transmitter Digital Ground
19	TxD03P	I	LVPECL	Transmitter 155 Mbits/s Data Input
20	TxD03N	I	LVPECL	Transmitter 155 Mbits/s Data Input
21	TxD01P	I	LVPECL	Transmitter 155 Mbits/s Data Input
22	TxD01N	I	LVPECL	Transmitter 155 Mbits/s Data Input
23	TxDGND	I	Supply	Transmitter Digital Ground
24	PICLKP	I	LVPECL	Byte-Aligned Parallel Input Clock at 155 MHz
25	PICLKN	I	LVPECL	Byte-Aligned Parallel Input Clock ar 155 MHz
26	LOCKDET	O	LVTTL	Lock Detect
27	TxDGND	I	Supply	Transmitter Digital Ground
28	Tx3.3D	I	Supply	Transmitter 3.3 V Digital Supply
29	Tx3.3D	I	Supply	Transmitter 3.3 V Digital Supply
30	TxAGND	I	Supply	Transmitter Analog Ground
31	Tx3.3A	I	Supply	Transmitter 3.3 V Analog Supply
32	Tx3.3A	I	Supply	Transmitter 3.3 V Analog Supply
33	TxAGND	I	Supply	Transmitter Analog Ground
34	LPM	O	Analog	Laser Power Monitor
35	LSRALRM	O	Analog	Laser Degrade Alarm
36	LSRBIAS	O	Analog	Transmitter Laser Bias Output
37	NC	—	—	No User Connection Permitted
38	DLOOP	I	LVTTL	Diagnostic Loopback
39	NC	—	—	No User Connection Permitted
40	FP	O	LVPECL	Frame Pulse
41	FRAMEN	I	LVTTL	Frame Enable
42	RxDGND	I	Supply	Receiver Digital Ground

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND).

Pin Descriptions (continued)

Table 1. TA16-Type Transponder Pinout (continued)

Pin #	Pin Name	I/O	Logic	Description
43	Rx3.3D	I	Supply	Receiver 3.3 V Digital Supply
44	Rx3.3D	I	Supply	Receiver 3.3 V Digital Supply
45	NC	—	—	No User Connection Permitted
46	RxAGND	I	Supply	Receiver Analog Ground
47	RxAGND	I	Supply	Receiver Analog Ground
48	Rx3.3A	I	Supply	Receiver 3.3 V Analog Supply
49	RxAGND	I	Supply	Receiver Analog Ground
50	RxAGND	I	Supply	Receiver Analog Ground
51	RxDGND	I	Supply	Receiver Digital Ground
52	NC	—	—	No User Connection Permitted
53	NC	—	—	No User Connection Permitted
54	NC	—	—	No User Connection Permitted
55	RxDGND	I	Supply	Receiver Digital Ground
56	RxQ14P	O	LVPECL	Receiver 155 Mbits/s Data Output
57	RxQ14N	O	LVPECL	Receiver 155 Mbits/s Data Output
58	RxQ12P	O	LVPECL	Receiver 155 Mbits/s Data Output
59	RxQ12N	O	LVPECL	Receiver 155 Mbits/s Data Output
60	RxDGND	I	Supply	Receiver Digital Ground
61	RxQ10P	O	LVPECL	Receiver 155 Mbits/s Data Output
62	RxQ10N	O	LVPECL	Receiver 155 Mbits/s Data Output
63	RxQ08P	O	LVPECL	Receiver 155 Mbits/s Data Output
64	RxQ08N	O	LVPECL	Receiver 155 Mbits/s Data Output
65	RxDGND	I	Supply	Receiver Digital Ground
66	RxQ06P	O	LVPECL	Receiver 155 Mbits/s Data Output
67	RxQ06N	O	LVPECL	Receiver 155 Mbits/s Data Output
68	RxQ04P	O	LVPECL	Receiver 155 Mbits/s Data Output
69	RxQ04N	O	LVPECL	Receiver 155 Mbits/s Data Output
70	RxDGND	I	Supply	Receiver Digital Ground
71	RxQ02P	O	LVPECL	Receiver 155 Mbits/s Data Output
72	RxQ02N	O	LVPECL	Receiver 155 Mbits/s Data Output
73	RxQ00P	O	LVPECL	Receiver 155 Mbits/s LSB Data Output
74	RxQ00N	O	LVPECL	Receiver 155 Mbits/s LSB Data Output
75	RxDGND	I	Supply	Receiver Digital Ground
76	NC	—	—	No User Connection Permitted
77	NC	—	—	No User Connection Permitted
78	NC	—	—	No User Connection Permitted
79	NC	—	—	No User Connection Permitted
80	FGND	I	Supply	Frame Ground[1]
81	FGND	I	Supply	Frame Ground[1]
82	RESET	I	LVTTL	Master Reset
83	TxDGND	I	Supply	Transmitter Digital Ground
84	TxRefClkP	I	LVPECL	Transmitter 155 Mbits/s Reference Clock Input
85	TxRefClkN	I	LVPECL	Transmitter 155 Mbits/s Reference Clock Input

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND).

Pin Descriptions (continued)

Table 1. TA16-Type Transponder Pinout (continued)

Pin #	Pin Name	I/O	Logic	Description
86	TxD14P	I	LVPECL	Transmitter 155 Mbits/s Data Input
87	TxD14N	I	LVPECL	Transmitter 155 Mbits/s Data Input
88	TxDGND	I	SUPPLY	Transmitter Digital Ground
89	TxD12P	I	LVPECL	Transmitter 155 Mbits/s Data Input
90	TxD12N	I	LVPECL	Transmitter 155 Mbits/s Data Input
91	TxD10P	I	LVPECL	Transmitter 155 Mbits/s Data Input
92	TxD10N	I	LVPECL	Transmitter 155 Mbits/s Data Input
93	TxDGND	I	Supply	Transmitter Digital Ground
94	TxD08P	I	LVPECL	Transmitter 155 Mbits/s Data Input
95	TxD08N	I	LVPECL	Transmitter 155 Mbits/s Data Input
96	TxD06P	I	LVPECL	Transmitter 155 Mbits/s Data Input
97	TxD06N	I	LVPECL	Transmitter 155 Mbits/s Data Input
98	TxDGND	I	Supply	Transmitter Digital Ground
99	TxD04P	I	LVPECL	Transmitter 155 Mbits/s Data Input
100	TxD04N	I	LVPECL	Transmitter 155 Mbits/s Data Input
101	TxD02P	I	LVPECL	Transmitter 155 Mbits/s Data Input
102	TxD02N	I	LVPECL	Transmitter 155 Mbits/s Data Input
103	TxDGND	I	Supply	Transmitter Digital Ground
104	TxD00P	I	LVPECL	Transmitter 155 Mbits/s LSB Data Input
105	TxD00N	I	LVPECL	Transmitter 155 Mbits/s LSB Data Input
106	TxDGND	I	Supply	Transmitter Digital Ground
107	PCLKP	O	LVPECL	Transmitter Parallel Reference Clock Output
108	PCLKN	O	LVPECL	Transmitter Parallel Reference Clock Output
109	TxDGND	I	Supply	Transmitter Digital Ground
110	TxAGND	I	Supply	Transmitter Analog Ground
111	Tx3.3D	I	Supply	Transmitter Digital 3.3 V Supply
112	Tx3.3A	I	Supply	Transmitter Analog 3.3 V Supply
113	NC	—	—	No User Connection Permitted
114	PHINIT	I	LVPECL	Phase Initialization
115	TxDIS	I	TTL	Transmitter Disable
116	NC	—	—	No User Connection Permitted
117	PHERR	O	LVPECL	Phase Error
118	LLOOP	I	LVTTL	Line Loopback (active-low)
119	LOS	O	LVTTL	Loss of Signal
120	RxDGND	I	Supply	Receiver Digital Ground
121	OOF	I	LVTTL	Out of Frame (enable frame detection)
122	RxDGND	I	Supply	Receiver Digital Ground
123	Rx3.3D	I	Supply	Receiver Digital 3.3 V Supply
124	Rx3.3D	I	Supply	Receiver Digital 3.3 V Supply
125	SEARCH	O	LVTTL	Frame Search Output
126	RxAGND	I	Supply	Receiver Analog Ground
127	RxAGND	I	Supply	Receiver Analog Ground
128	Rx3.3A	I	Supply	Receiver Analog 3.3 V Supply

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND).

Pin Descriptions (continued)

Table 1. TA16-Type Transponder Pinout (continued)

Pin #	Pin Name	I/O	Logic	Description
129	POCLKP	O	LVPECL	Byte-Aligned Parallel Output Clock at 155 MHz
130	POCLKN	O	LVPECL	Byte-Aligned Parallel Output Clock at 155 MHz
131	NC	—	—	No User Connection Permitted
132	NC	—	—	No User Connection Permitted
133	NC	—	—	No User Connection Permitted
134	NC	—	—	No User Connection Permitted
135	RxDGND	I	Supply	Receiver Digital Ground
136	RxQ15P	O	LVPECL	Receiver MSB 155 Mbits/s Data Output
137	RxQ15N	O	LVPECL	Receiver MSB 155 Mbits/s Data Output
138	RxQ13P	O	LVPECL	Receiver 155 Mbits/s Data Output
139	RxQ13N	O	LVPECL	Receiver 155 Mbits/s Data Output
140	RxDGND	I	Supply	Receiver Digital Ground
141	RxQ11P	O	LVPECL	Receiver 155 Mbits/s Data Output
142	RxQ11N	O	LVPECL	Receiver 155 Mbits/s Data Output
143	RxQ09P	O	LVPECL	Receiver 155 Mbits/s Data Output
144	RxQ09N	O	LVPECL	Receiver 155 Mbits/s Data Output
145	RxDGND	I	Supply	Receiver Digital Ground
146	RxQ07P	O	LVPECL	Receiver 155 Mbits/s Data Output
147	RxQ07N	O	LVPECL	Receiver 155 Mbits/s Data Output
148	RxQ05P	O	LVPECL	Receiver 155 Mbits/s Data Output
149	RxQ05N	O	LVPECL	Receiver 155 Mbits/s Data Output
150	RxDGND	I	Supply	Receiver Digital Ground
151	RxQ03P	O	LVPECL	Receiver 155 Mbits/s Data Output
152	RxQ03N	O	LVPECL	Receiver 155 Mbits/s Data Output
153	RxQ01P	O	LVPECL	Receiver 155 Mbits/s Data Output
154	RxQ01N	O	LVPECL	Receiver 155 Mbits/s Data Output
155	RxDGND	I	Supply	Receiver Digital Ground
156	NC	—	—	No User Connection Permitted
157	NC	—	—	No User Connection Permitted
158	NC	—	—	No User Connection Permitted
159	NC	—	—	No User Connection Permitted
160	FGND	I	Supply	Frame Ground[1]

1. Frame ground is connected to the housing and is isolated from all circuit grounds (TxDGND, TxAGND, RxDGND, RxAGND).

Pin Descriptions (continued)

Table 2. TA16-Type Transponder Input Pin Descriptions

Pin Name	Pin Description
TxD[0:15]P TxD[0:15]N	**16-bit Differential LVPECL Parallel Input Data Bus**. TxD15P/N is the most significant bit of the input word and is the first bit serialized. TxD00P/N is the least significant bit of the input word and is the last bit serialized. TxD[0:15]P/N is sampled on the rising edge of PICLK.
PICLKP PICLKN	**Differential LVPECL Parallel Input Clock**. A 155 MHz nominally 50% duty cycle input clock to which TxD[0:15]P/N is aligned. The rising edge of PICLK transfers the data on the 16 TxD inputs into the holding register of the parallel-to-serial converter.
TxREFCLKP TxREFCLKN	**Differential LVPECL Low Jitter 155.520 MHz Input Reference Clock**. This input is used as the reference for the internal clock frequency synthesizer which generates the 2.5 GHz bit rate clock used to shift data out of the parallel-to-serial converter and also for the byte-rate clock, which transfers the 16-bit parallel input data from the input holding register into the parallel-to-serial shift register. Input is internally terminated and biased. See discussion on interfacing, page 13.
TxDIS	**Transmitter Disable Input**. A logic HIGH on this input pin shuts off the transmitter's laser so that there is no optical output.
DLOOP	**Diagnostic Loopback Enable (LVTTL)**. When the DLOOP input is low, the 2.5 Gbits/s serial data stream from the parallel-to-serial converter is looped back internally to the serial-to-parallel converter along with an internally generated bit synchronous serial clock. The received serial data path from the optical receiver is disabled.
LLOOP	**Line Loopback Enable (LVTTL)**. When LLOOP is low, the 2.5 Gbits/s serial data and recovered clock from the optical receiver are looped directly back to the optical transmitter. The multiplexed serial data from the parallel-to-serial converter is ignored.
PHINIT	**Phase Initialization (LVPECL)**. A rising edge on this input will realign the internal timing associated with clocking data into and out of the internal FIFO. For a detailed explanation, see the section on Transmitter Data Input Timing on page 17.
FRAMEN	**Frame Enable Input (LVTTL)**. Enables the frame detection circuitry to detect A1 A2 byte alignment and to lock to a word boundary. The TA16 transponder will continually perform frame acquisition as long as FRAMEN is held high. When this input is low, the frame-detection circuitry is disabled. Frame-detection process is initiated by rising edge of out-of-frame pulse.
OOF	**Out of Frame (LVTTL)**. This input indicator is typically generated by external SONET/SDH overhead monitor circuitry in response to a state in which the frame boundaries of the received SONET/SDH signal are unknown, i.e., after system reset or loss of synchronization. The rising edge of the OOF input initiates the frame detection function if FRAMEN is high. The FP output goes high when the frame boundary is detected in the incoming serial data stream from the optical receiver.
RESET	**Master Reset (LVTTL)**. Reset input for the multiplexer/demultiplexer. A low on this input clears all buffers and registers. During reset, POCLK and PCLK do not toggle.

Pin Descriptions (continued)

Table 3. TA16-Type Transponder Output Pin Descriptions

Pin Name	Pin Description
RxQ[0:15]P RxQ[0:15]N	**16-bit Differential LVPECL Parallel Output Data Bus**. RxQ[0:15] is the 155 Mbyte/s 16-bit output word. RxQ15P/N is the most significant bit of the received word and is the first bit serialized. RxQ00P/N is the least significant bit of the received word and is the last bit serialized. RxQ[0:15]P/N is updated on the falling edge of POCLk.
POCLKP POCLKN	**Differential LVPECL Parallel Output Clock**. A 155 MHz nominally 50% duty cycle, byte rate output clock that is aligned to the RxQ[0:15] byte serial output data. RxQ[0:15] and FP are updated on the falling edge of POCLK.
FP	**Frame Pulse (LVPECL).** Indicates frame boundaries in the received serial data stream. If framing pattern detection is enabled (FRAMEN high and OOF), FP pulses high for one POCLK cycle when a 32-bit sequence matching the framing pattern is detected in the received serial data. FP is updated on the falling edge of POCLK.
SEARCH	**A1 A2 Frame Search Output (LVTTL)**. A high on this output pin indicates that the frame detection circuit is active and is searching for a new A1 A2 byte alignment. This output will be high during the entire A1 A2 frame search. Once a new alignment is found, this signal will remain high for a minimum of one 155 MHz clock period beyond the third A2 byte before it will be set low.
LOS	**Loss of Signal (LVTTL)**. A low on this output indicates a loss of lock by the clock recovery circuit in the optical receiver.
LSRBIAS	**Laser Bias (Analog)**. Provides an indication of the health of the laser in the transmitter. This output changes at the rate of 20 mV/mA of bias current. If this output voltage reaches 1.4 V (70 mA of bias), the automatic power control circuit is struggling to maintain output power. This may indicate that the transmitter has reached an end-of-life condition.
LSRALRM	**Laser Degrade Alarm (5 V CMOS).** A logic low on this output indicates that the transmitter's automatic power control circuits are unable to maintain the nominal output power. This output becomes active when the optical output power degrades 2 dB below the nominal operating power.
LPM	**Laser Power Monitor (Analog)**. Provides an indication of the output power level from the transmitter laser. This output is set at 500 mV for the nominal transmitter optical output power. If the optical power decreases by 3 dB, this output will drop to approximately 250 mV, and if the output power should increase by 3 dB, this output will increase to 1000 mV.
PCLKP/N	**Parallel Byte Clock (Differential LVPECL)**. A byte-rate reference clock generated by dividing the internal 2.488 GHz serial bit clock by 16. This output is normally used to synchronize byte-wide transfers from upstream logic into the TA16 transponder. See timing discussion for additional details, page 17.
PHERR	**Phase Error Signal (Single-Ended LVPECL)**. This signal pulses high during each PCLK cycle for which there is potential setup/hold timing violations between the internal byte clock and the PICLK timing domains. PHERR is updated on the falling edge of the PICLK output. For a detailed explanation, see the section on Transmitter Data Input Timing on page 17.
IDPMON	**Receiver Photodiode Current Monitor (Analog)**. This output provides a current output that is a mirror of the photocurrent generated by the optical receiver's photodiode (APD or PIN).
LOCKDET	**Lock Detect (LVTTL).** This output goes low after the transmit side PLL has locked to the clock signal provided at the TXREFCLK input pins. LOCKDET is an asynchronous output.

Functional Description

Receiver

The optical receiver in the TA16-type transponder is optimized for the particular SDH/SONET application segment in which it was designed to operate and will have either an APD or PIN photodetector. The detected serial data output of the optical receiver is connected to a clock and data recovery circuit (CDR), which extracts a 2488.32 MHz clock signal. This recovered serial bit clock signal and a retimed serial data signal are presented to the 16-bit serial-to-parallel converter and to the frame and byte detection logic.

The serial-to-parallel converter consists of three 16-bit registers. The first is a serial-in parallel-out shift register, which performs serial-to-parallel conversion. The second is an internal 16-bit holding register, which transfers data from the serial-to-parallel register on byte boundaries as determined by the frame and byte detection logic. On the falling edge of the free-running POCLK signal, the data in the holding register is transferred to the output holding register where it becomes available as RxQ[0:15].

The frame and byte boundary detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by an A2 byte. Framing pattern detection is enabled and disabled by the FRAMEN input. The frame detection process is started by a rising edge on OOF while FRAMEN is active (FRAMEN= high). It is disabled when a framing pattern is detected. When framing pattern detection is enabled (FRAMEN = high), the framing pattern is used to locate byte and frame boundaries in the incoming serial data stream from the CDR circuits. During this time, the parallel output data bus (RxQ[0:15]) will not contain valid data. The timing generator circuitry takes the located byte boundary and uses it to block the incoming serial data stream into bytes for output on the parallel output data bus (RxQ[0:15]). The frame boundary is reported on the framing pulse (FP) output when any 32-bit pattern matching the framing pattern is detected in the incoming serial data stream. When framing detection is disabled (FRAMEN = low), the byte boundary is fixed at the location found when frame detection was previously enabled.

Transmitter

The optical transmitter in the TA16-type transponder is optimized for the particular SDH/SONET segment in which it is designed to operate. The transmitter will have either a Fabry-Perot or a DFB laser as the optical element and can operate at either 1310 nm or 1550 nm. The transmitter is driven by a serial data stream developed in the parallel-to-serial conversion logic and by a 2488.32 MHz serial bit clock signal synthesized from the 155.52 MHz TxREFCLK input.

The parallel-to-serial converter block shown in Figure 1 is comprised of two byte-wide registers. The first register latches the 16 bits of parallel input data (TxD[0:15]) on the rising edge of PICLK. The second register is a 16-bit parallel-load serial-out shift register that is loaded from the input register. An internally generated byte clock, which is phase aligned to the 2488.32 MHz serial transmit clock, activates the data transfer between the input register and the parallel-to-serial register.

The clock divider and phase detect circuitry shown in Figure 1 generates internal reference clocks and timing functions for the transmitter. Therefore, it is important that the TxREFCLK input is generated from a precise and stable source. To prevent internal timing signals from producing jitter in the transmitted serial data that exceeds the SDH/SONET jitter generation requirements of 0.01 UI, it is required that the TxREFCLK input be generated from a crystal oscillator or other source having a frequency accuracy better than 20 ppm. In order to meet the SDH/SONET requirement, the reference clock jitter must be guaranteed to be less than 1 ps rms over the 12 kHz to 20 MHz bandwidth. When used in SONET network applications, this input clock must be derived from a source that is synchronized to the primary reference clock (stratum 1 clock).

The timing generation circuitry provides two separate functions. It develops a byte rate clock that is synchronized to the 2488.32 MHz transmit serial clock, and it provides a mechanism for aligning the phase between the incoming byte clock (PICLK) and the clock which loads the parallel data from the input register into the parallel-to-serial shift register. The PCLK output is a byte rate (155 MHz) version of the serial transmit clock and is intended for use by upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the parallel data coming into the transmitter and the subsequent parallel-to-serial timing functions. The timing generator also provides a feedback reference clock to the phase detector for use by the transmit serial clock synthesizer (for additional discussions, see transmitter input options, page 17.)

Functional Description (continued)

Loopback Modes

The TA16 transponder is capable of operating in either of two loopback modes: diagnostic loopback or line loopback.

Line Loopback

When LLOOP is pulled low, the received serial data stream and recovered 2488.32 MHz serial clock from the optical receiver are connected directly to the serial data and clock inputs of the optical transmitter. This establishes a receive-to-transmit loopback at the serial line rate.

Diagnostic Loopback

When DLOOP is pulled low, a loopback path is established from the transmitter to the receiver. In this mode, the serial data from the parallel-to-serial converter and the transmit serial clock are looped back to the serial-to-parallel converter and the frame and byte detect circuitry, respectively.

Transponder Interfacing

The TxD[0:15]P/N and PICLKP/N inputs and the RxQ[0:15]P/N, POCLKP/N, and PCLKP/N outputs are high-speed (155 Mbits/s), LVPECL differential data and clock signals. To maintain optimum signal fidelity, these inputs and outputs must be connected to their terminating devices via 50 Ω controlled-impedance transmission lines. The transmitter inputs (TxD[0:15]P/N, TxREFCLKP/N, and PICLKP/N) must be terminated as close as possible to theTA16 transponder connector with a Thevenin equivalent impedance equal to 50 ¾ terminated to Vcc – 2V. The receiver outputs (RxQ[0:15]P/N, POCLKP/N, and PCLKP/N) must be terminated as close as possible to the device (IC) that these signals interface to with a Thevenin equivalent impedance equal to 50 Ω terminated to Vcc – 2 V.

Figure 3, below, shows one example of the proper terminations. Other methods may be used, provided they meet the requirements stated above.

TxREFCLKP/N. The reference clock input is different than the TxD and PICLK inputs because it is internally terminated, ac-coupled, and self-biased. Therefore, it must be treated somewhat differently than the TxD and PICLK inputs. Figure 14 shows the proper method for connecting the TxREFCLK input.

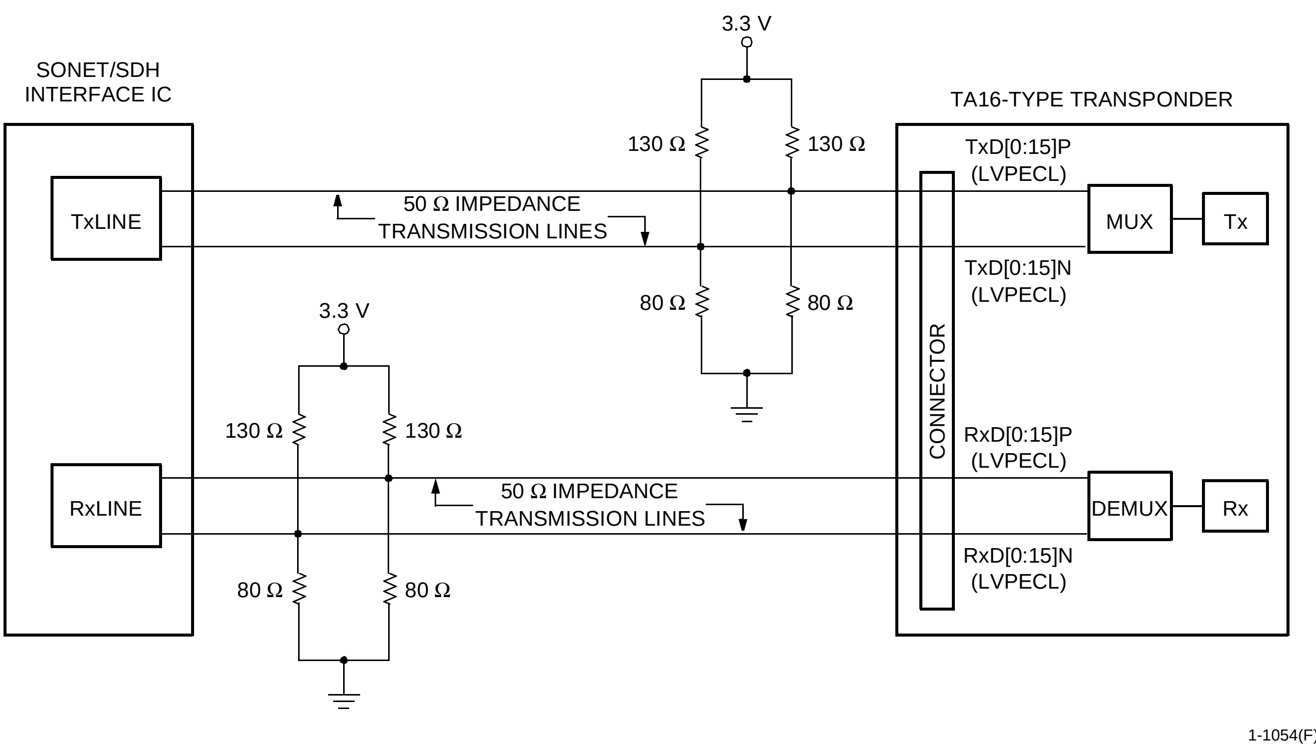


Figure 3. Transponder Interfacing

Optical Characteristics

Minimum and maximum values specified over operating case temperature range at 50% duty cycle data signal. Typical values are measured at room temperature unless otherwise noted.

Table 4. OC48/STM-16 Transmitter Optical Characteristics (T_C = 0 °C to 65 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Average Output Power: [1]					
Intraoffice (F-P laser)	P_O	–10	–5	–3	dBm
Short Haul (DFB laser)	P_O	–5	–2	0	dBm
Long Haul:					
1.3 µm DFB Laser	P_O	–2	0	2	dBm
1.55 µm DFB Laser	P_O	–2	0	3	dBm
Operating Wavelength:					
Intraoffice (F-P laser)	λ	1270	—	1360	nm
Short Haul (DFB laser)	λ	1270	—	1360	nm
Long Haul (1.3 µm DFB laser)	λ	1280	—	1335	nm
Long Haul (1.55 µm DFB laser)	λ	1500	—	1580	nm
Spectral Width:					
Intraoffice (F-P laser)	$\Delta\lambda_{rms}$	—	—	4	nm
Short Haul and Long Haul (DFB laser) [2]	$\Delta\lambda_{20}$	—	—	1	nm
Side-mode Suppression Ratio (DFB laser) [3]	SSR	30	—	—	dB
Extinction Ratio[4]	r_e	8.2	—	—	dB
Optical Rise and Fall Times	t_R, t_F	—	—	200	ps
Eye Mask of Optical Output [5, 6]	Compliant with GR-253 and ITU-T G.957				
Jitter Generation	Compliant with GR-253 and ITU-T G.958				

1. Output power definitions and measurements per ITU-T Recommendation G.957.
2. Full spectral width measured 20 dB down from the central wavelength peak under fully modulated conditions.
3. Ratio of the average output power in the dominant longitudinal mode to the power in the most significant side mode under fully modulated conditions.
4. Ratio of logic 1 output power to logic 0 output power under fully modulated conditions.
5. GR-253-CORE, *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria.*
6. ITU-T Recommendation G.957, *Optical Interfaces for Equipment and Systems Relating to the Synchronous Digital Hierarchy.*

Table 5. OC48/STM-16 Receiver Optical Characteristics (T_C = 0 °C to 65 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Average Receiver Sensitivity[1]:					
PIN Receiver (intraoffice, short haul)	P_{RMIN}	–20	–25	—	dBm
APD Receiver (long haul)	P_{RMIN}	–29	–34	—	dBm
Maximum Optical Power:					
PIN Receiver	P_{RMAX}	1	—	—	dBm
APD Receiver (long reach)	RMAX	–6	—	—	dBm
Link Status Switching Threshold Decreasing Light Input:					
APD	LSTD	—	TBD	—	dBm
PIN	LSTD	—	TBD	—	dBm
Link Status Response Time	—	3	—	100	µs
Optical Path Penalty (1310 nm/1550 nm)	—	—	—	1/2	dB
Receiver Reflectance	—	—	—	–27	dB
Jitter Tolerance and JitterTransfer	Compliant with GR-253 and ITU-T G.958				

1. At 1310 nm, 1 x 10^{-10} BER, 2^{23} – 1 pseudorandom data input.

Electrical Characteristics

Table 6. Transmitter Electrical I/O Characteristics (T_C = 0 °C to 65 °C, V_{CC} = 3.3 V ± 5%)

Parameter	Symbol	Logic	Min	Typ	Max	Unit
Parallel Input Clock	PICLKP/N	Diff. LVPECL	153.90	155.52	157.00	MHz
Parallel Clock in Duty Cycle	—	—	40	—	60	%
Reference Clock Frequency Tolerance	TxREFCLKP/N	Diff. LVPECL	–20	—	20	ppm
Reference Clock Jitter (in 12 KHz to 20 MHz band)	—	—	—	—	1	ps rms
Reference Clock Input Duty Cycle	—	—	45	—	55	%
Reference Clock Rise and Fall Times[1]	—	—	—	—	1.5	ns
Reference Clock Signal Levels:[2]		Diff. LVPECL				
Diff. Input Voltage Swing	ΔV_{INDIFF}		300	—	1200	mV
Single-ended Input Voltage Swing	$\Delta V_{INSINGLE}$		150	—	600	mV
Differential Input Resistance	R_{DIFF}		80	100	120	Ω
Input Data Signal Levels:	TxD[0:15]P/N	Diff. LVPECL				
Input High, V_{IH}			V_{CC} – 1.2	—	V_{CC} – 0.3	V
Input Low, V_{IL}			V_{CC} – 2.0	—	V_{CC} – 1.5	V
Input Voltage Swing, ΔV_{IN}			300	—	—	mV
Transmitter Disable Input[3]	TxDIS	TTL (5 V)	2.0	—	5.5	V
Transmitter Enable Input[3]	TxEN	TTL (5 V)	0	—	0.8	V
Laser Bias Voltage Output[4]	LSRBIAS	Analog	0	200	1600	mV
Laser Power Monitor Output[5]	LPM	Analog	35	500	1000	mV
Laser Degrade Alarm:	LSRALM	5 V CMOS				
Output High, V_{OH}			4.5	—	5.2	V
Output Low, V_{OL}			0	—	0.4	V
Phase Initialization:	PHINIT	Single-Ended LVPECL				
Input High, V_{IH}			V_{CC} – 1.0	—	V_{CC} – 0.57	V
Input Low, V_{IL}			V_{CC} – 2.3	—	V_{CC} – 1.44	V
Phase Error[6]:	PHERR	Single-Ended LVPECL				
Output High, V_{OH}			V_{CC} – 1.2	—	V_{CC} – 0.65	V
Output Low, V_{OL}			V_{CC} – 2.2	—	V_{CC} – 1.5	V
Line Loopback Enable:	LLOOP	LVTTL				
Active-Low:						
Input High, V_{IH}			2.0	—	V_{CC} + 1.0	V
Input Low, V_{IL}			0	—	0.8	V

1. 20% to 80%.
2. Internally biased and ac-coupled. See Figure 13.
3. The transmitter is normally enabled and only requires an external voltage to disable.
4. Output conversion factor is 20 mV/mA of laser bias current.
5. Set at 500 mV at nominal output power; will track P_O linearly (–3 dB = 250 mV, +3 dB = 1000 mV).
6. Terminated into 220 Ω to GND with 100 Ω line-to-line.

Electrical Characteristics (continued)

Table 6. Transmitter Electrical I/O Characteristics (T_C = 0 °C to 65 °C, V_{CC} = 3.3 V ± 5%) (continued)

Diagnostic Loopback Enable: Active-Low: Input High, V_{IH} Input Low, V_{IL}	DLOOP	LVTTL	 2.0 0	 — —	 V_{CC} + 1.0 0.8	 V V
Parallel Output Clock:[6] Output High, V_{OH} Output Low, V_{OL} S-E Output Voltage Swing, ΔV_{SINGLE} Diff. Voltage Swing, ΔV_{DIFF}	PCLKP/N	Diff. LVPECL	 V_{CC} – 1.15 V_{CC} – 1.95 400 800	 — — — —	 V_{CC} – 0.6 V_{CC} – 1.45 950 1900	 V V mV mV

1. 20% to 80%.
2. Internally biased and ac-coupled. See Figure 13.
3. The transmitter is normally enabled and only requires an external voltage to disable.
4. Output conversion factor is 20 mV/mA of laser bias current.
5. Set at 500 mV at nominal output power; will track P_O linearly (–3 dB = 250 mV, +3 dB = 1000 mV).
6. Terminated into 220 Ω to GND with 100 Ω line-to-line.

Table 7. Receiver Electrical I/O Characteristics (T_C = 0 °C to 65 °C, V_{CC} = 3.3 V ± 5%)

Parameter	Symbol	Logic	Min	Typ	Max	Unit
Parallel Output Clock: Output High, V_{OH} Output Low, V_{OL}	POCLKP/N	 Diff. LVPECL	 V_{CC} – 1.3 V_{CC} – 2.00	 — —	 V_{CC} – 0.7 V_{CC} – 1.4	 V V
POCLK Duty Cycle	—	—	40	—	60	%
Output Data Signal Levels[1]: Output High, V_{OH} Output Low, V_{OL}	RxQ[0:15]P/N	Diff. LVPECL	 2.275 1.490	 — —	 2.420 1.680	 V V
RxQ[0:15] Rise/Fall Time[2]	—	—	—	—	1.0	ns
Frame Pulse: Output High, V_{OH} Output Low, V_{OL}	FP	LVPECL	 V_{CC} – 1.3 V_{CC} – 2.00	 — —	 V_{CC} – 0.7 V_{CC} – 1.4	 V V
Loss-of-Signal Output: Output High, V_{OH} Output Low, V_{OL}	LOS	LVTTL	 2.4 0	 — —	 V_{CC} 0.4	 V V
Out-of-Frame Input: Input High, V_{IH} Input Low, V_{IL}	OOF	LVTTL	 2.00 0.0	 — —	 V_{CC} + 1.0 0.8	 V V
Frame Enable Input	FRAMEN	LVTTL	 2.00 0.0	 — —	 V_{CC} + 1.0 0.8	 V V

1. Terminated into 330 Ω to ground.
2. 20% to 80%, 330 Ω to ground.

Table 8. Power Supply Characteristics (T_C = 0 °C to 65 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.13	3.3	3.47	V
dc Power Supply Current Drain[1]	I_{CC}	—	1800	2300	mA
Power Dissipation	P_{DISS}	—	6	—	W

1. Does not include output termination resistor current drain.

Timing Characteristics

Transmitter Data Input Timing

The TA16 transponder utilizes a unique FIFO to decouple the internal and external (PICLK) clocks. The FIFO can be initialized, which allows the system designer to have an infinite PCLK-to-PICLK delay through this interfacing logic (ASIC or commercial chip set). The configuration of the FIFO is dependent upon the I/O pins, which comprise the synch timing loop. This loop is formed from PHERR to PHINIT and PCLK to PICLK.

The FIFO can be thought of as a memory stack that can be initialized by PHINT or LOCKDET. The PHERR signal is a pointer that goes high when a potential timing mismatch is detected between PICLK and the internally generated PCLK clock. When PHERR is fed back to PHINIT, it initializes the FIFO so that it does not overflow or underflow.

The internally generated divide-by-16 clock is used to clock out data from the FIFO. PHINIT and LOCKDET signals will center the FIFO after the third PICLK pulse. This is done to ensure that PICLK is stable. This scheme allows the user to have an infinite PCLK to PICLK delay through the ASIC. Once the FIFO is centered, the PCLK and PICLK can have a maximum drift of ±5 ns.

During normal operation, the incoming data is passed from the PICLK input timing domain to the internally generated divide-by-16 PCLK timing domain. Although the frequency of PICLK and PCLK are the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two domains, the timing generator circuitry monitors the phase relationship between PICLK and PCLK.

When an FIFO timing violation is detected, the phase error (PHERR) signal pulses high. If the condition persists, PHERR will remain high. When PHERR is fed back into the PHINIT input (by shorting them on the printed-circuit board [PCB]), PHINIT will initialize the FIFO if PHINIT is held high for at least two byte clocks. The initialization of the FIFO prevents PCLK and PICLK from concurrently trying to read and write over the same FIFO bank.

During realignment, one to three bytes (16-bits wide) will be lost. Alternatively, the customer logic can take in the PHERR signal, process it, and send an output to the PHINIT input in such a way that only idle bytes are lost during the initialization of the FIFO. Once the FIFO has been initialized, PHERR will go inactive.

Timing Characteristics (continued)

Input Timing Mode 1

In the configuration shown in Figure 4, PHERR to PHINIT has a zero delay (shorted on the PCB) and the PCLK is used to clock 16-bit-wide data out of the customer ASIC. The FIFO in the multiplexer is 16-bits wide and six registers deep.

The PCLK and PICLK signals respectively control the READ and WRITE counters for the FIFO. The data bank from the FIFO has to be read by the internally generated clock (PCLK) only once after it has been written by the PICLK input.

Since the delay in the customer ASIC is unknown, the two clocks (PCLK and PICLK) might drift in respect to each other and try to perform the read and writer operation on the same bank in the FIFO at the same time. However, before such a clock mismatch can occur, PHERR goes high and, if externally connected to PHINIT, will initialize the FIFO provided PHINIT remains high for at least two byte clocks. One to three 16-bit words of data will be lost during the initialization of the FIFO.

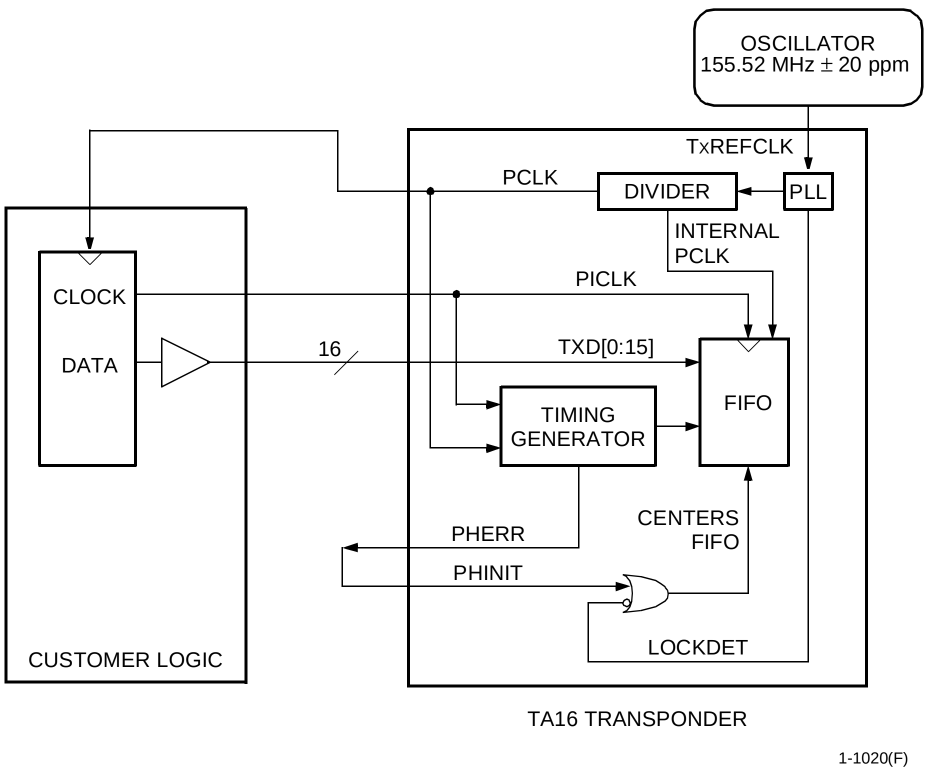


Figure 4. Block Diagram Timing Mode 1

Timing Characteristics (continued)

Input Timing Mode 2

To avoid the loss of data, idle or dummy bytes should be sent on the TxD[0:15] bus whenever PHERR goes high. In the configuration shown in Figure 5, the PHERR signal is used as an input to the customer logic. Upon detecting a high on the PHERR signal, the customer logic should return a high signal, one that remains high for at least two byte-clock cycles, to the PHINIT input of the TA16. Also, when PHERR goes high, the customer logic should start sending idle or dummy bytes to the TA16 on the TxD[0:15] bus. This should continue until PHERR goes low.

The FIFO is initialized two-to-eight byte clocks after PHINIT goes high for two byte clocks. PHERR goes low after the FIFO is initialized. Upon detecting a low on PHERR, the customer logic can start sending real data bytes on TxD[0:15]. The two timing loops (PCLK to PICLK and PHERR to PHINIT) do not have to be of equal length.

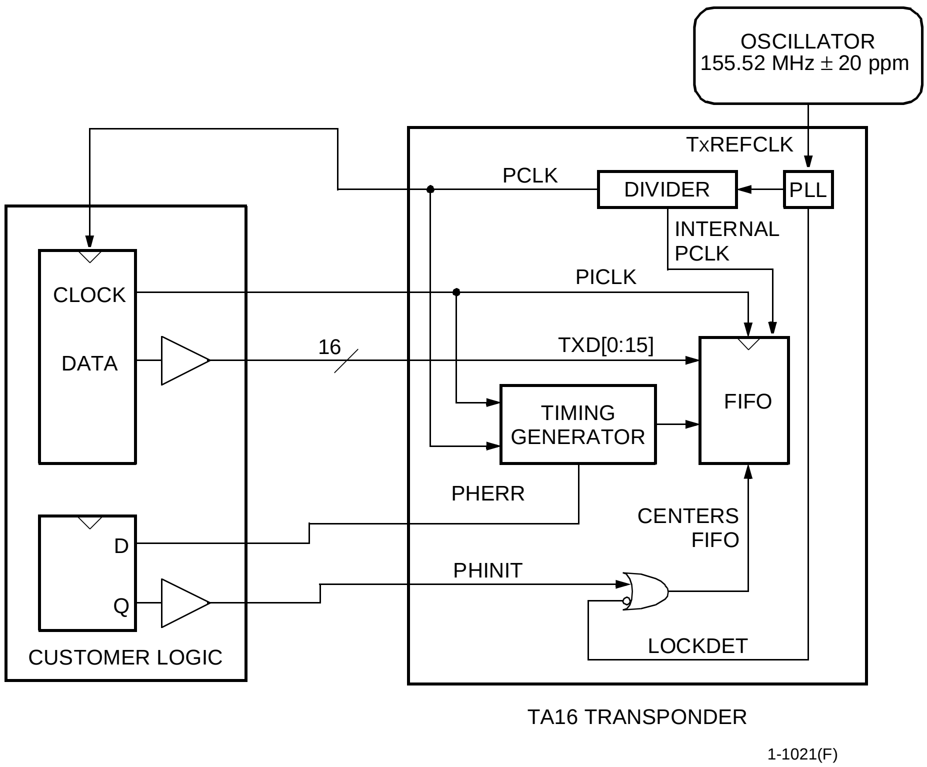


Figure 5. Block Diagram Timing Mode 2

Timing Characteristics (continued)

Forward Clocking

In some applications, it is necessary to forward-clock the data in a SONET/SDH system. In this application, the reference clock from which the high-speed serial clock is synthesized and the parallel data clock both originate from the same source on the customer application circuit. The timing control logic in the TA16 transponder transmitter automatically generates an internal load signal that has a fixed relationship to the reference clock. The logic takes into account the variation of the reference clock to the internal load signal over temperature and voltage. The connections required to implement this clocking method are shown in Figure 6. The setup and hold times for PICLK to TxD[0:15] must be met by the customer logic.

Possible problems: to meet the jitter generation specifications required by SONET/SDH, the jitter of the reference clock must be minimized. It could be difficult to meet the SONET jitter generation specifications using a reference clock generated from the customer logic.

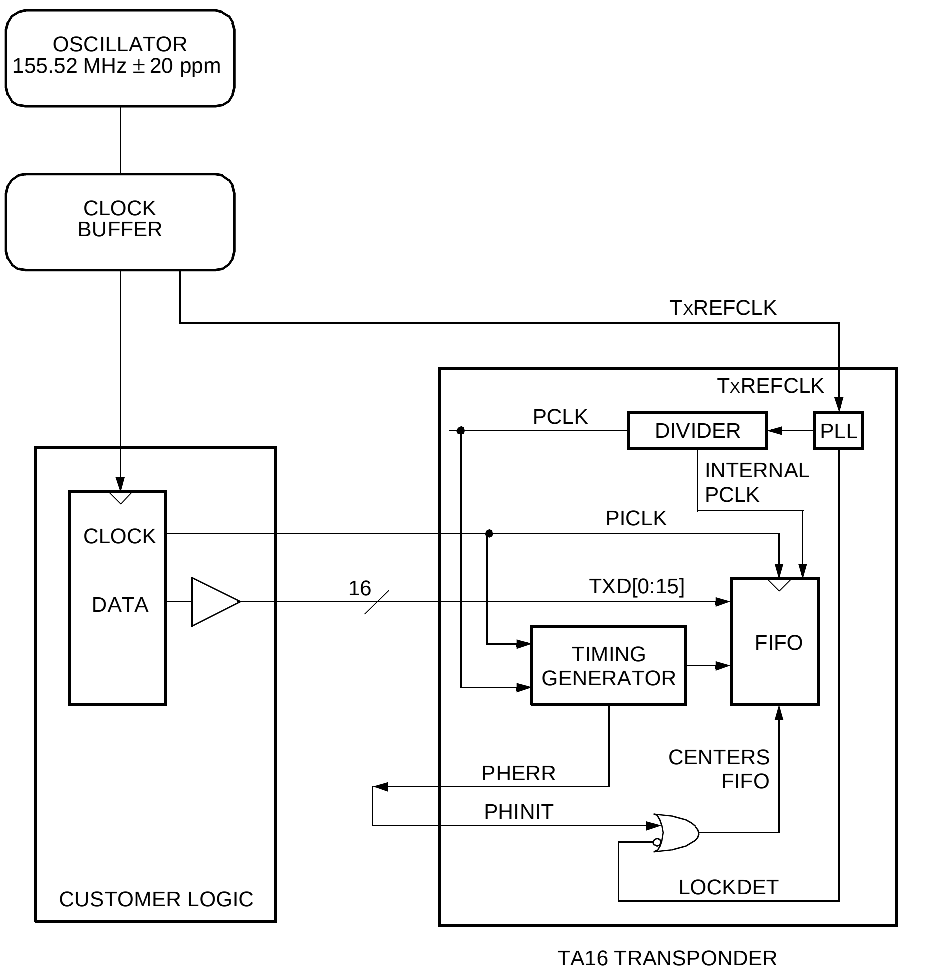


Figure 6. Forward Clocking of the TA16 Transmitter

Timing Characteristics (continued)

PCLK-to-PICLK Timing

After powerup or RESET, the LOCKDET signal will go active, signifying that the PLL has locked to the clock provided on the TXREFCLK input. The FIFO is initialized on the third PICLK after LOCKDET goes active. The PCLK-to-PICLK delay (tD) can have any value before the FIFO is initialized. The tD is fixed at the third PICLK after LOCKDET goes active. Once the FIFO is initialized, PCLK and PICLK cannot drift more than 5.2 ns; tCH cannot be more than 5.2 ns.

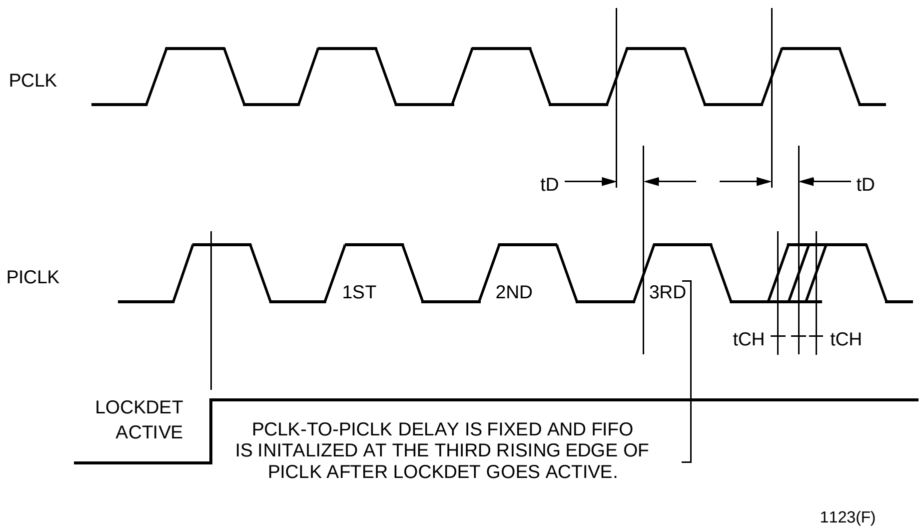


Figure 7. PCLK-to-PICLK Timing

Timing Characteristics (continued)

PHERR/PHINIT

Case 1— PHERR and PHINIT are shorted on the printed-circuit board:

PHINIT would go high whenever there is a potential timing mismatch between PCLK and PICLK. PHINIT would remain high as long as the timing mismatch between PCLK and PICLK. If PHINIT is high for more than two byte clocks, the FIFO will be initialized. PHINIT will initialize the FIFO two-to-eight byte clocks after it is high for at least two byte clocks, PHERR (and thus PHINIT) goes active once the FIFI is initialized.

Case 2—PHERR signal is input to the customer logic and the customer logic outputs a signal to PHINIT:

Another possible configuration is where the PHERR signal is input into the customer logic and the customer logic sends an output to the PHINIT input. However, the customer logic must ensure that, upon detecting a high on PHERR, the PHINIT signal remains high for more than two byte clocks. If PHINIT is high for less than two byte clocks, the FIFO is not guaranteed to be initialized. Also, the customer logic must ensure that PHINIT goes low after the FIFO is initialized (PHERR goes low).

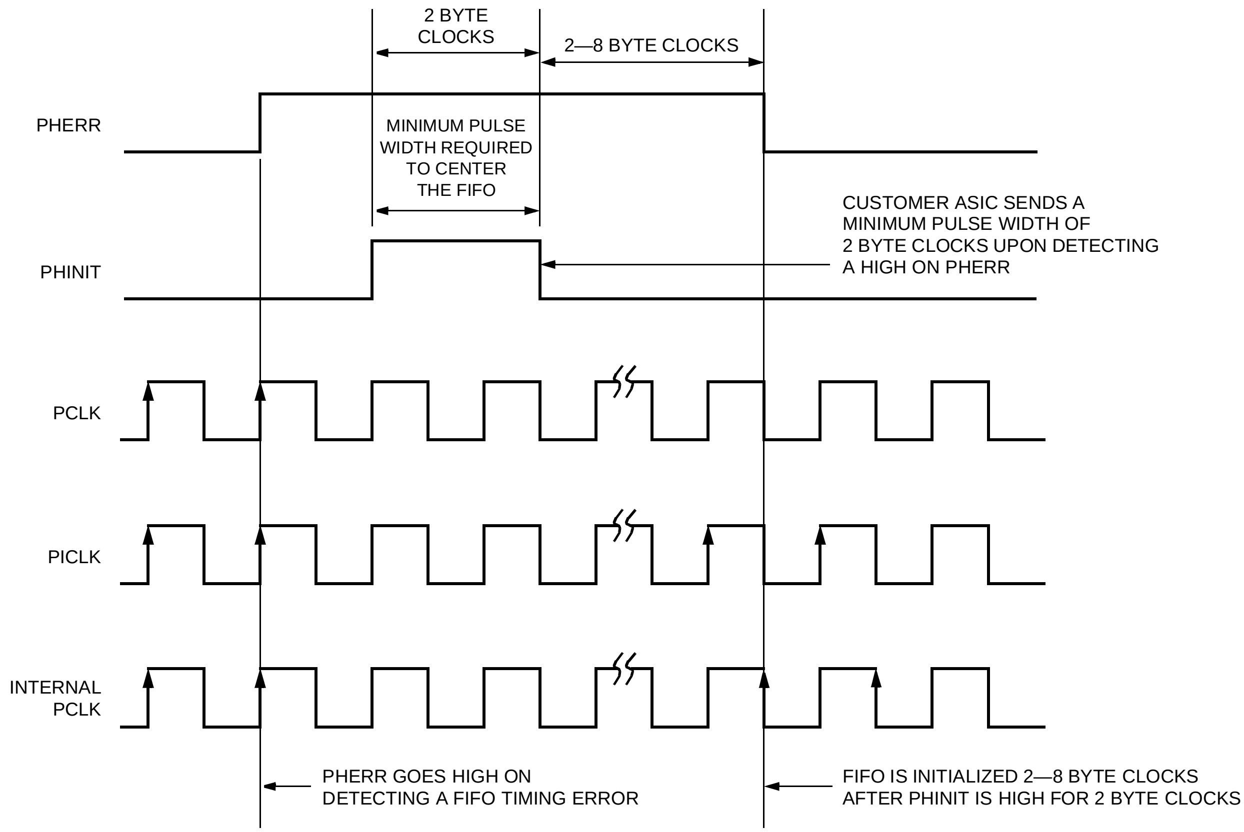


Figure 8. PHERR/PHINIT Timing

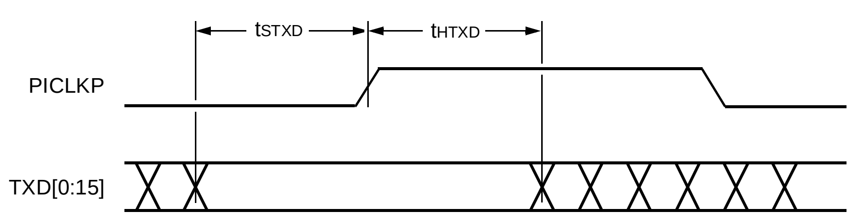


Figure 9. ac Input Timing

Timing Characteristics (continued)

Table 9. Transmitter ac Timing Characteristics

Symbol	Description	Min	Max	Unit
tSTxD	TxD[0:15] Setup Time w. r. t. PICLK	1.5	—	ns
tHTxD	TxD[0:15] Hold Time w. r. t. PICLK	0.5	—	ns
—	PCLKP/N Duty Cycle	40	60	%
—	PICLKP/N Duty Cycle	40	60	%
tD	PCLK -to-PICLK Drift After FIFO is Centered	—	5.2	ns

Table 10. Receiver ac Timing Characteristics

Symbol	Description	Min	Max	Unit
—	POCLK Duty Cycle	45	55	%
—	RxD[15:0] Rise and Fall Time[1]	—	1.0	ns
tPPOUT	POCLK Low to RxD[15:0] Valid prop. delay	–1	1	ns
tSPOUT	RxD[15:0] and FP Setup Time w. r. t. POCLK	2	—	ns
tHPOUT	RxD[15:0] and FP Hold Time w. r. t. POCLK	2	—	ns

1. 20% to 80%; 330 Ω to GND

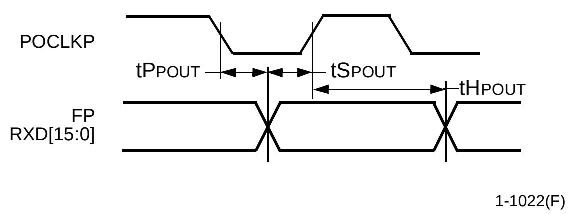


Figure 10. Receiver Output Timing Diagram

Timing Characteristics (continued)

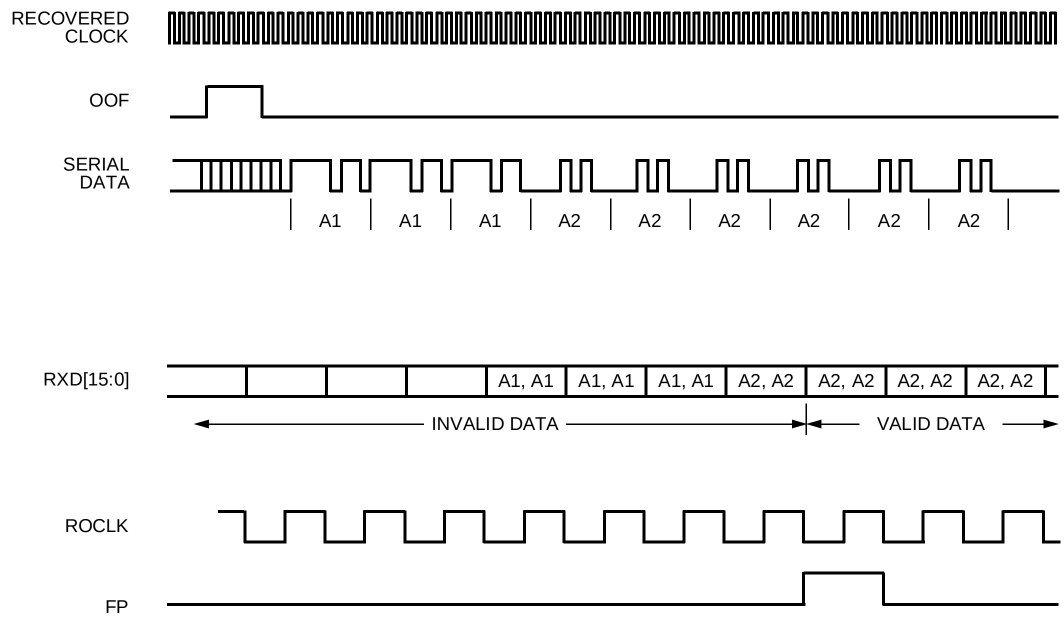
Receiver Framing

Figure 11 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF. Both the frame and byte boundaries are recognized upon receipt of the first A2 byte following three consecutive A1 bytes. The third A2 byte is the first data byte to be reported with the correct byte alignment on the outgoing data bus (RxD[15:0]). Concurrently, the frame pulse (FP) is set high for one POCLK cycle.

The frame and byte boundary detection block is activated by the rising edge of OOF and stays active until the first FP pulse.

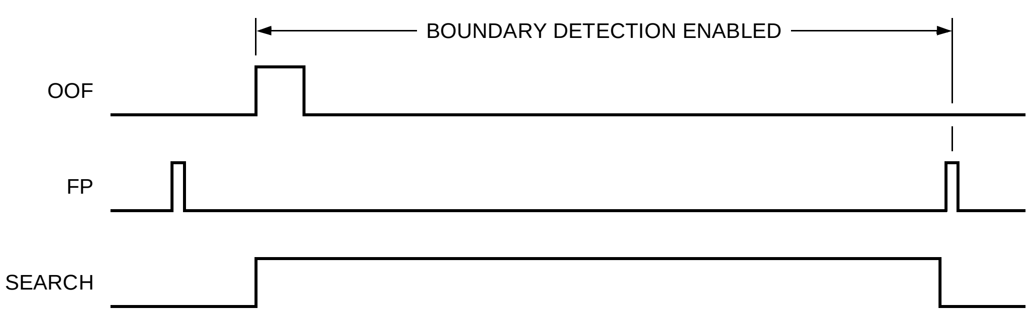
Figure 12 shows the frame and byte boundary detection activation by a rising edge of OOF and deactivation by the first FP pulse.

Figure 13 shows the frame and byte boundary detection by the activation of a rising edge of OOF and deactivation by the FRAMEN input.



1-1023(F)r.3

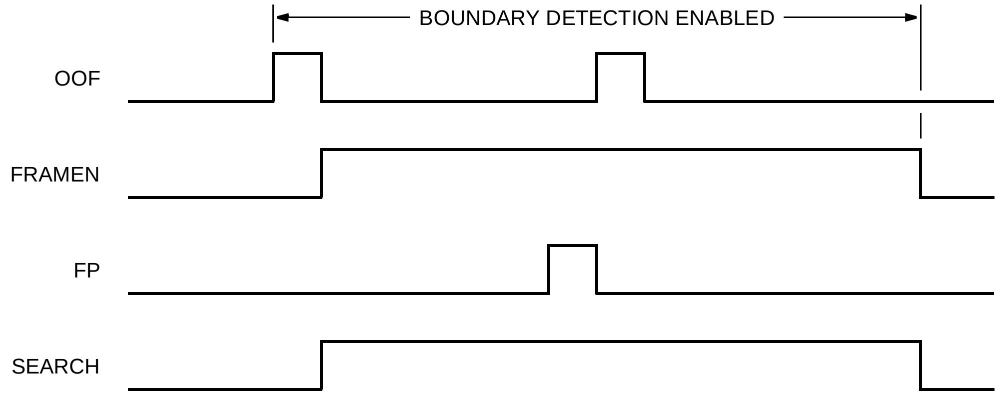
Figure 11. Frame and Byte Detection



1-1024(F)

Figure 12. OOF Timing (FRAMEN = High)

Timing Characteristics (continued)



1-1025(F)

Figure 13. FRAMEN Timing

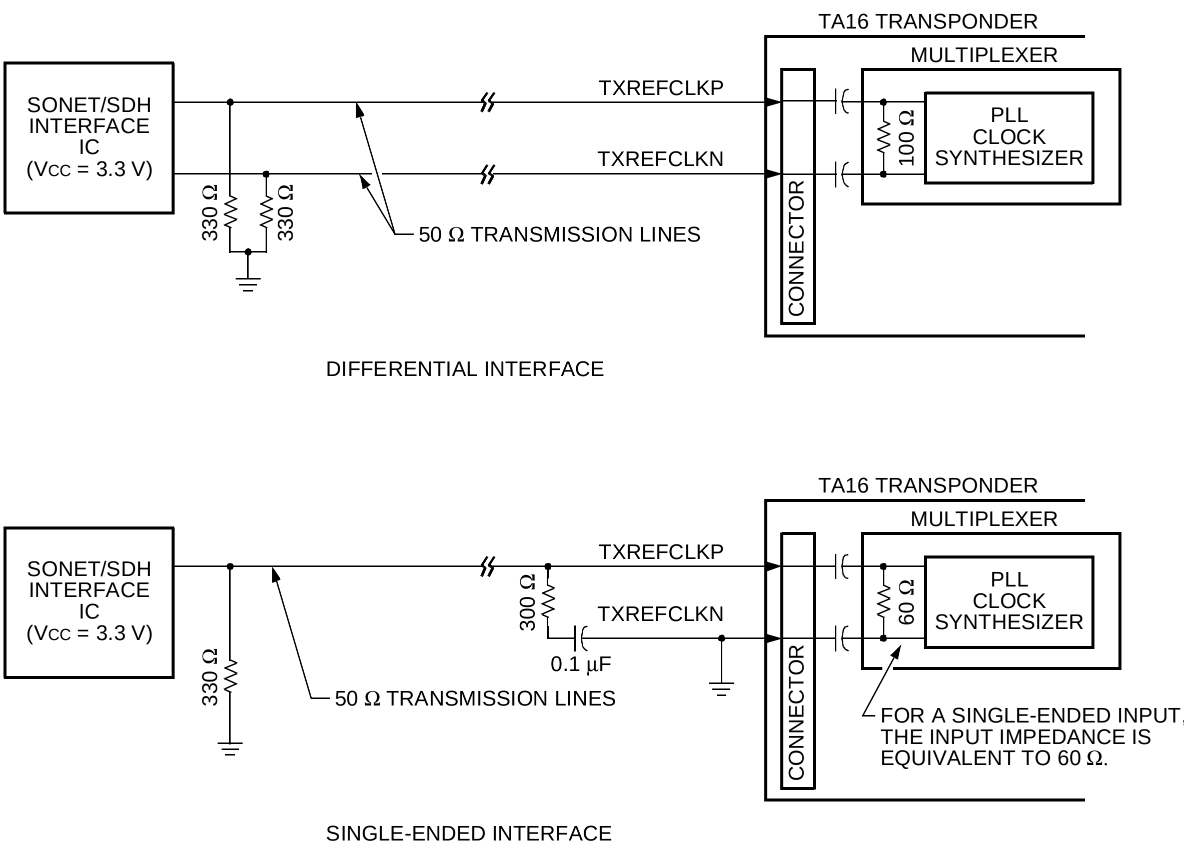


Figure 14. Interfacing to the TxRefClk Input

Qualification and Reliability

To help ensure high product reliability and customer satisfaction, Agere is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronics modules are qualified to Agere internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies* * requirements. This qualification program fully meets the intent of *Telcordia Technologies* reliability practices TR-NWT-000468 and TA-TSY-000983. In addition, the Agere Optoelectronics design, development, and manufacturing facility has been certified to be in full compliance with the latest *ISO*† -9001 Quality System Standards.

* *Telcordia Technologies* is a trademark of Telcordia Technologies, Inc.
† *ISO* is a registered trademark of the International Organization for Standardization.

Laser Safety Information

Class I Laser Product

All versions of the TA16-type transponders are classified as Class I laser products per FDA/CDRH, 21 CFR 1040 Laser Safety requirements. The transponders have been registered/certified with the FDA under Accession Number 8720009. All versions are classified as Class I laser products per *IEC*‡ 60825-1:1993.

CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.

This product complies with 21 CFR 1040.10 and 1040.11.
8.8 µm/125 µm single-mode pigtail with 900 µm tight buffer jacket and connector.
Wavelength = 1.3 µm, 1.5 µm.
Maximum power = 1.6 mW.
Product is not shipped with power supply.
Because of size constraints, laser safety labeling is not affixed to the module but is attached to the outside of the shipping carton.

NOTICE

Unterminated optical connectors can emit laser radiation.

Do not view with optical instruments.

Electromagnetic Emissions and Immunity

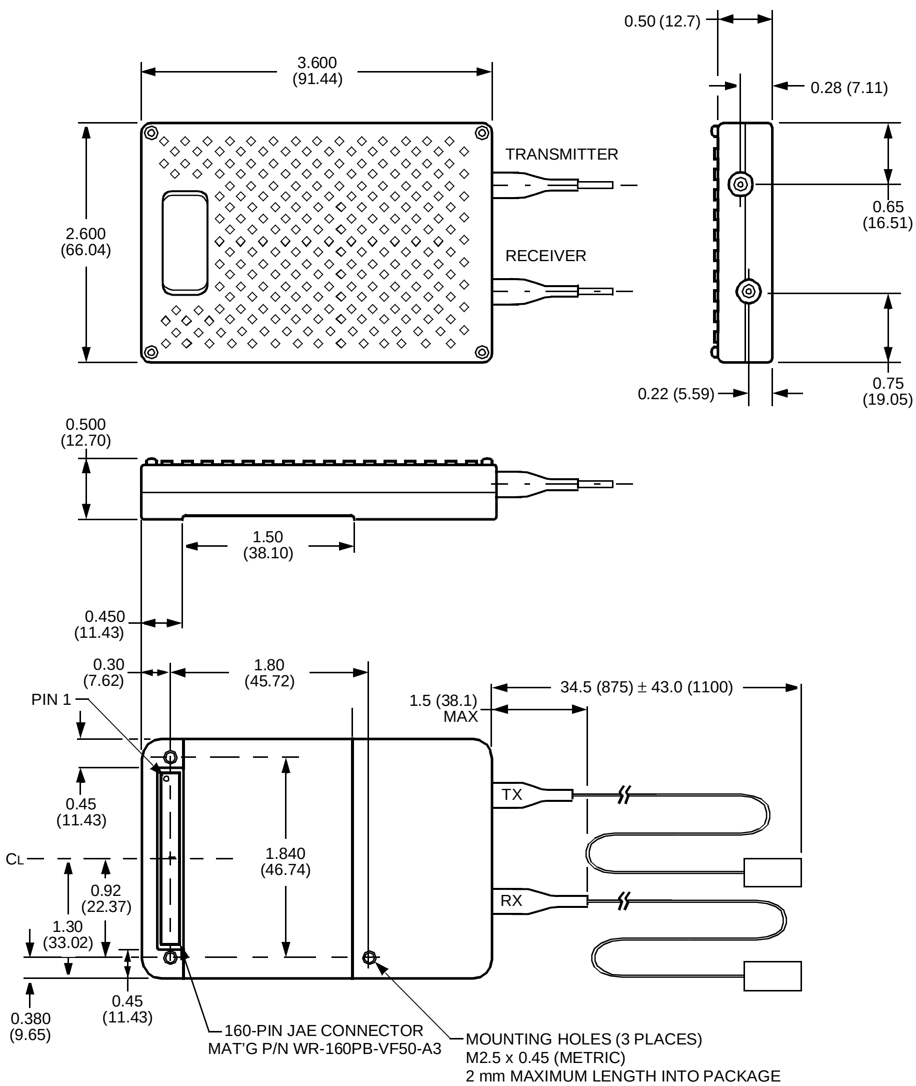
The TA16 transponder will be tested against CENELEC EN50 081 part 1 and part 2, FCC 15, Class B limits for emissions.

The TA16 transponder will be tested against CENELEC EN50 082 part 1 immunity requirements.

‡ *IEC* is a registered trademark of The International Electrotechnical Commission.

Outline Diagram

Dimensions are in inches and (millimeters).



1-1012(F).d

Ordering Information

ORDER CODE: TA 16 – XX – X – XX

BASIC PART NUMBER

STM LEVEL
16 = STM-16 (SONET OC-48)

APPLICATION
N1 = I-16, 1310 nm, intraoffice/(SONET short reach)
S1 = S-16.1, 1310 nm, short hauL (SONET IR-1)
S2 = S-16.2, 1550 nm, short haul (SONET IR-2)
L1 = L-16.1, 1310 nm, long hauL (SONET LR-1)
L2 = L-16.2, 1550 nm, long haul (SONET LR-2)

CONNECTOR*
C = SC
F = FC

OPTIONS

* Other connectors may be made available.

Table 11. Ordering Information

Code	Application	Connector	Comcode
TA16N1CAA	1310 nm, Intraoffice	SC	108440066
TA16N1FAA	1310 nm, Intraoffice	FC/PC	108440074
TA16S1CAA	1310 nm, Short Haul	SC	108432907
TA16S1FAA	1310 nm, Short Haul	FC/PC	108432915
TA16S2CAA	1550 nm, Short Haul	SC	108432923
TA16S2FAA	1550 nm, Short Haul	FC/PC	108432931
TA16L1CAA	1310 nm, Long Haul	SC	108432865
TA16L1FAA	1310 nm, Long Haul	FC/PC	108432873
TA16L2CAA	1550 nm, Long Haul	SC	108432881
TA16L2FAA	1550 nm, Long Haul	FC/PC	108432899

Related Product Information

Table 12. Related Product Information

Description	Document Number
Using the Lucent Technologies Transponder Test Board Application Note	AP00-017OPTO

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@agere.com**
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