

MEDIUM POWER PHASE CONTROL THYRISTORS

Power Modules

Features

- Electrically isolated base plate
- Types up to 1200 V_{RRM}
- 3500 V_{RMS} isolating voltage
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL E78996 approved 

50 A
70 A
90 A

Description

These series of T-modules are intended for general purpose applications such as battery chargers, welders and plating equipment, regulated power supplies and temperature and speed control circuits. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built.

Major Ratings and Characteristics

Parameters	T50RIA	T70RIA	T90RIA	Units
$I_{T(AV)}$	50	70	90	A
@ T _C	70	70	70	°C
$I_{T(RMS)}$	80	110	141	A
I_{TSM} @50Hz	1310	1660	1780	A
@60Hz	1370	1740	1870	A
I^2t @50Hz	8550	13860	15900	A ² s
@60Hz	7800	12650	14500	A ² s
$I^2\sqrt{t}$	85500	138500	159100	A ² √s
V _{DRM} /V _{RRM}	100 to 1200			V
T _J	-40 to 125			°C

T..RIA Series

Bulletin I27105 rev. B 02/02

International
IOR Rectifier

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} , maximum repetitive peak reverse voltage V	V_{RSM} , maximum non-repetitive peak reverse voltage V	I_{DRM}/I_{RRM} max. @ 25°C μA
T50RIA T70RIA T90RIA	10	100	150	100
	20	200	300	
	40	400	500	
	60	600	700	
	80	800	900	
	100	1000	1100	
	120	1200	1300	

On-state Conduction

Parameter	T50RIA	T70RIA	T90RIA	Units	Conditions
$I_{T(AV)}$ Max. average on-state current @ Case temperature	50 70	70 70	90 70	A °C	180° conduction, half sine wave
$I_{T(RMS)}$ Max. RMS on-state current	80	110	141	A	
I_{TSM} Maximum peak, one-cycle on-state, non-repetitive surge current	1310 1370 1100 1150	1660 1740 1400 1460	1780 1870 1500 1570	A	$t = 10ms$ $t = 8.3ms$ $t = 10ms$ $t = 8.3ms$ No voltage reappplied 100% V_{RRM} reappplied Sine half wave, Initial $T_J = T_J$ max.
I^2t Maximum I^2t for fusing	8550 7800 6050 5520	13860 12650 9800 8950	15900 14500 11250 10270	A ² s	$t = 10ms$ $t = 8.3ms$ $t = 10ms$ $t = 8.3ms$ No voltage reappplied 100% V_{RRM} reappplied Initial $T_J = T_J$ max.
I^2/t Maximum I^2/t for fusing	85500	138500	159100	A ² √s	$t = 0.1$ to 10ms, no voltage reappplied
$V_{T(TO)1}$ Low level value of threshold voltage	0.97	0.77	0.78	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, @ T_J max.
$V_{T(TO)2}$ High level value of threshold voltage	1.13	0.88	0.88	V	$(I > \pi \times I_{T(AV)})$, @ T_J max.
r_{t1} Low level value on-state slope resistance	4.1	3.6	2.9	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, @ T_J max.
r_{t2} High level value on-state slope resistance	3.3	3.2	2.6	mΩ	$(I > \pi \times I_{T(AV)})$, @ T_J max.
V_{TM} Maximum on-state voltage drop	1.60	1.55	1.55	V	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = 25^\circ C$, $tp = 400\mu s$ square Av. power = $V_{T(TO)} \times I_{T(AV)} + r_f \times (I_{T(RMS)})^2$
I_H Maximum holding current	200			mA	Anode supply = 6V initial $I_T = 30A$, $T_J = 25^\circ C$
I_L Maximum latching current	400			mA	Anode supply = 6V resistive load = 10Ω gate pulse: 10V, 100μs, $T_J = 25^\circ C$

Switching

Parameter	T50RIA	T70RIA	T90RIA	Units	Conditions
t_{gd} Typical turn-on time	0.9			μs	$T_J = 25^\circ C$ $V_d = 50\% V_{DRM}$, $I_{TM} = 50 A$ $I_g = 500mA$, $tr \leq 0.5$, $tp \geq 6\mu s$
t_{rr} Typical reverse recovery time	3.0			μs	$T_J = 125^\circ C$, $I_{TM} = 50A$ $tp = 300\mu s$ $di/dt = 10A/\mu s$
t_q Typical turn-off time	110			μs	$T_J = T_J$ max., $I_{TM} = 50A$, $tp = 300\mu s$, $-di/dt = 15A/\mu s$, $V_r = 100V$; linear to 80% V_{DRM}

Blocking

Parameter	T50RIA	T70RIA	T90RIA	Units	Conditions
I_{RRM} I_{DRM} Maximum peak reverse and off-state leakage current	15			mA	$T_J = T_J = T_J \text{ max.}$
V_{INS} RMS isolation voltage	3500			V	50Hz, circuit to base, all terminals shorted, $T_J = 25^\circ\text{C}$, $t = 1\text{s}$
dv/dt Critical rate of rise of off-state voltage	500			V/ μs	$T_J = T_J \text{ max.}$, linear to 80% rated V_{DRM} (1)

(1) Available with $dv/dt = 1000\text{V}/\mu\text{s}$, to complete code add S90 i.e. T90RIA80S90

Triggering

Parameter		T50RIA	T70RIA	T90RIA	Units	Conditions	
P _{GM}	Max. peak gate power	10	12	12	W	tp ≤ 5ms, T _J = T _J max.	
P _{G(AV)}	Max. average gate power	2.5	3.0	3.0	W	f = 50Hz, T _J = T _J max.	
I _{GM}	Max. peak gate current	2.5	3.0	3.0	A	tp ≤ 5ms, T _J = T _J max.	
-V _{GT}	Max. peak negative gate voltage	10	10	10	V		
V _{GT}	Max. required DC gate voltage to trigger	4.0	4.0	4.0	V	T _J = - 40°C	Anode supply = 6V, resistive load; Ra = 1Ω
		2.5	2.5	2.5		T _J = 25°C	
		1.5	1.5	1.5		T _J = T _J max.	
I _{GT}	Max. required DC gate current to trigger	250	270	270	mA	T _J = - 40°C	Anode supply = 6V, resistive load; Ra = 1Ω
		100	120	120		T _J = 25°C	
		50	60	60		T _J = T _J max.	
V _{GD}	Max. gate voltage that will not trigger	0.2	0.2	0.2	V	@ T _J = T _J max., rated V _{DRM} applied	
I _{GD}	Max. gate current that will not trigger	5.0	6.0	6.0	mA		
di/dt	Max. rate of rise of turned-on current	200			A/μs	V _D = 0.67 rated V _{DRM} ; I _{TM} = 2 x rated di/dt I _g = 400mA for T50RIA and I _g = 500mA for T70RIA & T90RIA; tr < 0.5μs, tp ≥ 6μs For repetitive value use 40% non-repetitive Per JEDEC std. RS397, 5.2.2.6	
		180					
		160					
		150					

Thermal and Mechanical Specifications

Parameter		T50RIA	T70RIA	T90RIA	Units	Conditions
T _J	Max. junction operating temperature range	-40 to 125			°C	
T _{stg}	Max. storage temperature range	-40 to 150			°C	
R _{thJC}	Max. thermal resistance, junction to case	0.65	0.50	0.38	K/W	DC operation, per junction
R _{thCS}	Max. thermal resistance, case to heatsink	0.2			K/W	Mounting surface smooth, flat and greased
T	Mounting torque ± 10%	1.3 ± 10%			Nm	M3.5 mounting screws (2) non lubricated M5 screw terminals threads
	to heatsink terminals	3 ± 10%				
wt	Approximate weight	54			g	See outline table
	Case style	D-56				T type

(2) A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.

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ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Devices	Sinusoidal conduction @ T_J max.					Rectangular conduction @ T_J max.					Units
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
T50RIA	0.08	0.10	0.13	0.19	0.31	0.06	0.10	0.14	0.20	0.32	K/W
T70RIA	0.07	0.08	0.10	0.14	0.24	0.05	0.08	0.11	0.15	0.24	
T90RIA	0.05	0.06	0.08	0.12	0.20	0.04	0.06	0.09	0.12	0.20	

Ordering Information Table

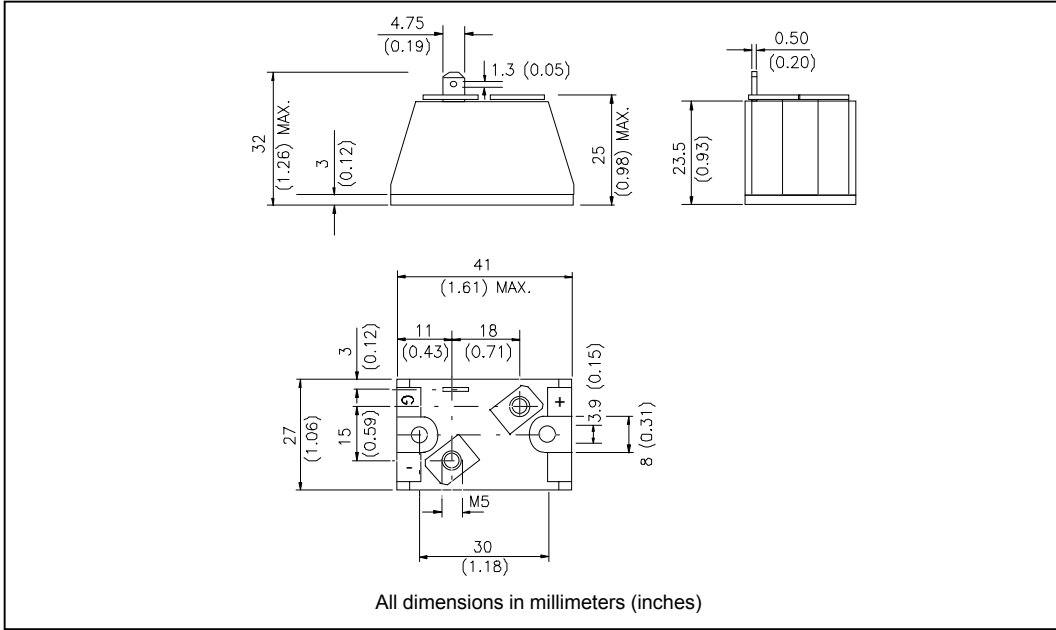
Device Code

T	50	RIA	120
①	②	③	④

1 - Module type
2 - Current rating
3 - Circuit configuration **
4 - Voltage code : code x 10 = V_{RRM}

Circuit configuration **

Outline Table



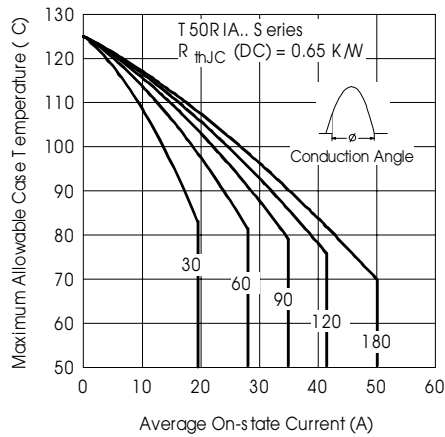


Fig. 1 - Current Ratings Characteristics

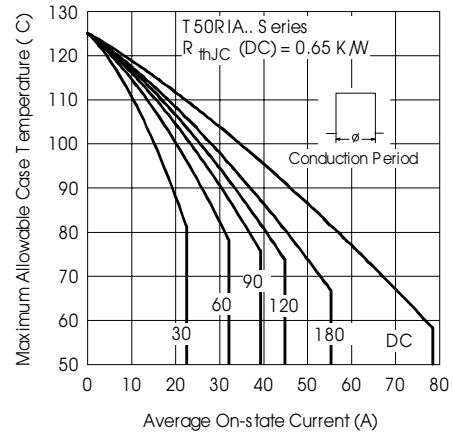


Fig. 2 - Current Ratings Characteristics

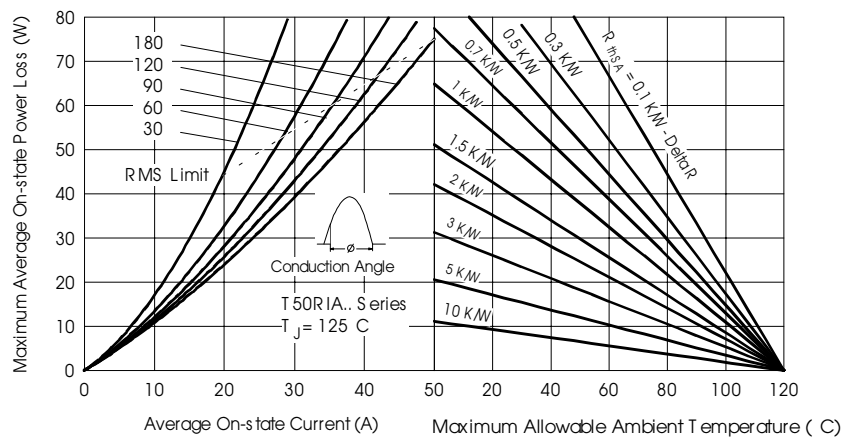


Fig. 3 - On-state Power Loss Characteristics

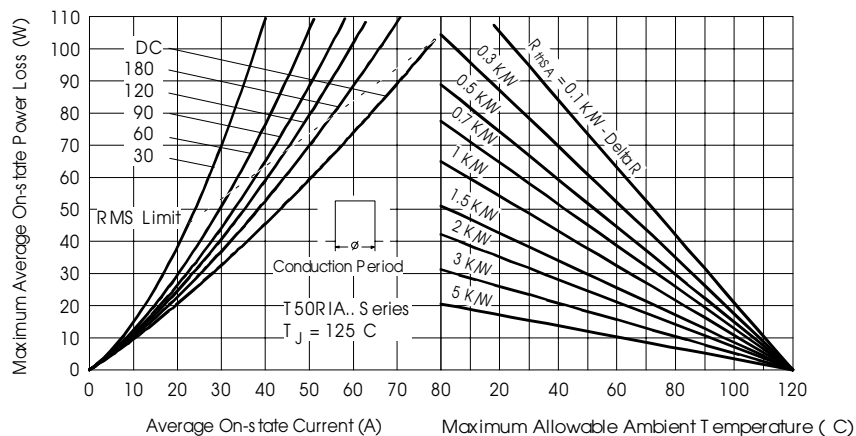


Fig. 4 - On-state Power Loss Characteristics

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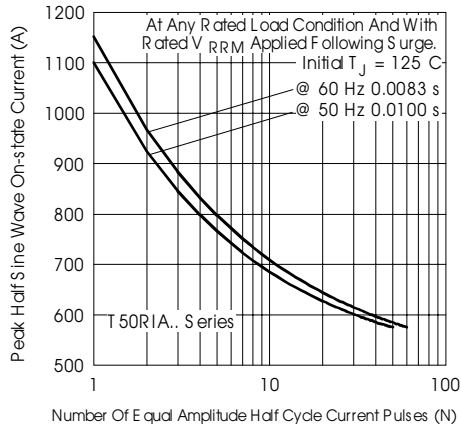


Fig. 5 - Maximum Non-Repetitive Surge Current

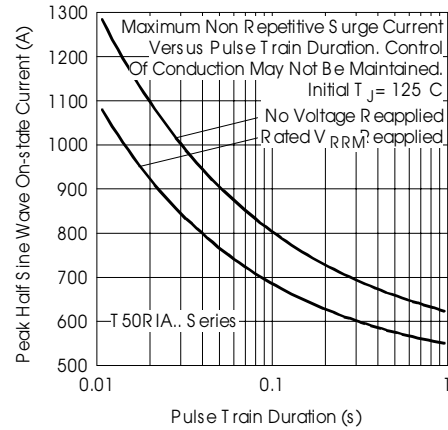


Fig. 6 - Maximum Non-Repetitive Surge Current

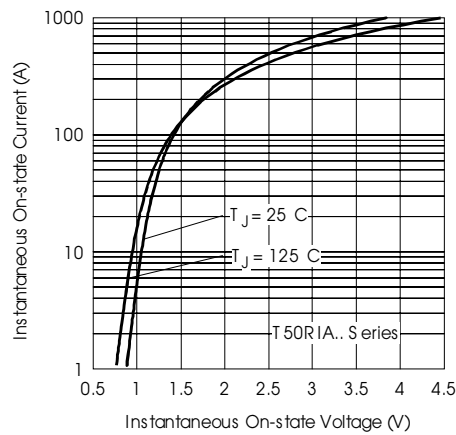


Fig. 10 - On-state Voltage Drop Characteristics

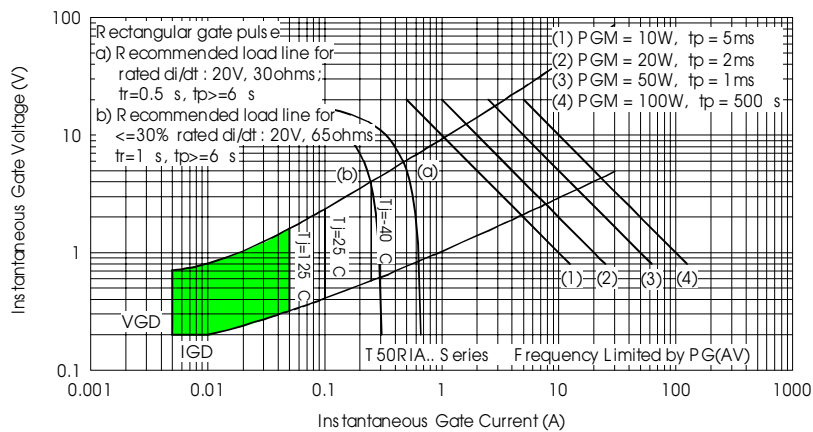


Fig. 9 - Gate Characteristics

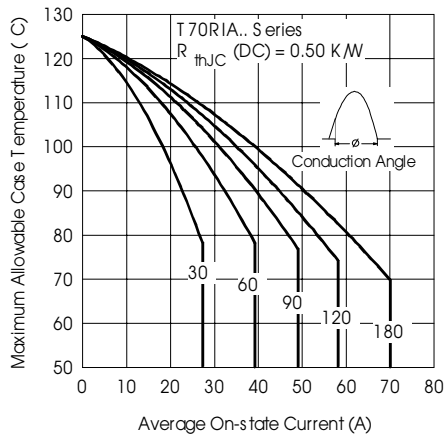


Fig. 12 - Current Ratings Characteristics

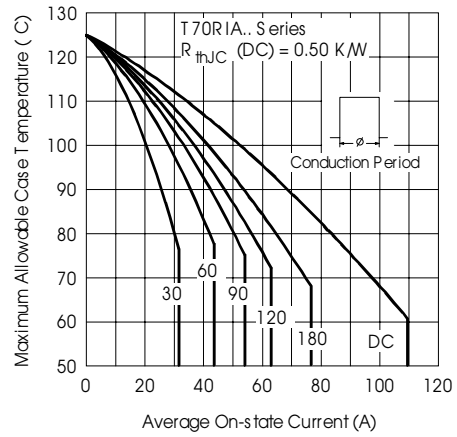


Fig. 13 - Current Ratings Characteristics

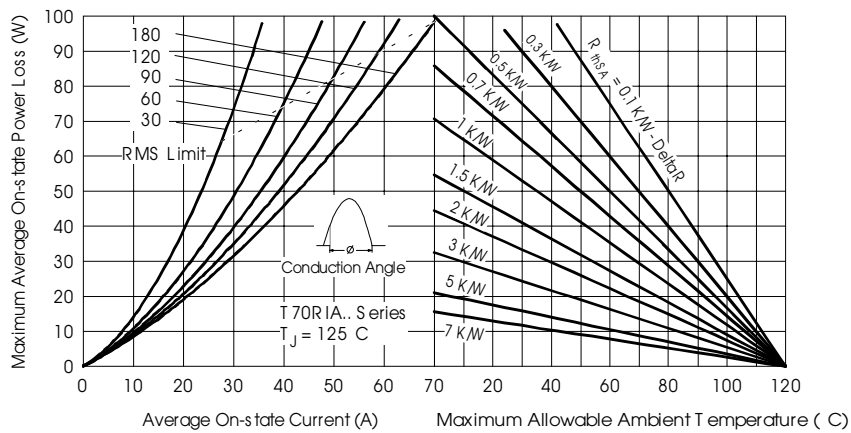


Fig. 18 - On-state Power Loss Characteristics

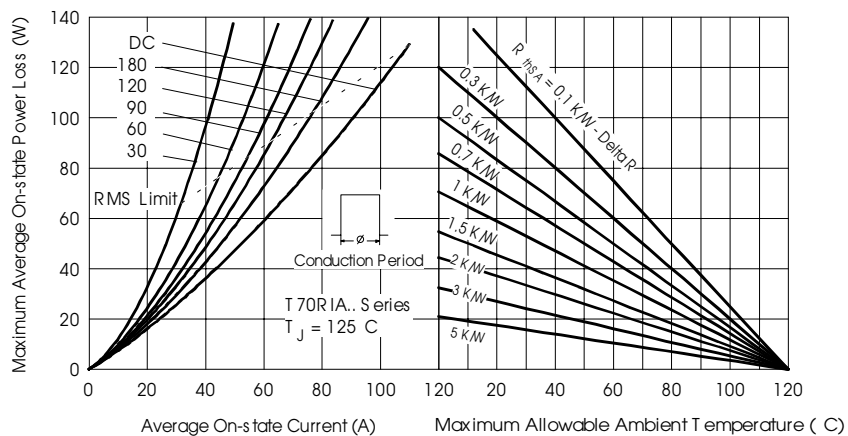


Fig. 15 - On-state Power Loss Characteristics

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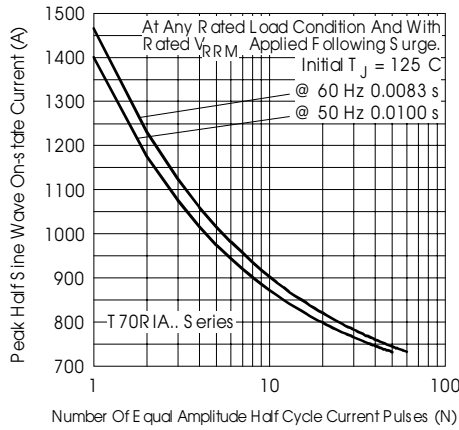


Fig. 16 - Maximum Non-Repetitive Surge Current

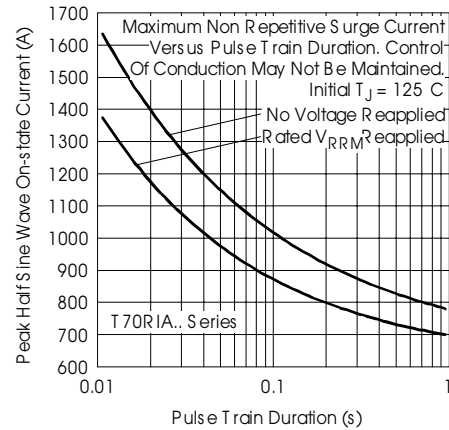


Fig. 17 - Maximum Non-Repetitive Surge Current

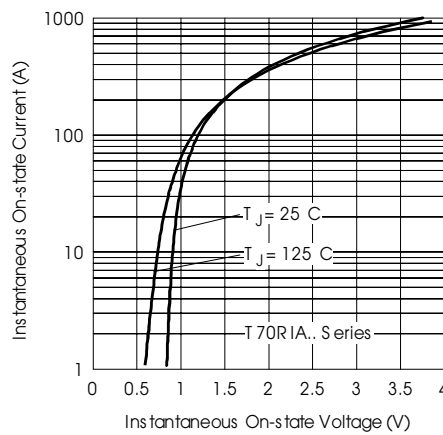


Fig. 10 - On-state Voltage Drop Characteristics

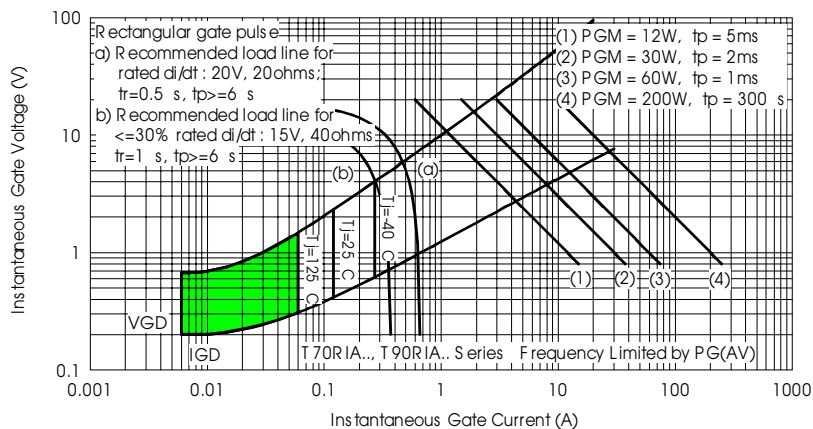


Fig. 19 - Gate Characteristics

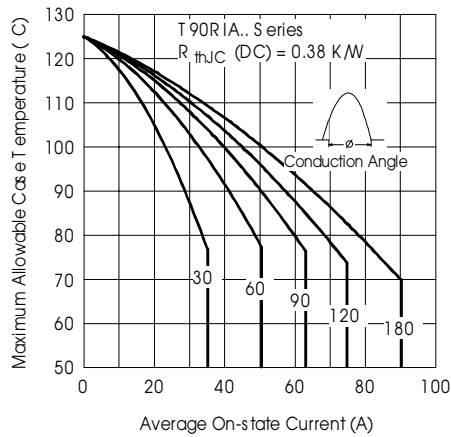


Fig. 23 - Current Ratings Characteristics

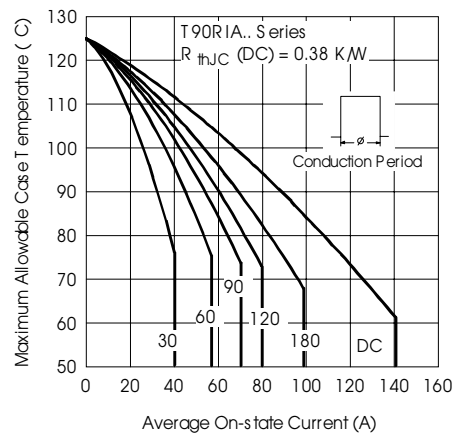


Fig. 24 - Current Ratings Characteristics

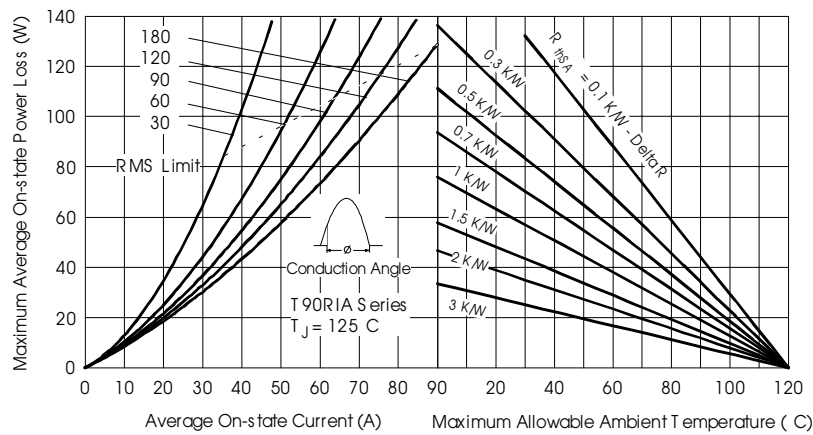


Fig. 29 - On-state Power Loss Characteristics

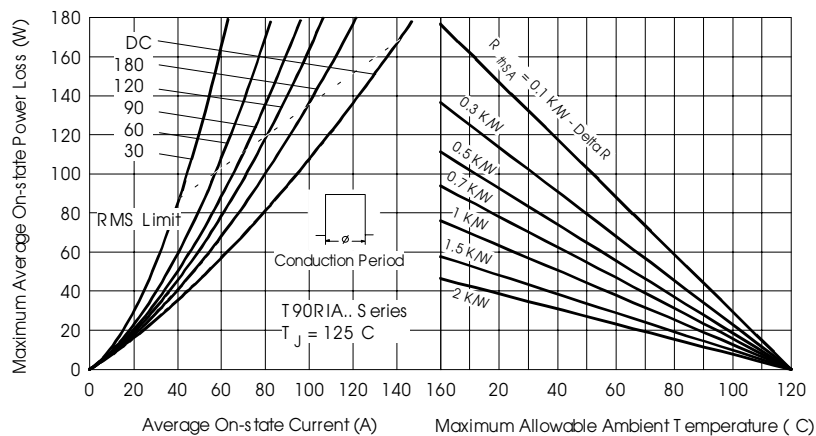


Fig. 29 - On-state Power Loss Characteristics

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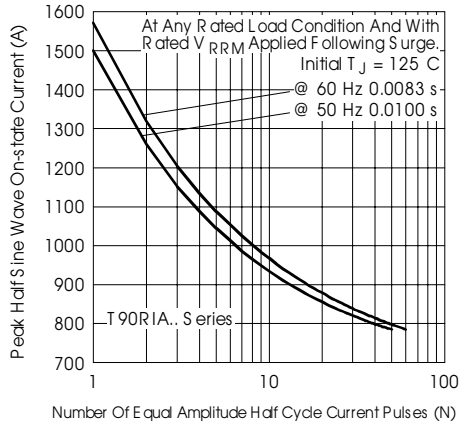


Fig. 27 - Maximum Non-Repetitive Surge Current

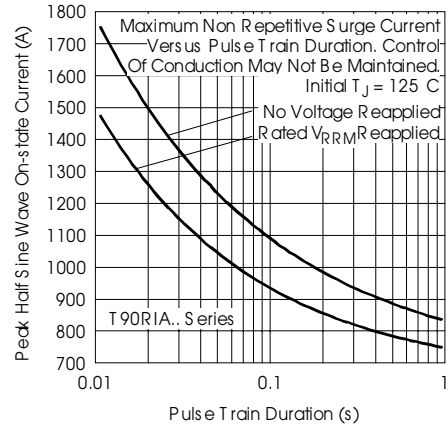


Fig. 28 - Maximum Non-Repetitive Surge Current

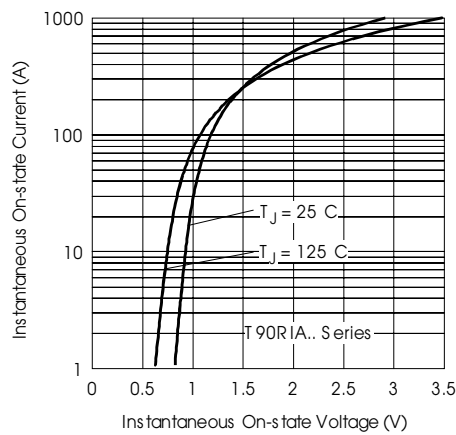


Fig. 21 - On-state Voltage Drop Characteristics

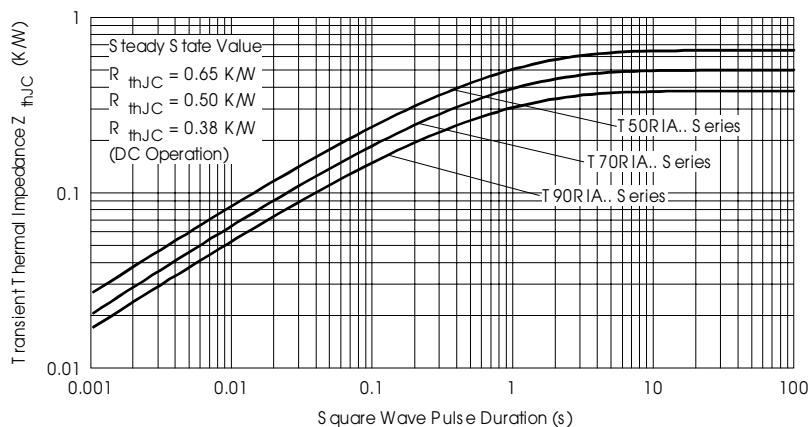


Fig. 34 - Thermal Impedance Z_{thJC} Characteristics

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial Level.
Qualification Standards can be found on IR's Web site.

International
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