

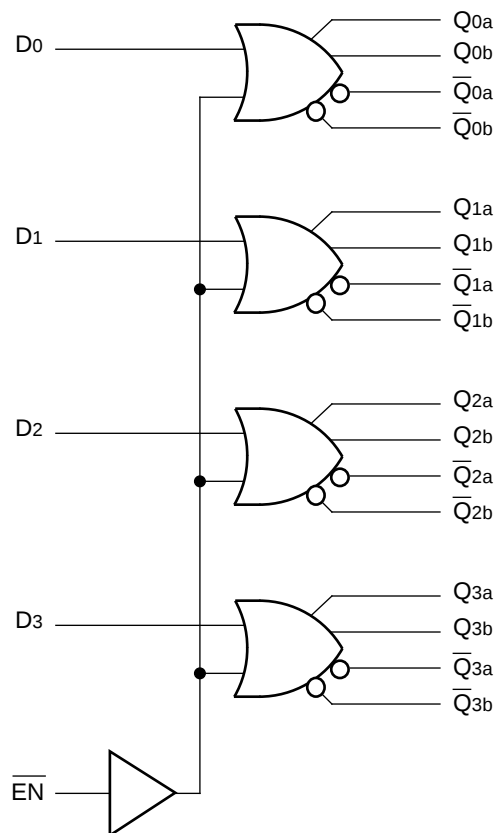
FEATURES

- 600ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- Common enable input
- Fully compatible with industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E112
- Available in 28-pin PLCC package

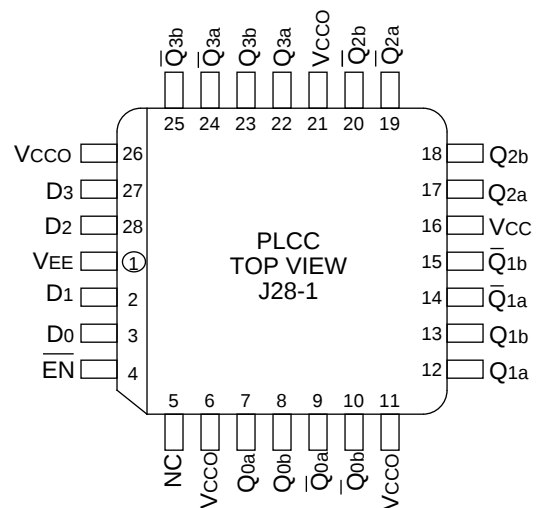
DESCRIPTION

The SY10/100E112 are quad drivers designed for use in new, high-performance ECL systems. The E112 has two pairs of OR/NOR outputs from each gate and a common, buffered enable input. The data input can also be used as an ECL memory address fan-out driver, although the E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the SY10/100E212 device.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0-D3	Data Inputs
$\overline{EN}$	Enable Input
Q _{na} , Q _{nb}	True Outputs
$\overline{Q}_{na}$, $\overline{Q}_{nb}$	Inverting Outputs
VCCO	Vcc to Output

TRUTH TABLE

$\overline{\text{EN}}$	Q_n	$\overline{\text{Q}}_n$
L	D_n	$\overline{\text{D}}_n$
H	H	L

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
	$\overline{\text{EN}}$ D	—	—	200	—	—	200	—	—	200	—	—	200	
I_{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	—	—	—	mA
	10E	—	47	56	—	47	56	—	47	56	—	47	56	
	100E	—	47	56	—	47	56	—	47	56	—	54	65	

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output D $\overline{\text{EN}}$	200 275	400 450	600 675	200 275	400 450	600 675	200 275	400 450	600 675	200 275	400 450	600 675	ps
t_{skew}	Within-Device Skew D_n to Q_n , $\overline{\text{Q}}_n^{(1)}$ Q_{na} to $\text{Q}_{nb}^{(2)}$	— —	80 40	— —	— —	80 40	— —	— —	80 40	— —	— —	80 40	— —	
t_r t_f	Rise/Fall Time 20% to 80%	275	425	700	275	425	700	275	425	700	275	425	700	ps

NOTES:

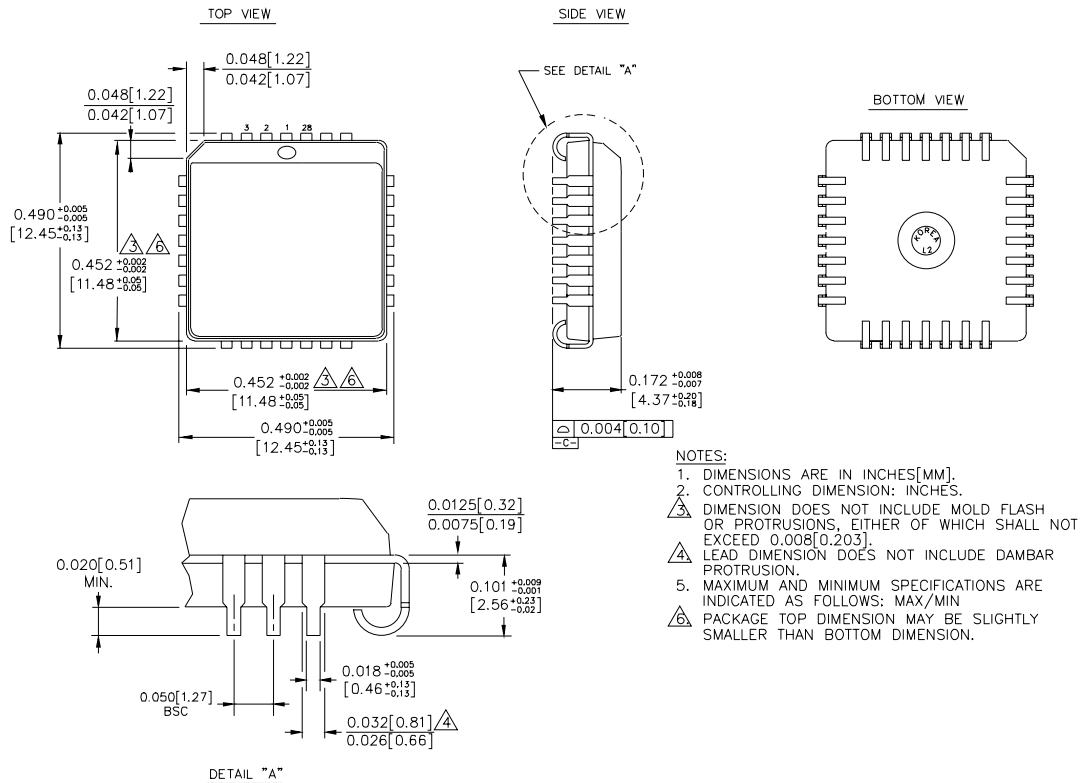
1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E112JC	J28-1	Commercial
SY10E112JCTR	J28-1	Commercial
SY100E112JC	J28-1	Commercial
SY100E112JCTR	J28-1	Commercial

Ordering Code	Package Type	Operating Range
SY10E112JI	J28-1	Industrial
SY10E112JITR	J28-1	Industrial
SY100E112JI	J28-1	Industrial
SY100E112JITR	J28-1	Industrial

28 LEAD PLCC (J28-1)



Rev. 03

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