DIFFERENTIAL PECL-to-TTL TRANSLATOR

FEATURES

- **2.5ns typical propagation delay**
- **Low power**
- **Differential PECL inputs**
- **24mA TTL outputs**
- **Flow-through pinouts**
- **Available in 8-pin SOIC package**

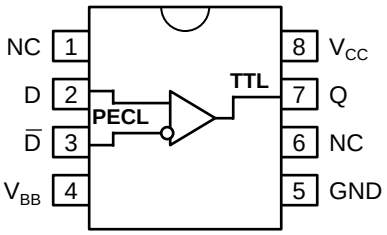
DESCRIPTION

The SY10/100ELT21 are single differential PECL-to-TTL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and low skew single gate design make the ELT21 ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

The V_{BB} output allow differential single-ended, or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to V_{CC} with a 0.01µF capacitor.

The ELT21 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
Q	TTL Output
D, /D	Differential PECL Inputs
V_{CC}	+5.0V Supply
V_{BB}	Reference Output
GND	Ground

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_I	PECL Input Voltage	0V to V_{CC}+0.5	V
V_O	Voltage Applied to Output at HIGH State	–0.5 to +5.5	V
I_O	Current Applied to Output at LOW State	Twice the Rated I_{OL}	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–40 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	/D	Q
L	H	L
H	L	H
Open	Open	L

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 5.25V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I_{OS}	Output Short Circuit Current	–80	–200	–80	–200	–80	—	–200	–80	–200	mA	V_{OUT} = 0V
I_{CC}	Power Supply Current	—	20	—	20	—	14	20	—	20	mA	—
V_{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	— —	2.5 2.0	— —	V V	I_{OH} = –3.0mA I_{OH} = –15mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	—	0.5	—	0.5	V	I_{OL} = 24mA

PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 5.25V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I_{IH}	Input HIGH Current	—	150	—	150	—	—	150	—	150	µA	
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	—	0.5	—	µA	
V_{IH}	Input HIGH Voltage(2) 10ELT 100ELT	3770 3835	4110 4120	3830 3835	4160 4120	3870 3835	—	4190 4120	3940 3835	4280 4120	mV	
V_{IL}	Input LOW Voltage(2) 10ELT 100ELT	3050 3190	3500 3525	3050 3190	3520 3525	3050 3190	— —	3520 3525	3050 3190	3555 3525	mV	
V_{BB}	Reference Output(2) 10ELT 100ELT	3570 3620	3700 3740	3620 3620	3730 3740	3650 3620	— —	3750 3740	3690 3620	3810 3740	mV	

NOTES:

1. These values are for V_{cc} = 5.0V. Level Specifications will vary 1:1 V_{cc}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 5.25V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Output Q	2.0	3.0	2.0	3.0	2.0	—	3.0	2.0	3.0	ns	C_L = 50pF
t_{skpp}	Part-to-Part Skew(1, 2)	—	0.5	—	0.5	—	—	0.5	—	0.5	ns	C_L = 50pF
f_{MAX}	Maximum Input Frequency (2, 3, 4)	160	—	160	—	160	—	—	160	—	MHz	C_L = 50pF
V_{CMR}	Common Mode Range	2.4	V_{CC}	2.4	V_{CC}	2.4	—	V_{CC}	2.4	V_{CC}	V	
V_{PP}	Minimum Peak-to-Peak Input(5)	200	—	200	—	200	—	—	200	—	mV	
t_r t_f	Output Rise/Fall Time (1.0V to 2.0V)	—	1.5	—	1.5	—	—	1.5	—	1.5	ns	C_L = 50pF

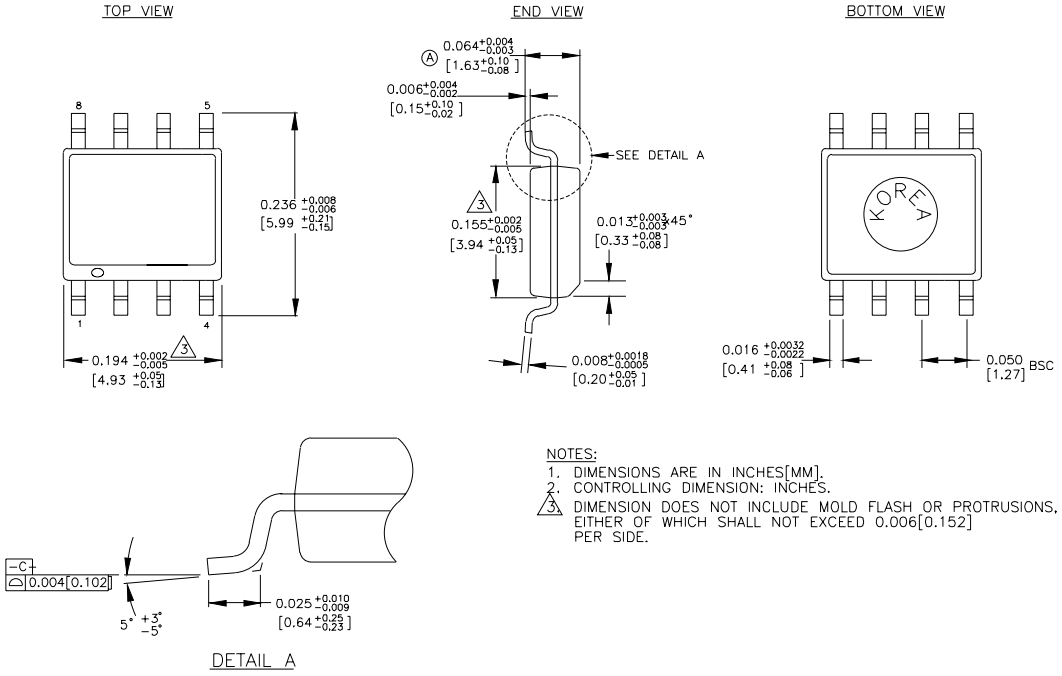
NOTES:

1. Part-to-Part Skew considering HIGH-to-HIGH transitions at common V_{CC} levels.
2. These parameters are guaranteed, but not tested.
3. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
4. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
5. 200mV input guarantees full logic at output.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Vcc Range (V)
SY10ELT21ZC	Z8-1	Commercial	+4.75 to +5.25
SY10ELT21ZCTR	Z8-1	Commercial	+4.75 to +5.25
SY100ELT21ZC	Z8-1	Commercial	+4.75 to +5.25
SY100ELT21ZCTR	Z8-1	Commercial	+4.75 to +5.25

8 LEAD SOIC .150" WIDE (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

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MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB http://www.micrel.com