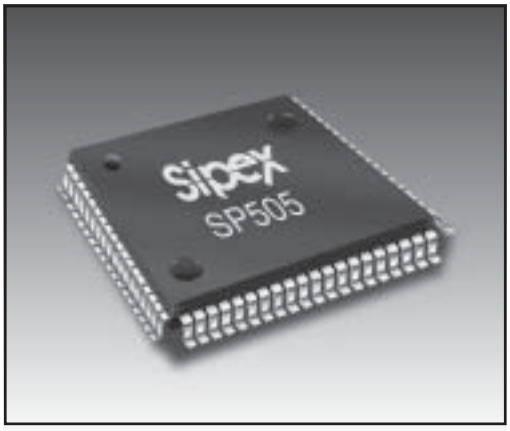
WAN Multi-Mode Serial Transceiver

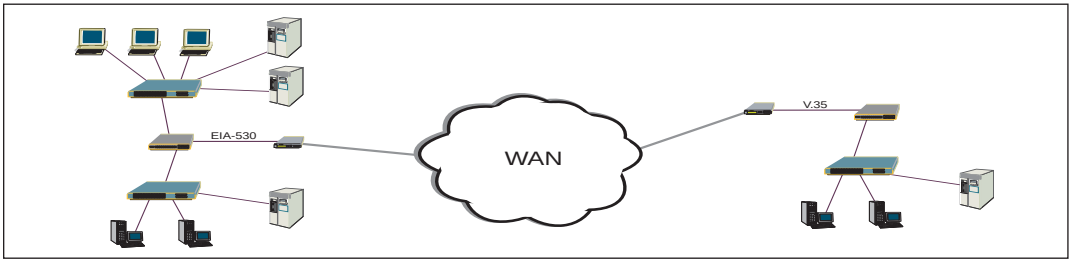
- +5V Only Operation
- Seven (7) Drivers and Seven (7) Receivers
- Driver and Receiver Tri-state Control
- Internal Transceiver Termination Resistors for V.11 and V.35 Protocols
- Loopback Self-Test Mode
- Software Selectable Protocol Selection
- Interface Modes Supported:
  - ✓ RS-232 **(V.28)**
  - ✓ X.21/RS-422 **(V.11)**
  - ✓ EIA-530 **(V.10 & V.11)**
  - ✓ EIA-530A **(V.10 & V.11)**
  - ✓ RS-449 **(V.10 & V.11)**
  - ✓ V.35 **(V.35 & V.28)**
  - ✓ V.36 **(V.10 & V.11)**
  - ✓ RS-485 **(un-terminated V.11)**
- Improved ESD Tolerance for Analog I/Os
- High Differential Transmission Rates
  - ➥ SP505A - 10Mbps
  - ➥ SP505B - over 16Mbps
- Compliant to NET1/2 and TBR2 Physical Layer Requirements
  (TUV Test Report NET2/052101/98)
  (TUV Test Report CTR2/052101/98)



DESCRIPTION...

The **SP505** is a monolithic device that supports eight (8) popular serial interface standards for DTE to DCE connectivity. The **SP505** is fabricated using a low power BiCMOS process technology, and incorporates a Sipex patented (5,306,954) charge pump allowing +5V only operation. Seven (7) drivers and seven (7) receivers can be configured via software for any of the above interface modes at any time. The **SP505** requires no additional external components for compliant operation for all of the eight (8) modes of operation. All necessary termination is integrated within the **SP505** and is switchable when V.35 drivers, V.35 receivers, and V.11 receivers are used. The **SP505** can operate as either a DTE or DCE.

Additional features with the **SP505** include internal loopback that can be initiated in either single-ended or differential modes. While in loopback mode, driver outputs are internally connected to receiver inputs creating an internal signal path convenient for diagnostic testing. This eliminates the need for an external loopback plug. The **SP505** also includes a latch enable pin with the driver and receiver address decoder. Tri-state ability for the driver and receiver outputs is controlled by supplying a 4-bit word into the address decoder. Seven (7) drivers and one (1) receiver in the **SP505** include separate enable pins for added convenience. The **SP505** is ideal for WAN serial ports in networking equipment such as routers, switches, DSU/CSU's, and other access devices.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....+7V
Input Voltages:
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....-0.3V to (V_{CC}+0.5V)
Receivers.....±15.5V
Output Voltages:
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....±15V
Receivers.....-0.3V to (V_{CC}+0.5V)
Storage Temperature.....-65˚C to +150˚C
Power Dissipation.....2000mW
Package Derating:
$ø_{JA}$.....46 °C/W
$ø_{JC}$.....16 °C/W

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 80-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order remove moisture prior to soldering. Sipex ships the 80-pin QFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= –3.2mA
V_{OH}	2.4			Volts	I_{OUT}= 1.0mA
V.28 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±15	Volts	per Figure 1
Loaded Voltage	±5.0		±15	Volts	per Figure 2
Short-Circuit Current			±100	mA	per Figure 4
Power-Off Impedance	300			Ω	per Figure 5
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			1.5	µs	per Figure 6; +3V to -3V
Instantaneous Slew Rate			30	V/µs	per Figure 3
Propagation Delay					
t_{PHL}	0.5	1	5	µs	
t_{PLH}	0.5	1	5	µs	
Max.Transmission Rate	120	230		kbps	
V.28 RECEIVER					
DC Parameters					
Inputs					
Input Impedance	3		7	kΩ	per Figure 7
Open-Circuit Bias			+2.0	Volts	per Figure 8
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	50	100	500	ns	
t_{PLH}	50	100	500	ns	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.28 RECEIVER (continued)					
AC Parameters (cont.)					
Max.Transmission Rate	120	230		kbps	
V.10 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage	±4.0		±6.0	Volts	per Figure 9
Test-Terminated Voltage	$0.9V_{OC}$			Volts	per Figure 10
Short-Circuit Current			±150	mA	per Figure 11
Power-Off Current			±100	µA	per Figure 12
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			200	ns	per Figure 13; 10% to 90%
Propagation Delay					
t_{PHL}	50	100	500	ns	
t_{PLH}	50	100	500	ns	
Max.Transmission Rate	120			kbps	
V.10 RECEIVER					
DC Parameters					
Inputs					
Input Current	–3.25		+3.25	mA	per Figures 14 and 15
Input Impedance	4			kΩ	
Sensitivity			±0.3	Volts	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	50	120	250	ns	
t_{PLH}	50	120	250	ns	
Max.Transmission Rate	120			kbps	
V.11 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±5.0	Volts	per Figure 16
Test Terminated Voltage	±2.0			Volts	per Figure 17
	$0.5V_{OC}$		$0.67V_{OC}$	Volts	
Balance			±0.4	Volts	per Figure 17
Offset			+3.0	Volts	per Figure 17
Short-Circuit Current			±150	mA	per Figure 18
Power-Off Current			±100	µA	per Figure 19
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			20	ns	per Figures 21 and 36; 10% to 90%
Propagation Delay					
t_{PHL}	50	85	110	ns	per Figures 33 and 36, C_L = 50pF
t_{PLH}	50	85	110	ns	per Figures 33 and 36, C_L = 50pF
Differential Skew		10	20	ns	per Figures 33 and 36, C_L = 50pF
Max.Transmission Rate					per Figure 33, C_L = 50pF
SP505ACF	10	12		Mbps	f_{IN} = 5MHz
SP505BCF	16.4	18		Mbps	f_{IN} = 8.2MHz
V.11 RECEIVER					
DC Parameters					
Inputs					
Common Mode Range	–7		+7	Volts	
Sensitivity			±0.3	Volts	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.11 RECEIVER (continued)					
DC Parameters (cont.)					
Input Current	–3.25		±3.25	mA	per Figure 20 and 22
Current w/ 100 Termination			±60.75	mA	per Figure 23 and 24
Input Impedance	4			kΩ	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	80	110	130	ns	per Figures 33 and 38; C_L = 50pF
t_{PLH}	80	110	130	ns	per Figures 33 and 38; C_L = 50pF
Differential Skew		20		ns	per Figure 33; C_L = 50pF
Max.Transmission Rate					per Figure 33; C_L = 50pF
SP505ACF	10	12		Mbps	f_{IN} = 5MHz
SP505BCF	16.4	18		Mbps	f_{IN} = 8.2MHz
V.35 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±1.20	Volts	per Figure 16
Test Terminated Voltage	±0.44		±0.66	Volts	per Figure 25
Offset			±0.6	Volts	per Figure 25
Source Impedance	50		150	Ω	per Figure 27; $Z_S = V_2/V_1 \times 50$
Short-Circuit Impedance	135		165	Ω	per Figure 28
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time		30	40	ns	per Figure 29; 10% to 90%
Propagation Delay					
t_{PHL}	50	90	110	ns	per Figures 33 and 36; C_L = 20pF
t_{PLH}	50	90	110	ns	per Figures 33 and 36; C_L = 20pF
Differential Skew		20	30	ns	per Figures 33 and 36; C_L = 20pF
Max.Transmission Rate					per Figure 33; C_L = 20pF
SP505ACF	10	12		Mbps	f_{IN} = 5MHz
SP505BCF	16.4	18		Mbps	f_{IN} = 8.2MHz
V.35 RECEIVER					
DC Parameters					
Inputs					
Sensitivity		±80		mV	
Source Impedance	90		110	Ω	per Figure 30; $Z_S = V_2/V_1 \times 50$
Short-Circuit Impedance	135		165	Ω	per Figure 31
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	80	110	130	ns	per Figures 33 and 38; C_L = 20pF
t_{PLH}	80	110	130	ns	per Figures 33 and 38; C_L = 20pF
Differential Skew		20		ns	per Figure 33; C_L = 20pF
Max.Transmission Rate					per Figure 33; C_L = 20pF
SP505ACF	10	12		Mbps	f_{IN} = 5MHz
SP505BCF	16.4	18		Mbps	f_{IN} = 8.2MHz
TRANSCEIVER LEAKAGE CURRENTS					
Driver Output 3-State Current		100	500	µA	per Figure 32; Drivers disabled
Rcvr Output 3-State Current		1	10	µA	DEC_X = 0000, 0.4V V_O 2.4V

OTHER AC CHARACTERISTICS

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.70	5.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.40	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.40	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.15	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.20	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 100pF, Fig. 34 & 40; S_2 closed
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		2.80	10.0	µs	C_L = 100pF, Fig. 34 & 37; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 34 & 37; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		2.60	10.0	µs	C_L = 100pF, Fig. 34 & 37; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 34 & 37; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 15pF, Fig. 34 & 37; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL}; Tri-state to Output LOW		0.12	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed
RS-423/V.10					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 38; S_2 closed

OTHER AC CHARACTERISTICS (Continued)

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-422/V.11					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_2 closed
V.35					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 35 & 39; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 35 & 39; S_2 closed
TRANSCEIVER TO TRANSCEIVER SKEW		(per Figures 33, 36, 38)			
V.28 Driver		100		ns	$\lvert (t_{phl})_{Tx1} - (t_{phl})_{Tx6,7} \rvert$
		100		ns	$\lvert (t_{plh})_{Tx1} - (t_{plh})_{Tx6,7} \rvert$
V.28 Receiver		20		ns	$\lvert (t_{phl})_{Rx1} - (t_{phl})_{Rx2,7} \rvert$
		20		ns	$\lvert (t_{phl})_{Rx1} - (t_{phl})_{Rx2,7} \rvert$
V.11 Driver		2		ns	$\lvert (t_{phl})_{Tx1} - (t_{phl})_{Tx6,7} \rvert$
		2		ns	$\lvert (t_{plh})_{Tx1} - (t_{plh})_{Tx6,7} \rvert$
V.11 Receiver		3		ns	$\lvert (t_{phl})_{Rx1} - (t_{phl})_{Rx2,7} \rvert$
		3		ns	$\lvert (t_{phl})_{Rx1} - (t_{phl})_{Rx2,7} \rvert$
V.10 Driver		5		ns	$\lvert (t_{phl})_{Tx2} - (t_{phl})_{Tx3,4,5} \rvert$
		5		ns	$\lvert (t_{plh})_{Tx2} - (t_{plh})_{Tx3,4,5} \rvert$
V.10 Receiver		5		ns	$\lvert (t_{phl})_{Rx2} - (t_{phl})_{Rx3,4,5} \rvert$
		5		ns	$\lvert (t_{phl})_{Rx2} - (t_{phl})_{Rx3,4,5} \rvert$
V.35 Driver		4		ns	$\lvert (t_{phl})_{Tx1} - (t_{phl})_{Tx6,7} \rvert$
		4		ns	$\lvert (t_{plh})_{Tx1} - (t_{plh})_{Tx6,7} \rvert$
V.35 Receiver		6		ns	$\lvert (t_{phl})_{Rx1} - (t_{phl})_{Rx2,7} \rvert$
		6		ns	$\lvert (t_{phl})_{Rx1} - (t_{phl})_{Rx2,7} \rvert$

POWER REQUIREMENTS

PARAMETER		MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{CC}		4.75	5.00	5.25	Volts	
I_{CC}	(No Mode Selected)		30		mA	All I_{CC} values are with V_{CC} = +5V, T = +25ºC, all drivers are loaded to their specified maximum load and all drivers are active at their maximum specified data transmission rates.
	(V.28/RS-232)		60		mA	
	(V.11/RS-422)		300		mA	
	(RS-449)		250		mA	
	(V.35)		105		mA	
	EIA-530		260		mA	
	EIA-530A		250		mA	
	V.36		65		mA	

TEST CIRCUITS...

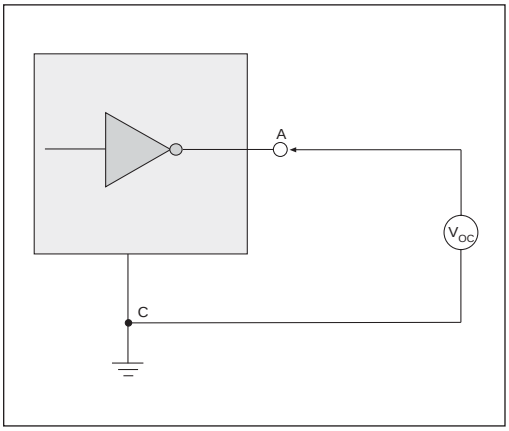


Figure 1. V.28 Driver Output Open Circuit Voltage

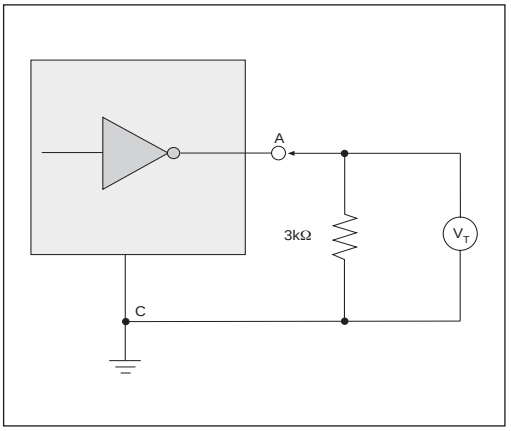


Figure 2. V.28 Driver Output Loaded Voltage

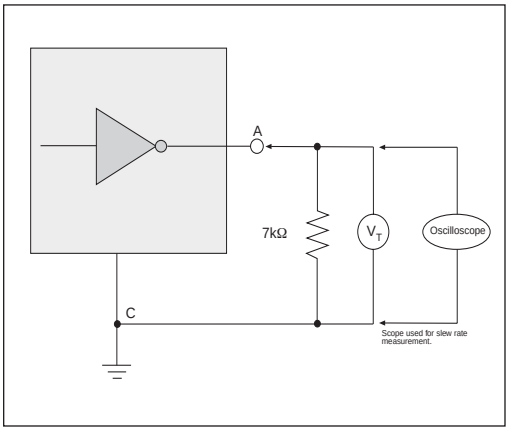


Figure 3. V.28 Driver Output Slew Rate

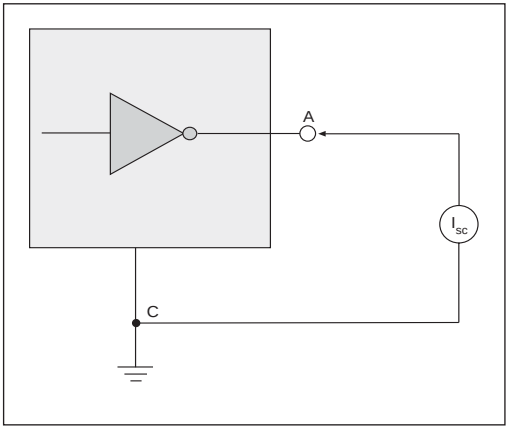


Figure 4. V.28 Driver Output Short-Circuit Current

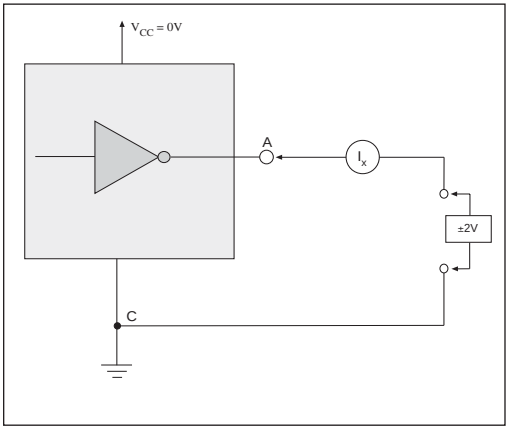


Figure 5. V.28 Driver Output Power-Off Impedance

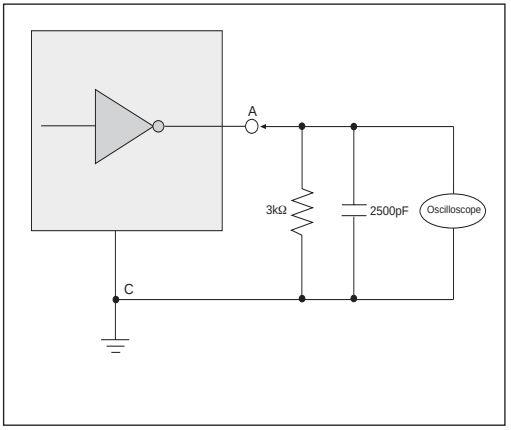


Figure 6. V.28 Driver Output Rise/Fall Times

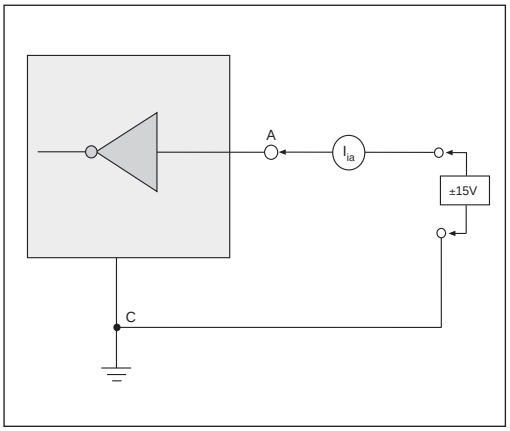


Figure 7. V.28 Receiver Input Impedance

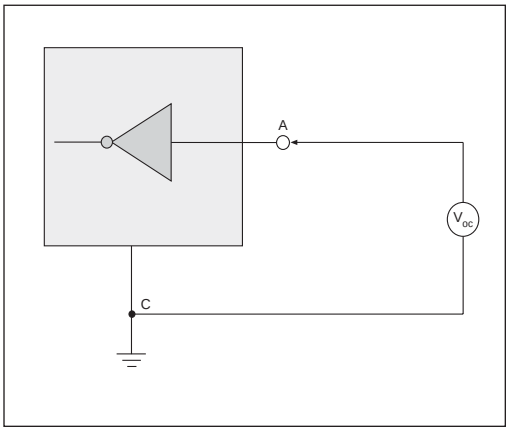


Figure 8. V.28 Receiver Input Open Circuit Bias

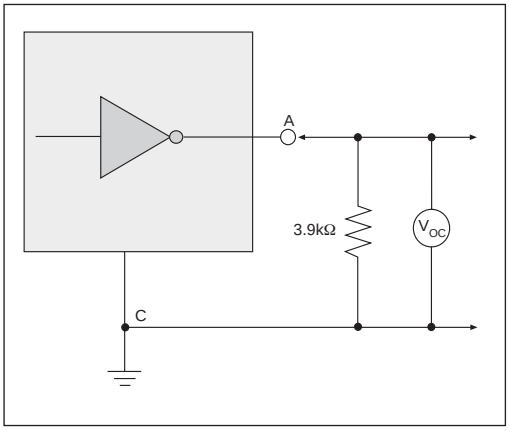


Figure 9. V.10 Driver Output Open-Circuit Voltage

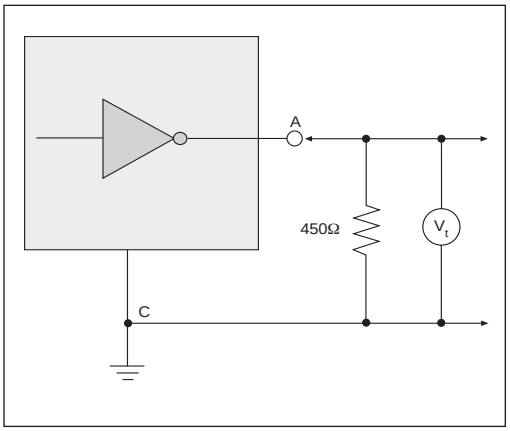


Figure 10. V.10 Driver Output Test Terminated Voltage

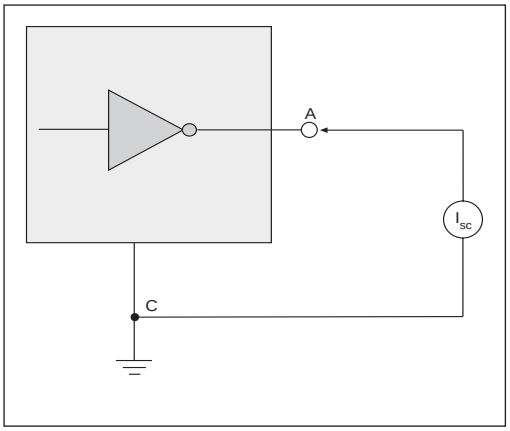


Figure 11. V.10 Driver Output Short-Circuit Current

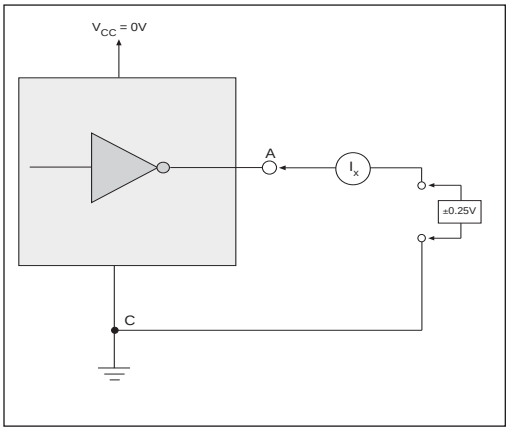


Figure 12. V.10 Driver Output Power-Off Current

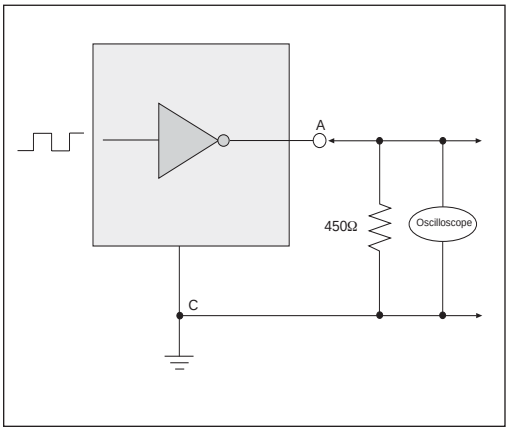


Figure 13. V.10 Driver Output Transition Time

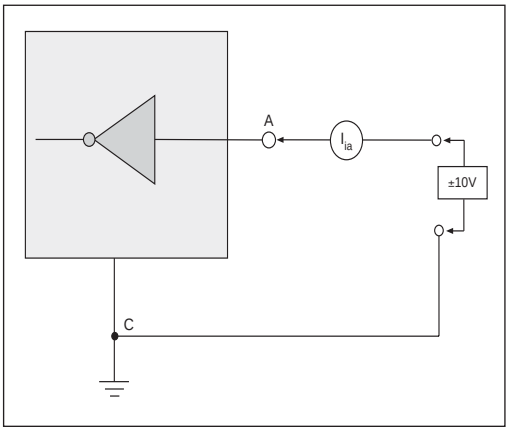


Figure 14. V.10 Receiver Input Current

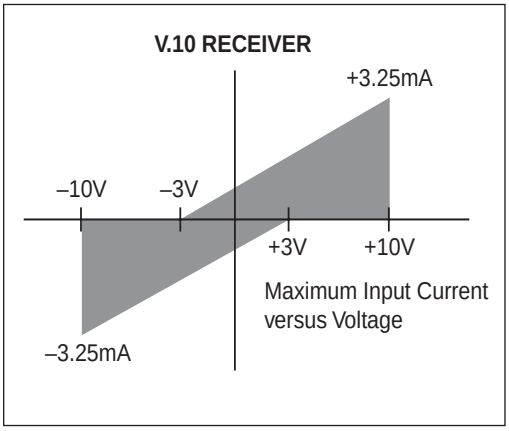


Figure 15. V.10 Receiver Input IV Graph

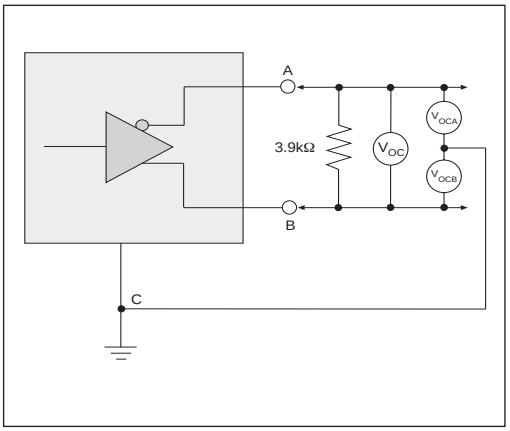


Figure 16. V.11 and V.35 Driver Output Open-Circuit Voltage

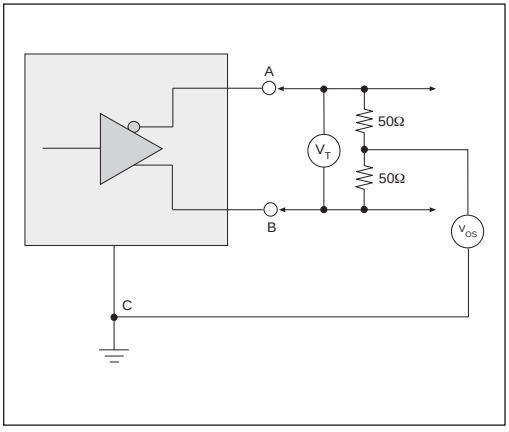


Figure 17. V.11 Driver Output Test Terminated Voltage

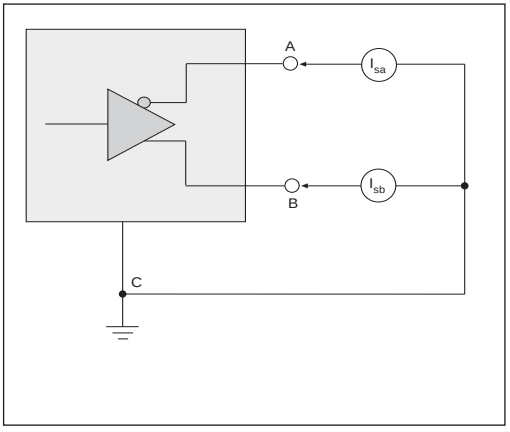


Figure 18. V.11 Driver Output Short-Circuit Current

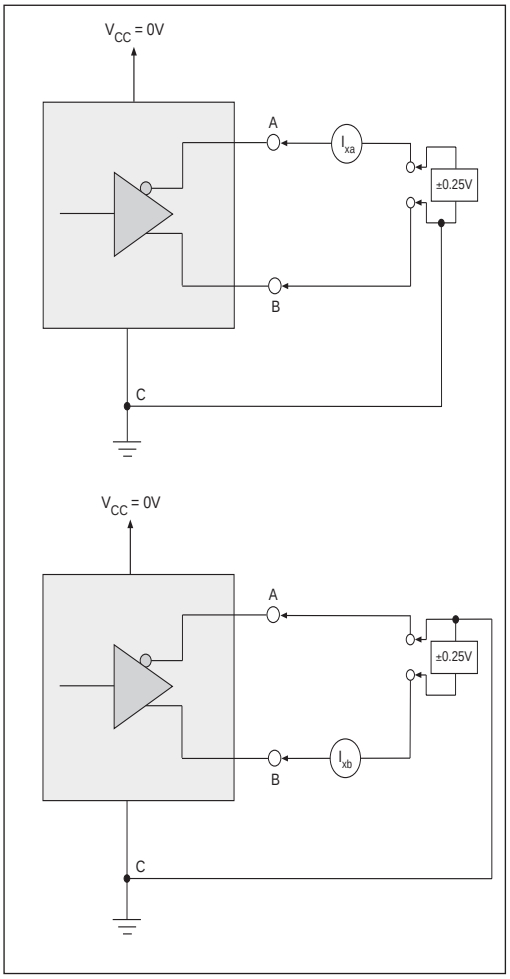


Figure 19. V.11 Driver Output Power-Off Current

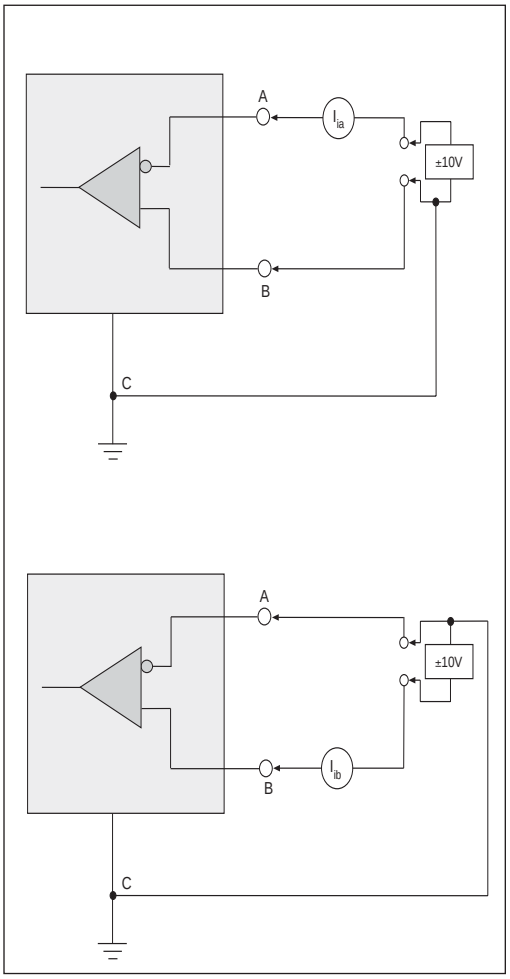


Figure 20. V.11 Receiver Input Current

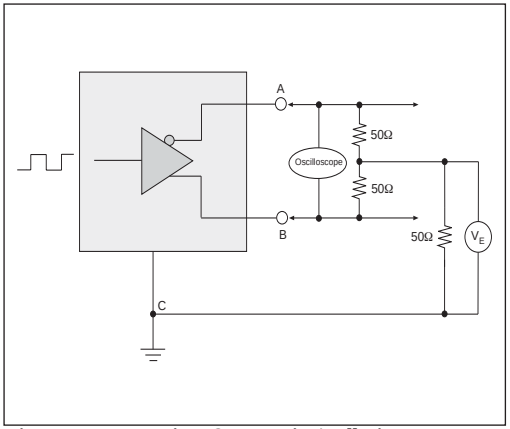


Figure 21. V.11 Driver Output Rise/Fall Time

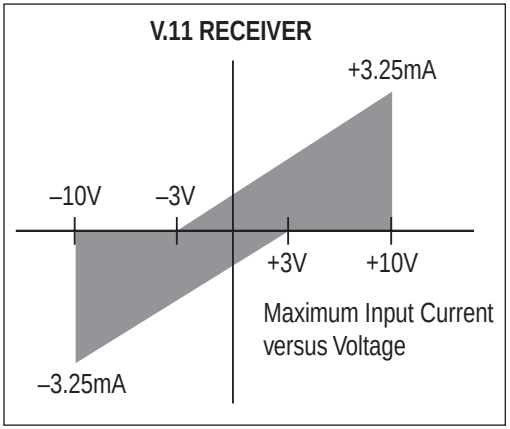


Figure 22. V.11 Receiver Input IV Graph

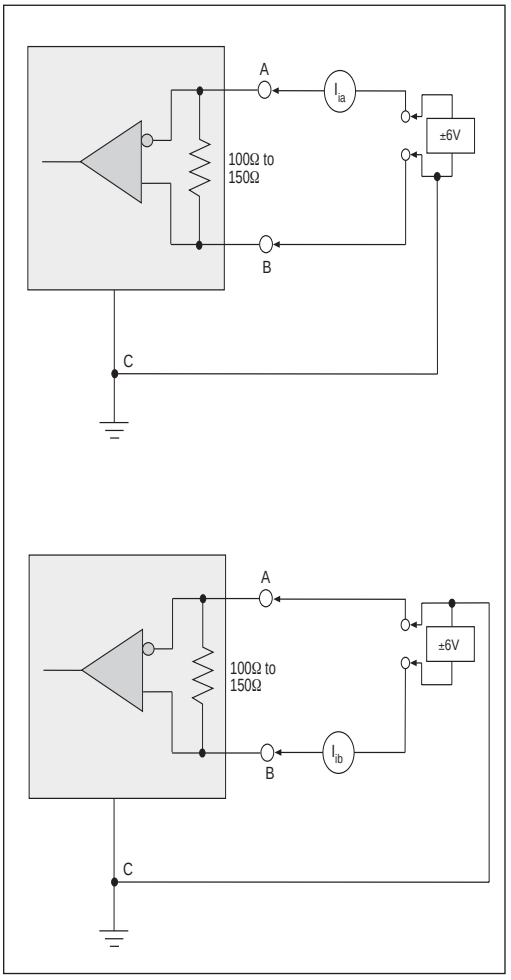


Figure 23. V.11 Receiver Input Current w/ Termination

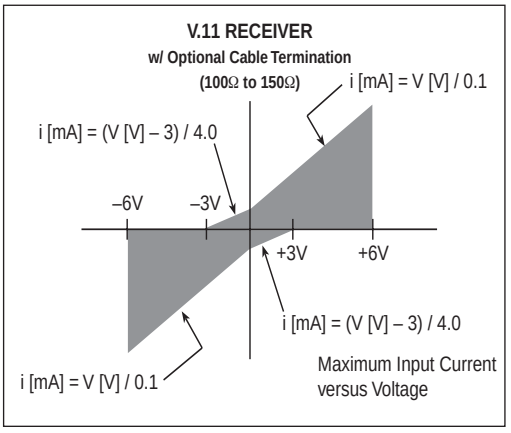


Figure 24. V.11 Receiver Input Graph w/ Termination

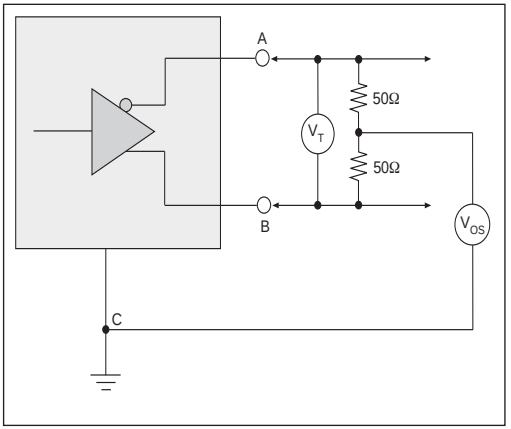


Figure 25. V.35 Driver Output Test Terminated Voltage

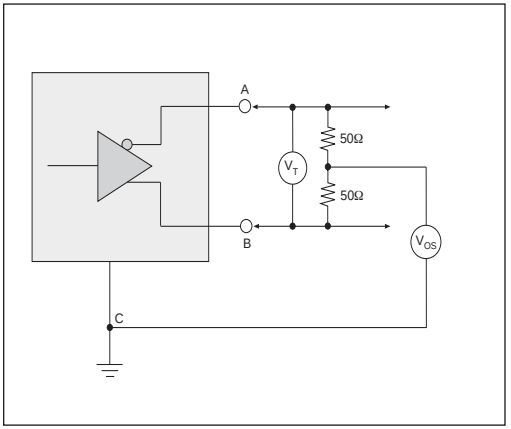


Figure 26. V.35 Driver Output Offset Voltage

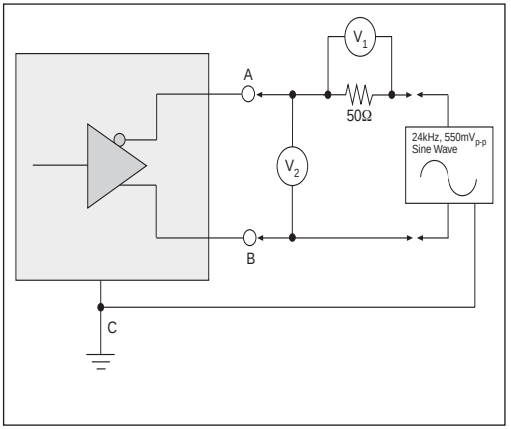


Figure 27. V.35 Driver Output Source Impedance

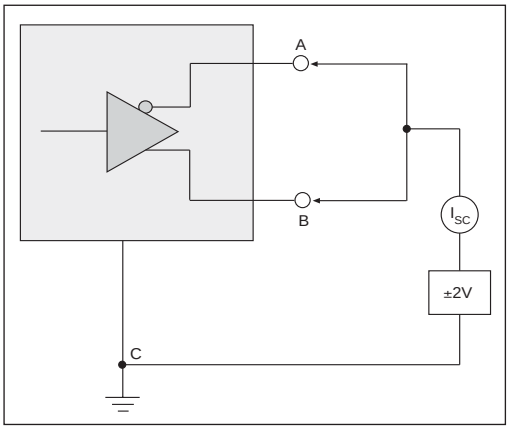


Figure 28. V.35 Driver Output Short-Circuit Impedance

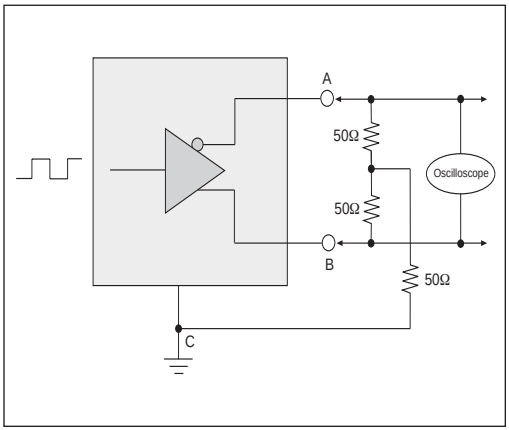


Figure 29. V.35 Driver Output Rise/Fall Time

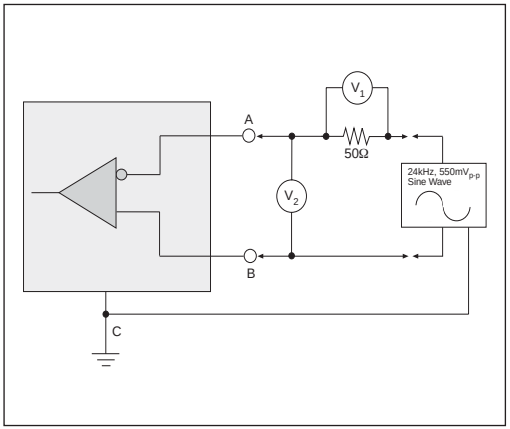


Figure 30. V.35 Receiver Input Source Impedance

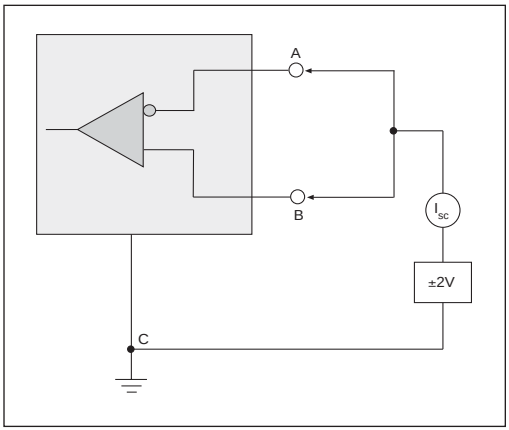


Figure 31. V.35 Receiver Input Short-Circuit Impedance

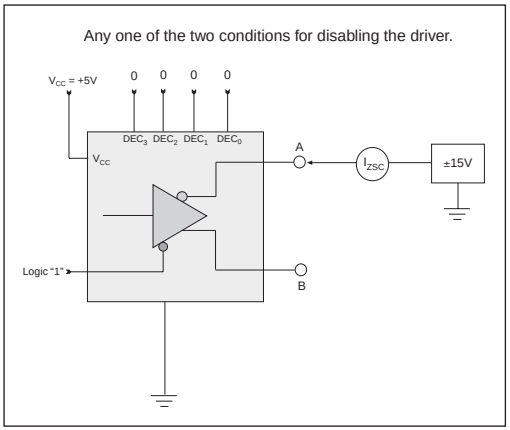


Figure 32. Driver Output Leakage Current Test

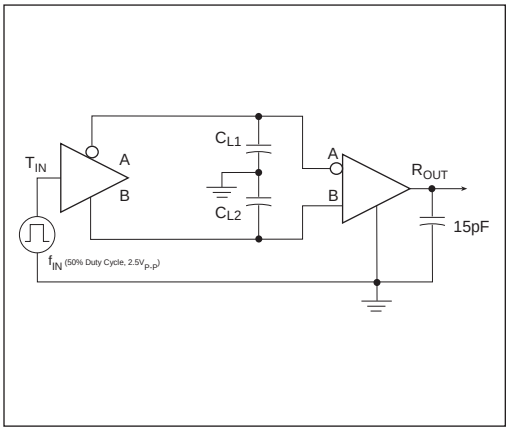


Figure 33. Driver/Receiver Timing Test Circuit

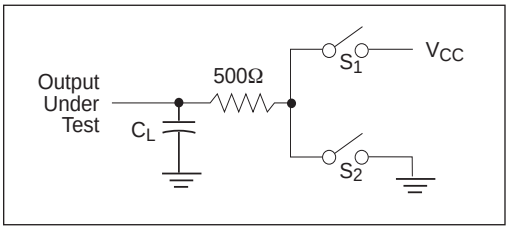


Figure 34. Driver Timing Test Load Circuit

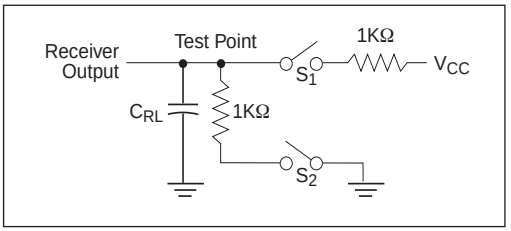


Figure 35. Receiver Timing Test Load Circuit

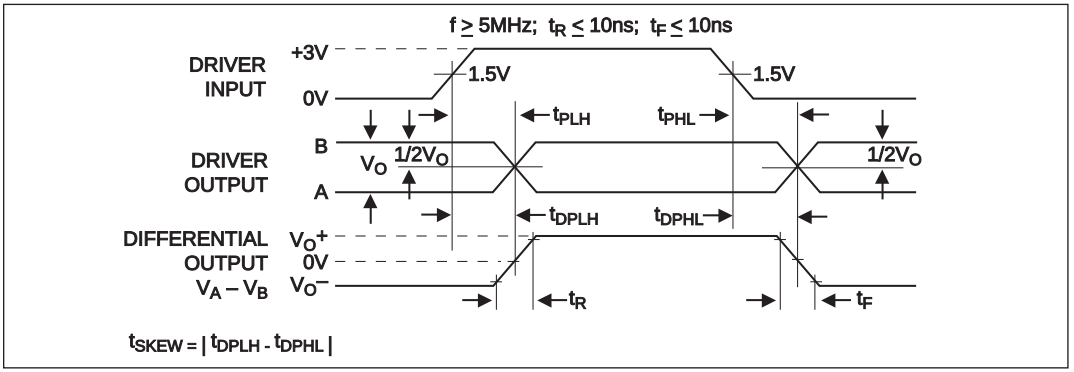


Figure 36. Driver Propagation Delays

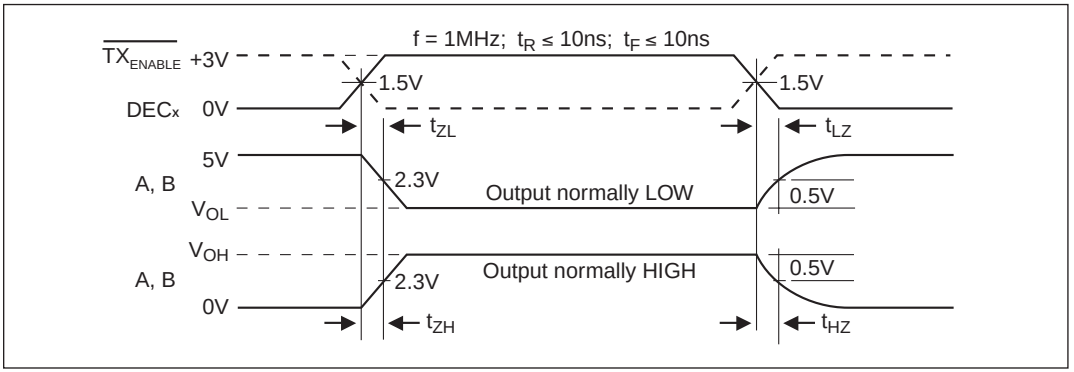


Figure 37. Driver Enable and Disable Times

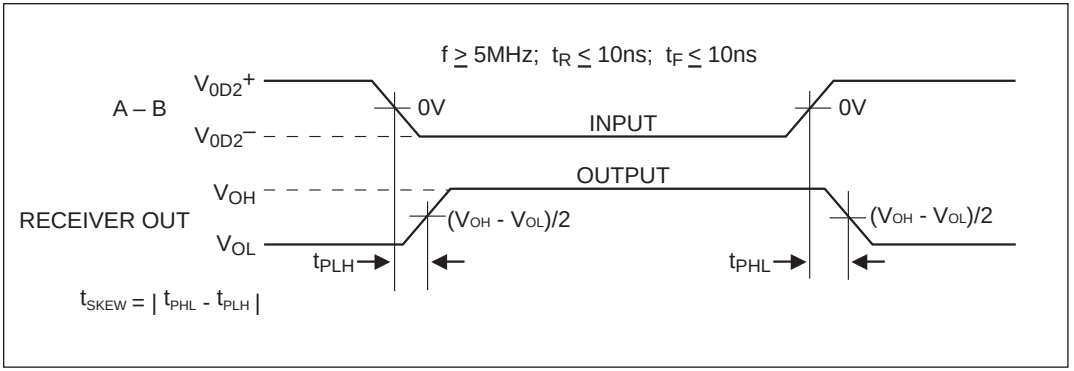


Figure 38. Receiver Propagation Delays

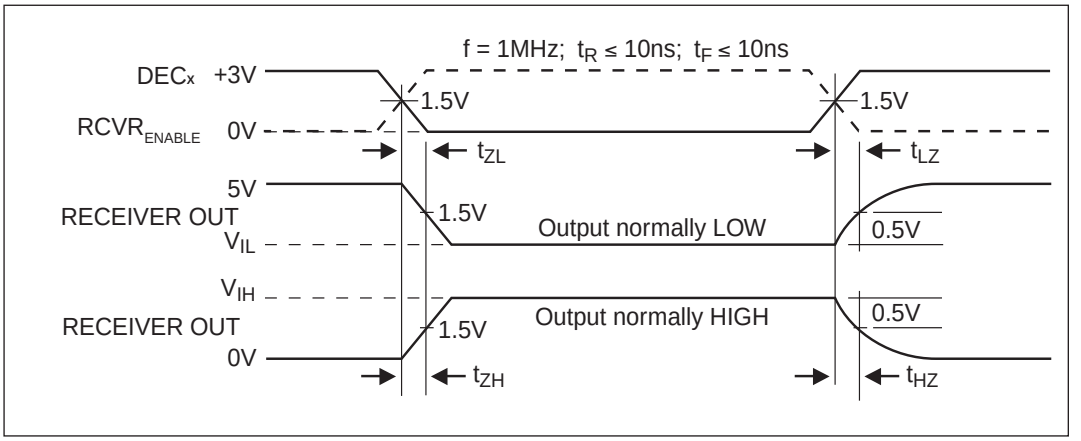


Figure 39. Receiver Enable and Disable Times

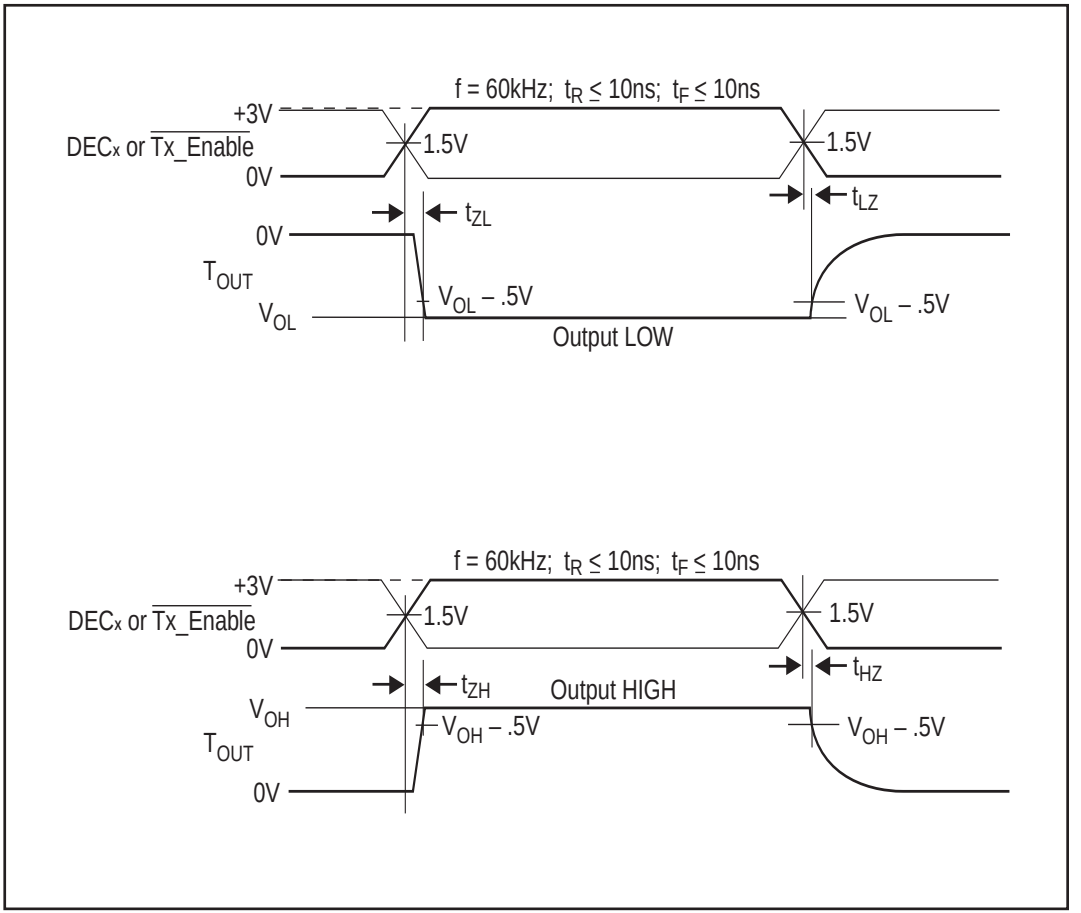


Figure 40. V.28 (RS-232) and V.10 (RS-423) Driver Enable and Disable Times

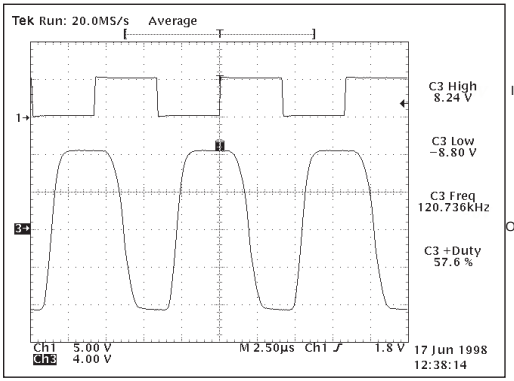


Figure 41. Typical V.28 Driver Output Waveform

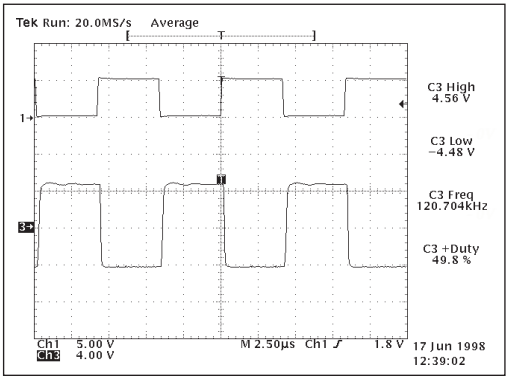


Figure 42. Typical V.10 Driver Output Waveform

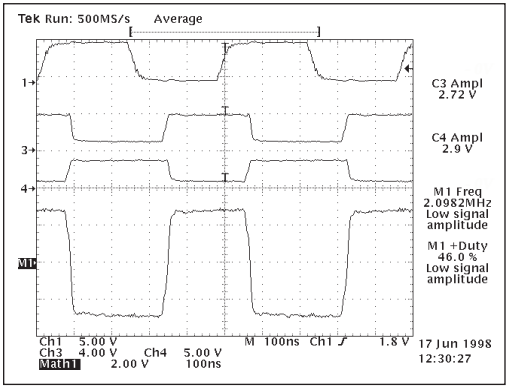


Figure 43. Typical V.11 Driver Output Waveform

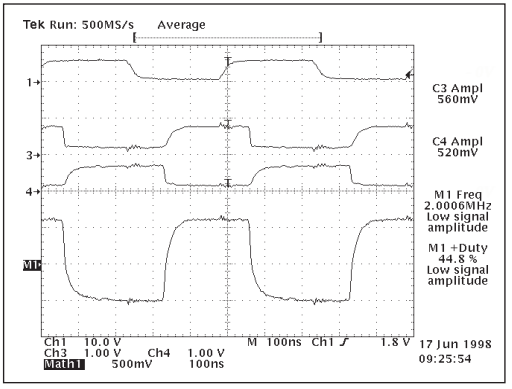
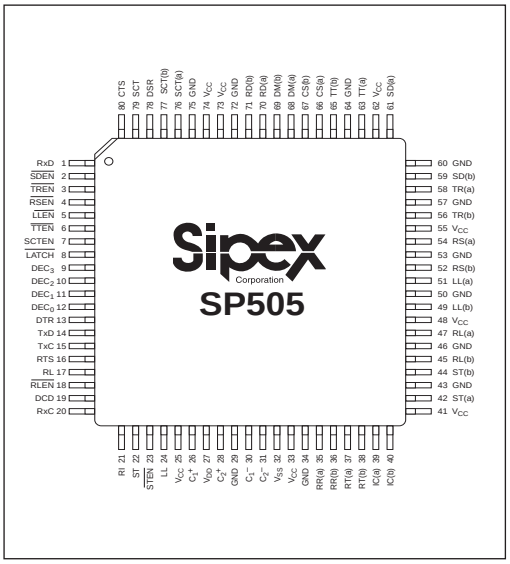


Figure 44. Typical V.35 Driver Output Waveform

PINOUT…



PIN ASSIGNMENTS…
CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non–inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit: analog input, non–inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a)— Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b)— Incoming Call; analog input,non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2 — $\overline{SDEN}$ — Enables TxD driver, active low; TTL input.

Pins 3 — $\overline{TREN}$ — Enables DTR driver, active low; TTL input.

Pins 4 — $\overline{RSEN}$ — Enables RTS driver, active low; TTL input.

Pins 5 — $\overline{LLEN}$ — Enables LL driver, active low; TTL input.

Pin 6 — $\overline{TTEN}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pin 8 — $\overline{LATCH}$ — Latch control for decoder bits (pins 9-12), active low. Logic high input will make decoder transparent.

Pins 12–9 — DEC_0 – DEC_3 — Transmitter and receiver decode register; configures transmitter and receiver modes; TTL inputs.

Pin 18 — $\overline{RLEN}$ — Enables RL driver; active low; TTL input.

Pin 23 — $\overline{STEN}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22µF, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22µF, 16V.

Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^-. Suggested capacitor size is 22µF, 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^-. Suggested capacitor size is 22µF, 16V.

FEATURES...

The **SP505** is a highly integrated serial transceiver that allows software control of its interface modes. Similar to the SP504, the **SP505** offers the same hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS-485, V.35, EIA-530 and includes V.36 and EIA-530A. The interface mode selection is done via a 4–bit switch for the drivers and receivers. The **SP505** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex**–patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin JEDEC Quad FlatPack package.

The **SP505** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The **SP505** has seven (7) independent drivers and seven (7) independent receivers. In V.35 mode, the **SP505** includes the necessary components and termination resistors internal within the device for compliant V.35 operation.

THEORY OF OPERATION

The **SP505** is made up of five separate circuit blocks — the charge pump, drivers, receivers, decoder and switching array. Each of these circuit blocks is described in more detail below.

Charge–Pump

The **SP505** charge pump is based on the SP504 design where **Sipex's** patented charge pump design (5,306,954) uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. The charge pump still requires external capacitors to store the charge. In addition the SP504 charge pump supplies ±10V or ±5V on V_{SS} and V_{DD} depending on the mode of operation. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

The **SP505** charge pump is used for RS-232 where the output voltage swing is typically ±10V and also used for RS-423. However, RS-423 requires the voltage swing on the driver output be between ±4V to ±6V during an open-circuit (no load). The charge pump would need to be regulated down from ±10V to ±5V. A typical ±10V charge pump would require external clamping such as 5V zener diodes on V_{DD} and V_{SS} to ground. The ±5V output has symmetrical levels as in the ±10V output. The ±5V is used in the following modes where RS-423 (V.10) are used: RS-449, EIA-530, EIA-530A and V.36.

Phase 1 (±10V)

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 1 (±5V)

— V_{SS} & V_{DD} charge storage and transfer — With the C_1 and C_2 capacitors initially charged to +5V, C_1^+ is then switched to ground and the charge on C_1^- is transferred to the V_{SS} storage capacitor. Simultaneously the C_2^- is switched to ground and 5V charge on C_2^+ is transferred to the V_{DD} storage capacitor.

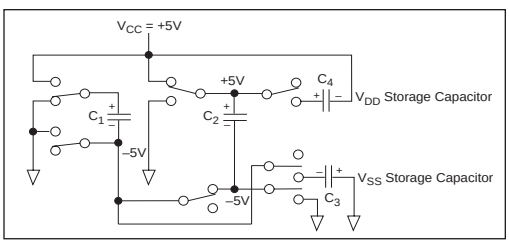


Figure 45. Charge Pump Phase 1 for ±10V.

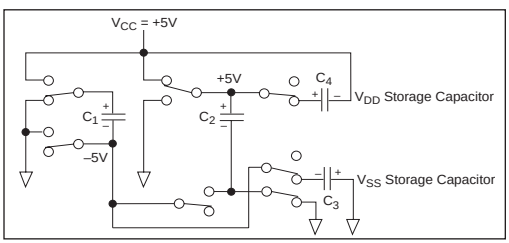


Figure 46. Charge Pump Phase 1 for ±5V.

Phase 2 (±10V)

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V or the generated –5V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 2 (±5V)

— V_{SS} & V_{DD} charge storage — C_1^+ is reconnected to V_{CC} to recharge the C_1 capacitor. C_2^+ is switched to ground and C_2^- is connected to C_3. The 5V charge from Phase 1 is now transferred to the V_{SS} storage capacitor. V_{SS} receives a continuous charge from either C_1 or C_2. With the C1 capacitor charged to 5V, the cycle begins again.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is l0V. For the 5V output, C_2^+ is connected to ground so that the potential on C_2 is only +5V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated l0V or the generated 5V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V_{DD} and V_{SS} are separately generated from V_{CC} in a no–load condition, V_{DD} and V_{SS} will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be a minimum of 22µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V^- pins. The value of the external supply voltages must be no greater than ±l0.5V. The tolerance should be ±5% from ±10V. The current drain for the supplies is used for RS-232 and RS-423 drivers. For the RS-232 driver, the current requirement will be 3.5mA per driver. The RS-423 driver worst case current drain will be 11mA per driver. Power sequencing is required for the SP505. The supplies must be sequenced accordingly: +10V, +5V and –10V. It is important to prevent V_{SS} from starting up before V_{CC} or V_{DD}.

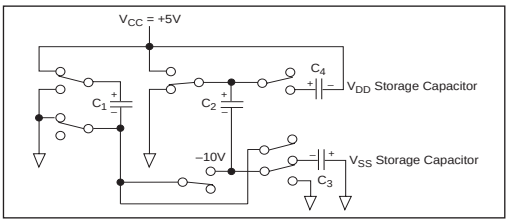


Figure 47. Charge Pump Phase 2 for ±10V.

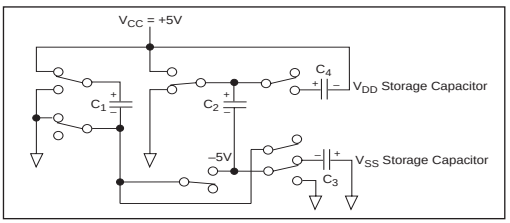


Figure 48. Charge Pump Phase 2 for ±5V.

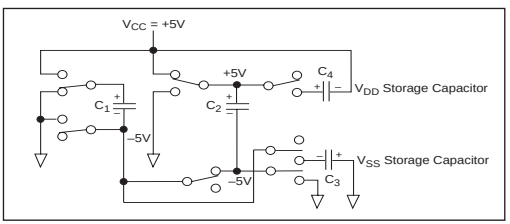


Figure 49. Charge Pump Phase 3.

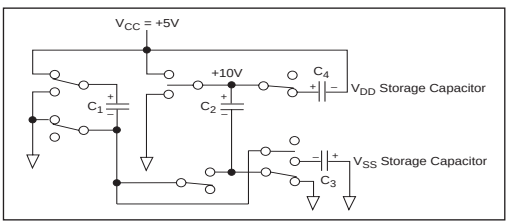


Figure 50. Charge Pump Phase 4.

Drivers

The **SP505** has seven (7) enhanced independent drivers. Control for the mode selection is done via a four–bit control word. The drivers are prearranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. *Table 1* shows the mode of each driver in the different interface modes that can be selected.

There are four basic types of driver circuits — V.28, V.11, V.10 and V.35.

V.28 Drivers

The V.28 drivers output single–ended signals with a minimum of ±5V (with 3kΩ & 2500pF loading), and can operate to at least 120kbps under full load. Since the **SP505** uses a charge pump to generate the RS-232 output rails, the driver outputs will never exceed ±10V. The V.28 drivers are used in RS-232 mode for all signals, and also in V.35 mode where four (4) drivers are used as the control line signals (DTR, RTS, LL, and RL).

V.10 Drivers

The V.10 (RS-423) drivers are also single–ended signals which produce open circuit V_{OL} and V_{OH} measurements of ±4.0V to ±6.0V. When terminated with a 450Ω load to ground, the driver output will not deviate more than 10% of the open circuit value. This is in compliance of the ITU V.10 specification. The V.10 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category II signals from each of their corresponding specifications.

V.11 Drivers

The third type of driver is a V.11 (RS-422) type differential driver. Due to the nature of differential signaling, the drivers are more immune to noise as opposed to single-ended transmission methods. The advantage is evident over high speeds and long transmission lines. The strength of the driver outputs can produce differential signals that can maintain typically ±2.2V differential output levels with a load of 100Ω. The signal levels and drive capability of these drivers allow the drivers to also support RS-485 requirements of ±1.5V minimum differential output levels with a 54Ω load. The driver is designed to operate over a common mode range of +12V to -7V, which follows the RS-485 specification. This also covers the +7V to -7V common mode range for V.11 (RS-422) requirements. The V.11 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category I signals which are used for clock and data signals.

V.35 Drivers

The fourth type of driver is the V.35 driver. These drivers were specifically designed to comply with the requirements of V.35. Unique to the industry, the **Sipex's** V.35 driver architecture used in the **SP505** does not need external termination resistors to operate and comply with V.35. This simplifies existing V.35 implementations that use external termination schemes. The V.35 drivers can produce ±0.55V driver output signals with minimum deviation (maximum 20%) given an equivalent load of 100Ω. With the help of internal resistor networks, the drivers achieve the 50Ω to 150Ω source impedance and the 135Ω to 165Ω short-circuit impedance for V.35. The V.35 driver is disabled and transparent when the decoder is in all other modes. All of the differential drivers; V.11 (RS-422) and V.35, can operate over 10Mbps.

Driver Enable and Input

All the drivers in the **SP505** contain individual enable lines which can tri-state the driver outputs when a logic "1" is applied. This simplifies half-duplex configurations for some applications and also provides simpler DTE/DCE flexibility with one integrated circuit.

The driver inputs are both TTL or CMOS compatible. Each driver input should have a pull-down or pull-up resistor so that the output will be at a defined state. Unused driver inputs should not be left floating.

Receivers

The **SP505** has seven (7) independent receivers which can be programmed for the different interface modes. Control for the mode selection is done via a 4–bit control word, which is the same as the driver's 4-bit control word.
Like the drivers, the receivers are prearranged for the specific requirements of the synchronous

serial interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows the mode of each receiver in the different interface modes that can be selected.

There are three basic types of receiver circuits — V.28, V.10, and V.11.

V.28 Receivers

The V.28 receiver is single–ended and accepts V.28 signals from the V.28 driver. The V.28 receiver has an operating voltage range of ±15V and can receive signals down to ±3V. The input sensitivity complies with RS-232 and V.28 specifications at ±3V. The input impedance is 3kΩ to 7kΩ in accordance to RS-232 and V.28 over a ±15V input range. The receiver output produces a TTL/CMOS signal with a +2.4V minimum for a logic "1" and a +0.8V maximum for a logic "0". V.28 receivers are used in RS-232 mode for all data, clock and control signals. They are also used in V.35 mode for control line signals: CTS, DSR, LL, and RL. The V.28 receivers can operate to at least 120kbps.

V.10 Receivers

The V.10 receivers are also single–ended as with the V.28 receivers but have an input threshold as low as ±200mV. The input impedance is guaranteed to be greater than 4KΩ, with an operating voltage range of ±7V. The V.10 receivers can operate to at least 120kbps. V.10 receivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category II signals as indicated by their corresponding specifications.

V.11 Receivers

The third type of receiver is a differential which supports V.11 and RS-485 signals. This receiver has a typical input impedance of 10kΩ and a typical differential threshold of ±200mV, which complies with the V.11 specification. Since the characteristics of the V.11 receivers are actually subsets of RS-485, the V.11 receivers can accept RS-485 signals. However, these receivers cannot support 32-transceivers on the signal bus due to the lower input impedance as specified in the RS-485 specification. Three receivers (RxD, RxC, and SCT) include a typical 120Ω cable termination resistor across the A and B inputs. The resistor for the three receivers is switched on when the **SP505** is configured in a mode which uses V.11 receivers. The V.11 cable termination resistor is switched off when the receiver is disabled or in another operating mode not using V.11 receivers. The V.11 receivers are used in X.21, RS-449, EIA-530, EIA-530A and V.36 as Category I signals for receiving clock, data, and some control line signals not covered by Category II V.10 circuits. The differential receivers can receive signals over 10Mbps.

V.35 Receiver

The V.11 receivers are also used for the V.35 mode. Unlike the older implementations of differential receivers used for V.35, the **SP505** contains an internal resistor termination network that ensures a V.35 input impedance of 100Ω (±10Ω) and a short-circuit impedance of 150Ω (±15Ω). The traditional V.35 implementations required external termination resistors to achieve the proper V.35 impedances. The internal network is connected via low on-resistance FET switches when the decoder is changed to V.35 mode. These FET switches can accept input signals of up to ±15V without any forward biasing and other parasitic affects. The V.35 termination resistor network is switched off when the receiver is disabled either by the decoder or receiver enable pin. The termination network is transparent when all other modes are selected. The V.35 receivers can operate over 10Mbps.

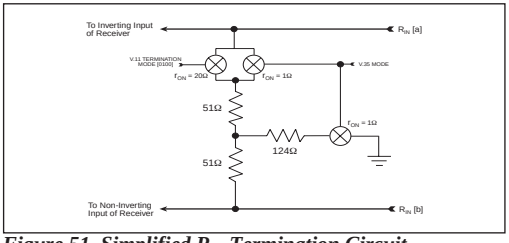


Figure 51. Simplified R_{IN} Termination Circuit

Receiver Enable and Output

Only one receiver includes an enable line. The SCTEN input for the SCT receiver can enable or tri-state the output of the receiver. When the pin is at a logic "0", the receiver output is high impedance and any input termination internal connected is switched off. The inputs will be at approximately 10kΩ during tri-state.

All receivers include a fail-safe feature that outputs a logic "1" when the receiver inputs are open. The differential receivers allocated for data and clock signals (RxD, RxC, and SCT) have advanced fail-safe that outputs a logic "1" when the inputs are either open, shorted, or terminated. Other discrete or integrated implementations require external pull-up and pull-down resistors to define the receiver output state. For single-ended V.28 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic high ("1") at the receiver outputs. The single-ended V.10 receivers produce a logic LOW ("0") on the output when the inputs are open. This is due to an internal pull-up device connected to the input. The differential receivers have the same internal pull-up device on the non-inverting input which produces a logic HIGH ("1") at the receiver output, representing an "OFF" state to the HDLC controller. The three differential receivers when configured in V.35 mode (RxD, RxC & SCT) will also include fail-safe even when the internal termination resistor network is connected and the inputs are either shorted or floating.

Decoder

The **SP505** has the ability to change the interface mode of the drivers or receivers via a 4–bit switch. The decoder for the drivers and receivers can be latched through a control pin.

The control word can be latched either high or low to write the appropriate code into the **SP505**. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP505**. Undefined codes may represent other interface modes not specified (consult the factory for more information). The drivers and receivers are controlled with the data bits labeled DEC_3–DEC_0. All of the drivers outputs and receiver outputs can be put into tri-state mode by writing 0000 to the driver decode switch. All internal termination networks are switched off during this mode. Individual tri-state capability is possible for all drivers through each driver's own enable control input. The SCT receiver also contains an individual enable input. When this control pin is disabled (logic "0"), the V.11 and V.35 input termination is deactivated. The 0000 decoder word will override the enable control line for the one receiver (SCT).

The **SP505** contains internal loopback capabilities for self-diagnostic tests. Loopback is enabled through the decoder. To initiate single-ended mode loopback, the decoder word is 1010. To initiate differential mode loopback, the decoder word is 1011. The minimum transmission rates into the **SP505** under loopback conditions are 120kbps for single-ended mode and 5Mbps for differential mode. The driver outputs are tri-stated and the receiver inputs are disabled during loopback. The receiver input impedance during loopback is approximately 10kΩ.

The **SP505** is equipped with a latch control for the four (4) decoder bits. The latch control pin is pin 8 of the **SP505**. The latch control is active low, a logic low on pin 8 will latch the decoder signals. A logic "1" on pin 8 will force the latch to be transparent to the user. A pulse width of at least 30ns is required to latch the decoder for the next mode. The resultant output is typically 600ns after the latch control pin is toggled assuming that the decoder word is set.

NET1/2 & TBR2 European Compliancy

As with all of **Sipex's** previous multi-protocol serial transceiver ICs, the drivers and receivers have been designed to meet all the requirements to NET1/2. The **SP505** is internally tested to all the NET1/2 physical layer testing parameters and the ITU Series V specifications.

With the emergence of ETSI TBR2 (Technical Basis for Regulation) document now in place as an alternative for European compliancy, **Sipex** has tested the **SP505** to TBR2 specifications to ensure "CE" approval for either testing method.

The **SP505** was externally tested by TUV Telecom Services, Division of TUV Rheinland, and passed both NET1/2 and TBR2 requirements. Test reports **(NET2/052101/98 for NET1/2 and CTR2/05101/98 for TBR2)** can be furnished upon request.

Please note that although the **SP505** adheres to NET1/2 testing; any complex or unusual configuration should be double-checked to ensure NET compliance. Consult factory for details.

SP505 Driver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422 w/ Term.	RS422	RS449	EIA530	EIA-530A	V.36
DEC_3 – DEC_0	0000	0010	1110	0100	0101	1100	1101	1111	0110
SD(a)	tri-state	V.28	V.35–	V.11–	V.11–	V.11–	V.11–	V.11–	V.11–
SD(b)	tri-state	tri-state	V.35+	V.11+	V.11+	V.11+	V.11+	V.11+	V.11+
TR(a)	tri-state	V.28	V.28	V.11–	V.11–	V.11–	V.11–	V.10	V.10
TR(b)	tri-state	tri-state	tri-state	V.11+	V.11+	V.11+	V.11+	tri-state	tri-state
RS(a)	tri-state	V.28	V.28	V.11–	V.11–	V.11–	V.11–	V.11–	V.10
RS(b)	tri-state	tri-state	tri-state	V.11+	V.11+	V.11+	V.11+	V.11+	tri-state
RL(a)	tri-state	V.28	V.28	V.11–	V.11–	V.10	V.11–	V.11–	V.10
RL(b)	tri-state	tri-state	tri-state	V.11+	V.11+	tri-state	V.11+	V.11+	tri-state
LL(a)	tri-state	V.28	V.28	V.11–	V.11–	V.10	V.10	V.10	V.10
LL(b)	tri-state	tri-state	tri-state	V.11+	V.11+	tri-state	tri-state	tri-state	tri-state
ST(a)	tri-state	V.28	V.35–	V.11–	V.11–	V.11–	V.11–	V.11–	V.11–
ST(b)	tri-state	tri-state	V.35+	V.11+	V.11+	V.11+	V.11+	V.11+	V.11+
TT(a)	tri-state	V.28	V.35–	V.11–	V.11–	V.11–	V.11–	V.11–	V.11–
TT(b)	tri-state	tri-state	V.35+	V.11+	V.11+	V.11+	V.11+	V.11+	V.11+

Table 1. SP505 Driver Decoder Table

SP505 Receiver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422 w/ Term.	RS422	RS449	EIA530	EIA-530A	V.36
DEC_3 – DEC_0	0000	0010	1110	0100	0101	1100	1101	1111	0110
RD(a)	>10kΩ to GND	V.28	V.35–	V.11– 120Ω	V.11–	V.11– 120Ω	V.11– 120Ω	V.11– 120Ω	V.11– 120Ω
RD(b)	>10kΩ to GND	>10kΩ to GND	V.35+	V.11+ 120Ω	V.11+	V.11+ 120Ω	V.11+ 120Ω	V.11+ 120Ω	V.11+ 120Ω
RT(a)	>10kΩ to GND	V.28	V.35–	V.11– 120Ω	V.11–	V.11– 120Ω	V.11– 120Ω	V.11– 120Ω	V.11– 120Ω
RT(b)	>10kΩ to GND	>10kΩ to GND	V.35+	V.11+ 120Ω	V.11+	V.11+ 120Ω	V.11+ 120Ω	V.11+ 120Ω	V.11+ 120Ω
CS(a)	>10kΩ to GND	V.28	V.28	V.11–	V.11–	V.11–	V.11–	V.11–	V.10
CS(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND
DM(a)	>10kΩ to GND	V.28	V.28	V.11–	V.11–	V.11–	V.11–	V.10	V.10
DM(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND	>10kΩ to GND
RR(a)	>10kΩ to GND	V.28	V.28	V.11–	V.11–	V.11–	V.11–	V.11–	V.10
RR(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND
IC(a)	>10kΩ to GND	V.28	V.28	V.11–	V.11–	V.10	V.10	V.10	V.10
IC(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND
SCT(a)	>10kΩ to GND	V.28	V.35–	V.11– 120Ω	V.11–	V.11– 120Ω	V.11– 120Ω	V.11– 120Ω	V.11– 120Ω
SCT(b)	>10kΩ to GND	>12kΩ to GND	V.35+	V.11+ 120Ω	V.11+	V.11+ 120Ω	V.11+ 120Ω	V.11+ 120Ω	V.11+ 120Ω

Table 2. SP505 Receiver Decoder Table

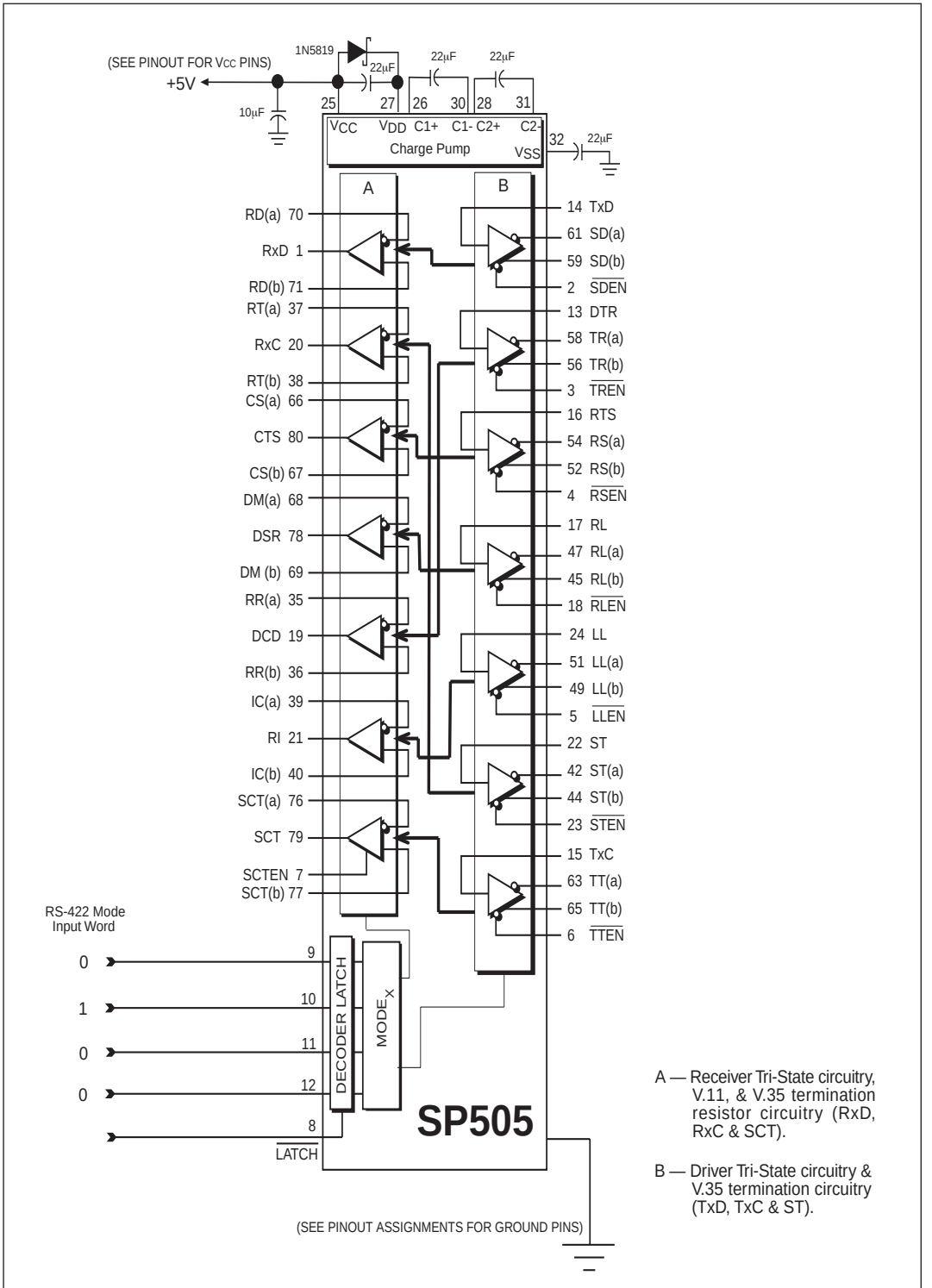


Figure 52. SP505 Typical Operating Circuit

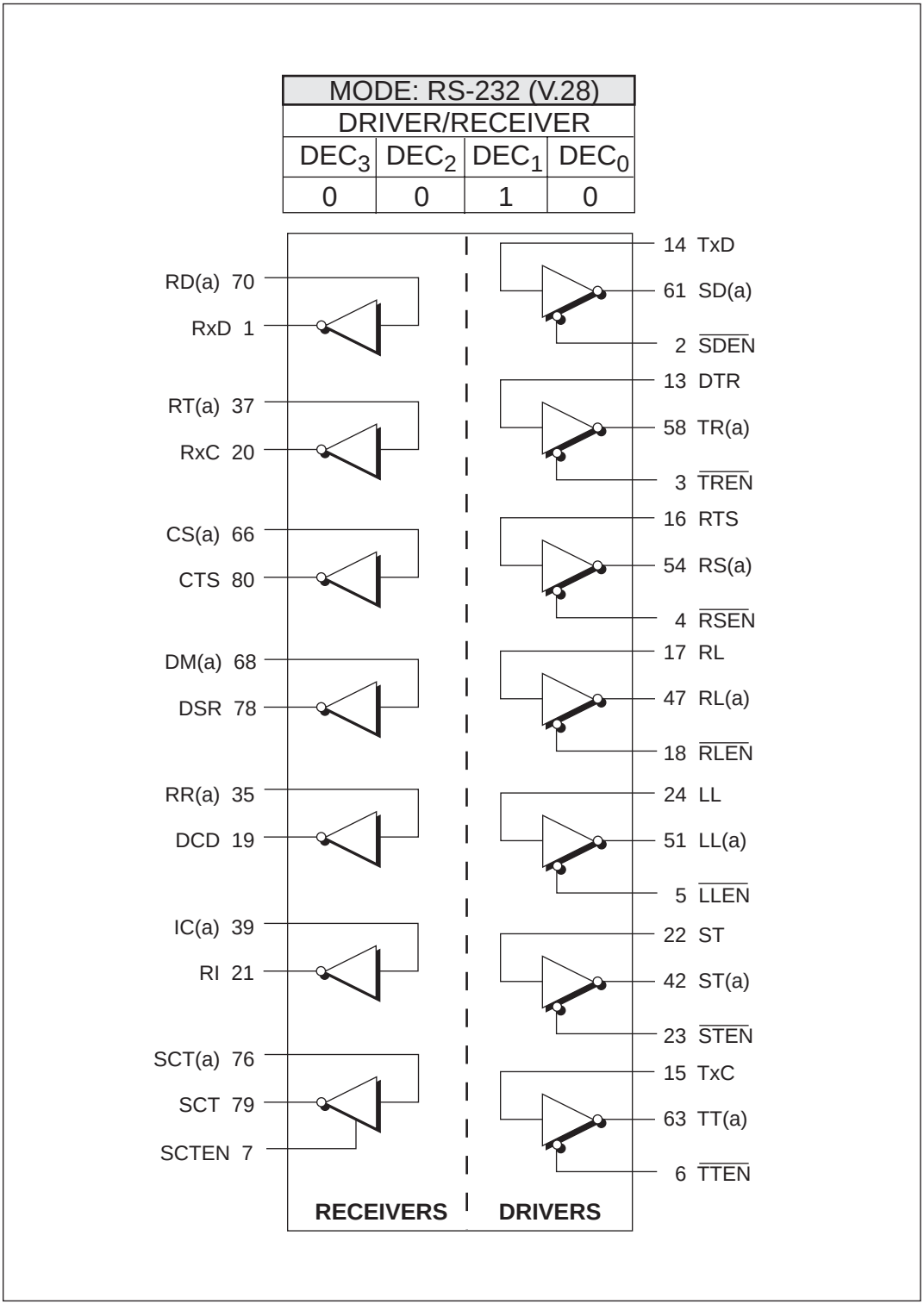


Figure 53. Mode Diagram — RS-232

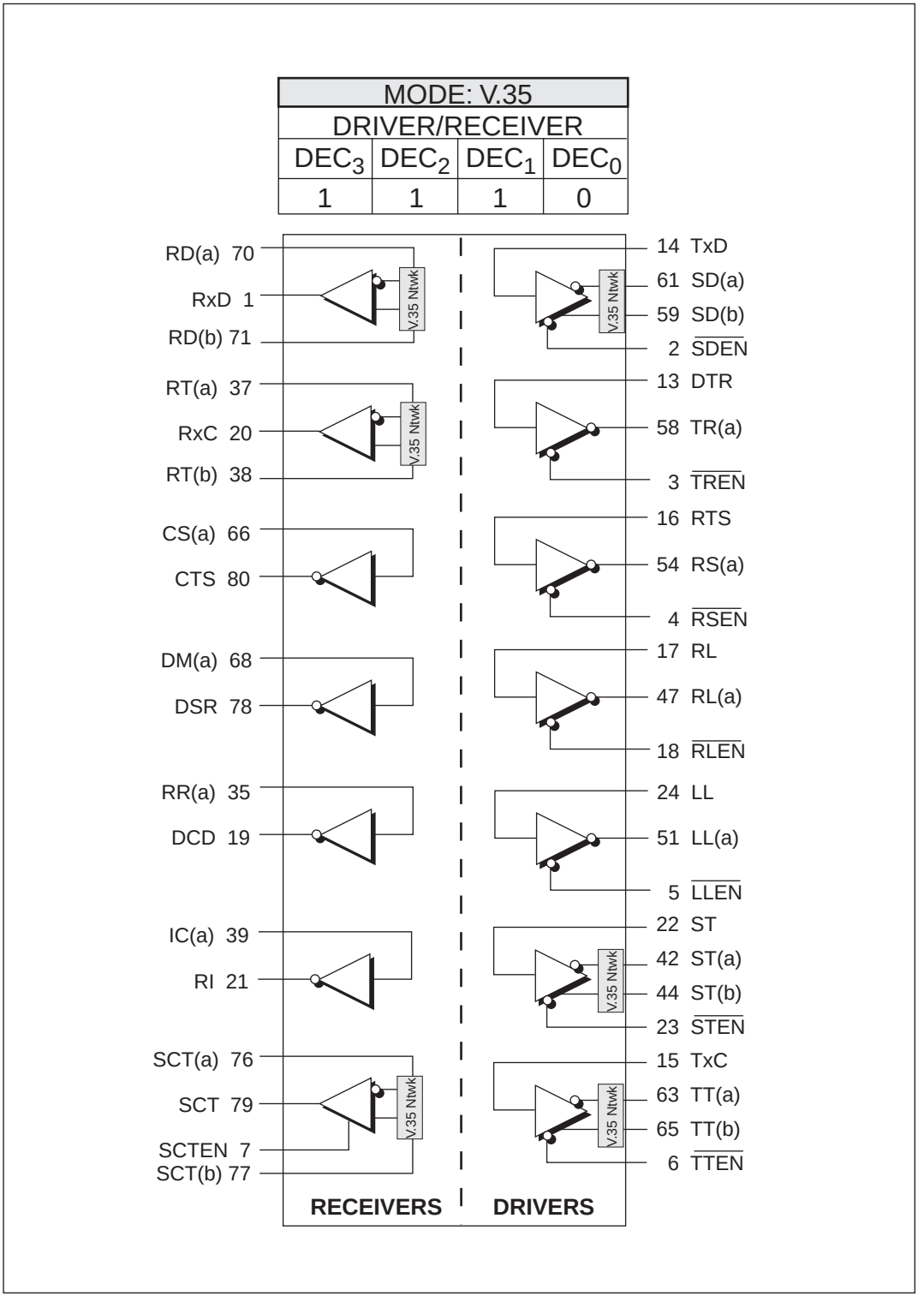


Figure 54. Mode Diagram — V.35

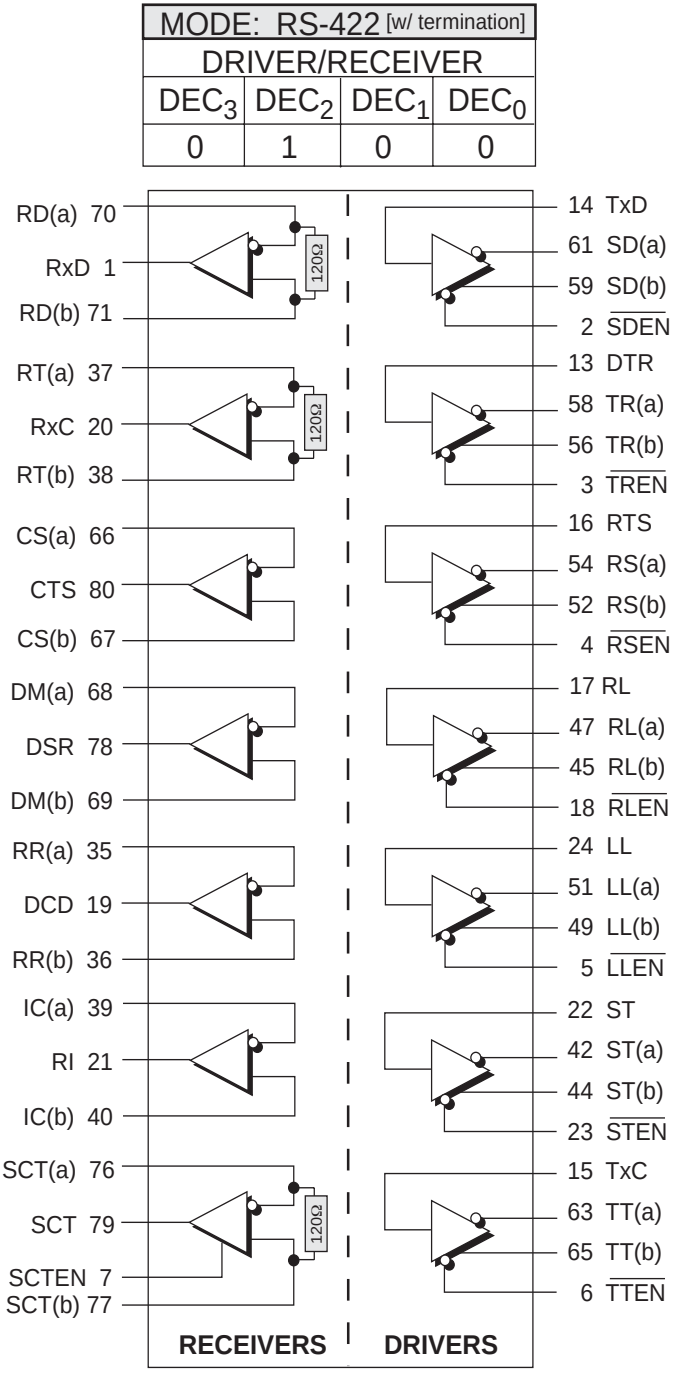


Figure 55. Mode Diagram — RS-422

MODE: RS-449			
DRIVER/RECEIVER			
DEC_3	DEC_2	DEC_1	DEC_0
1	1	0	0

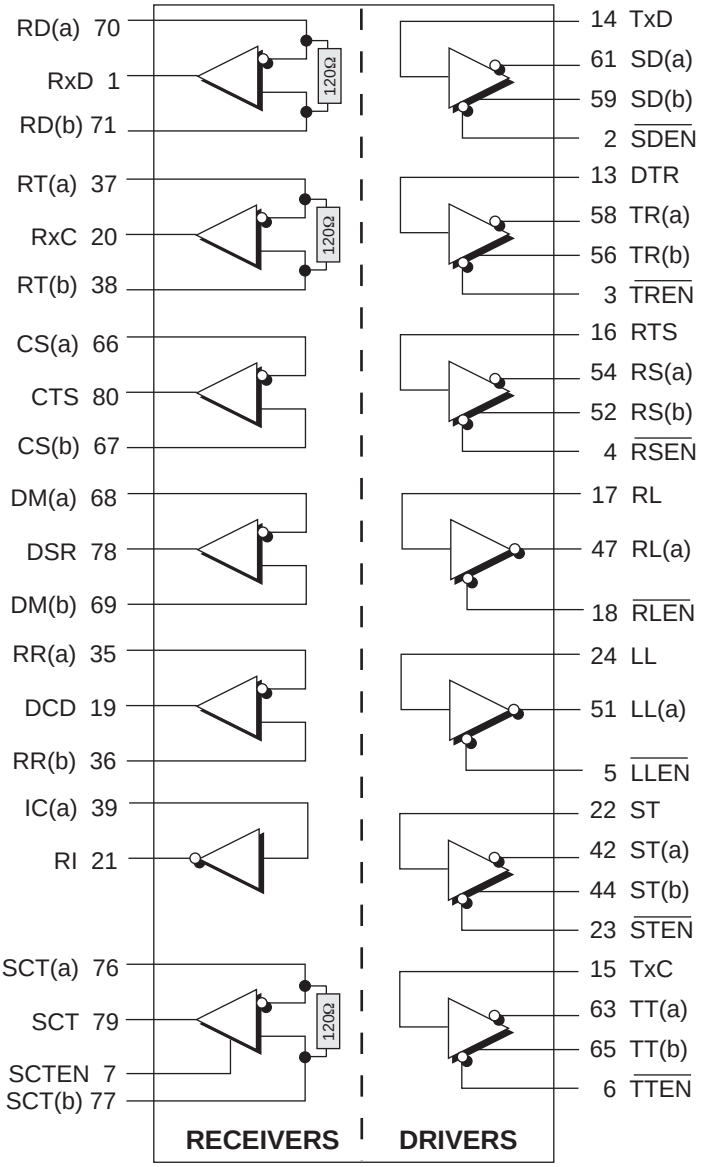


Figure 56. Mode Diagram — RS-449

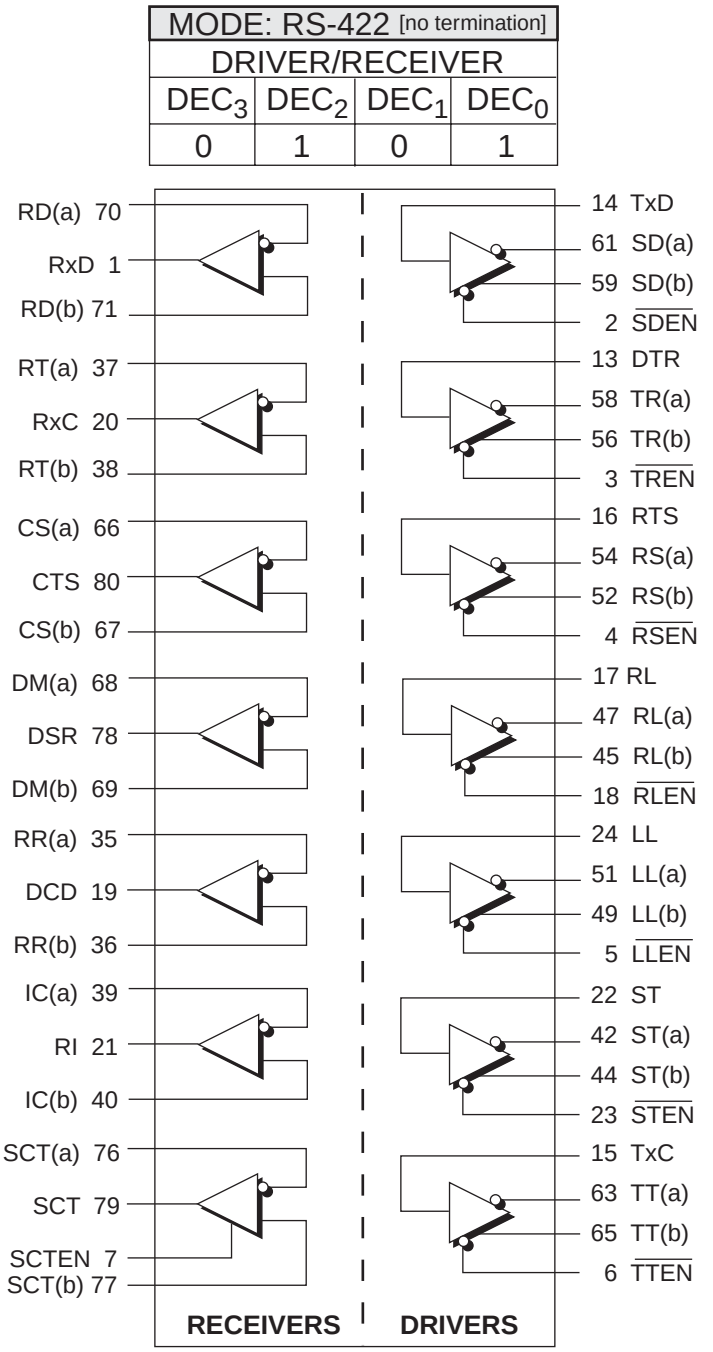


Figure 57. Mode Diagram — RS-422 w/o termination

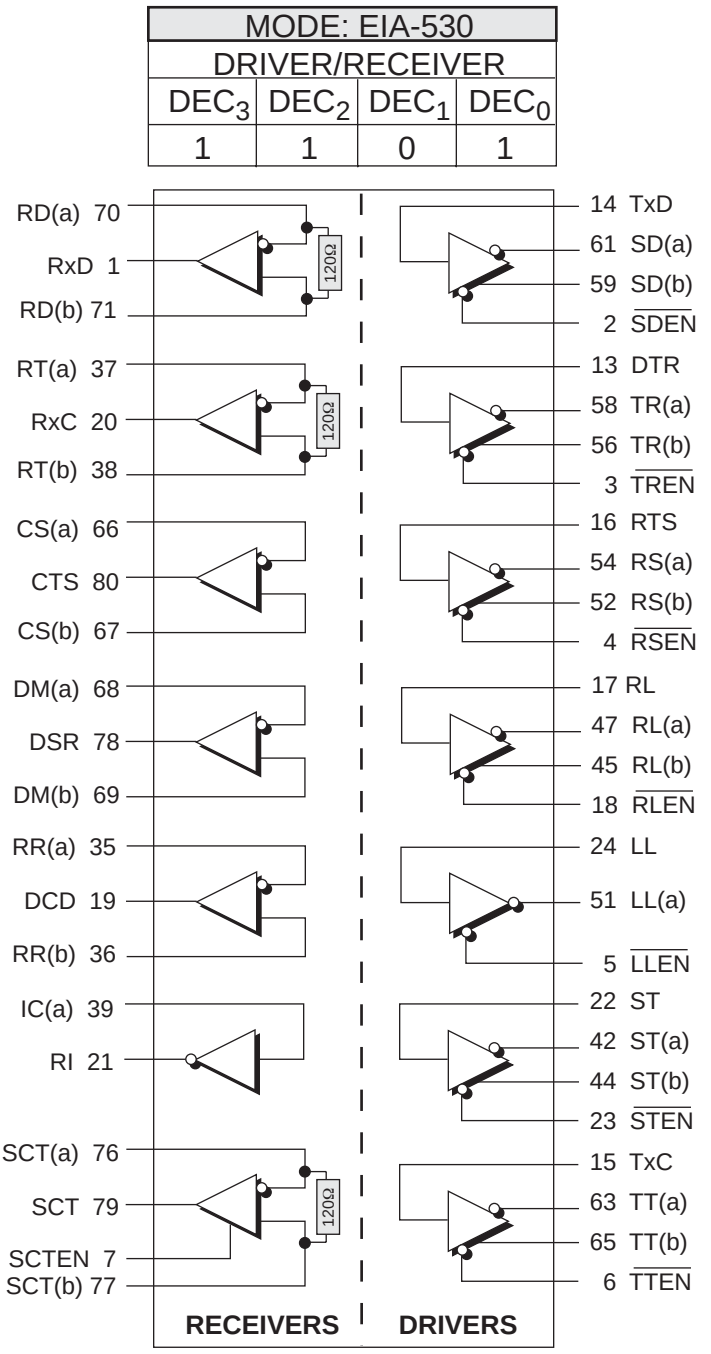


Figure 58. Mode Diagram — EIA-530

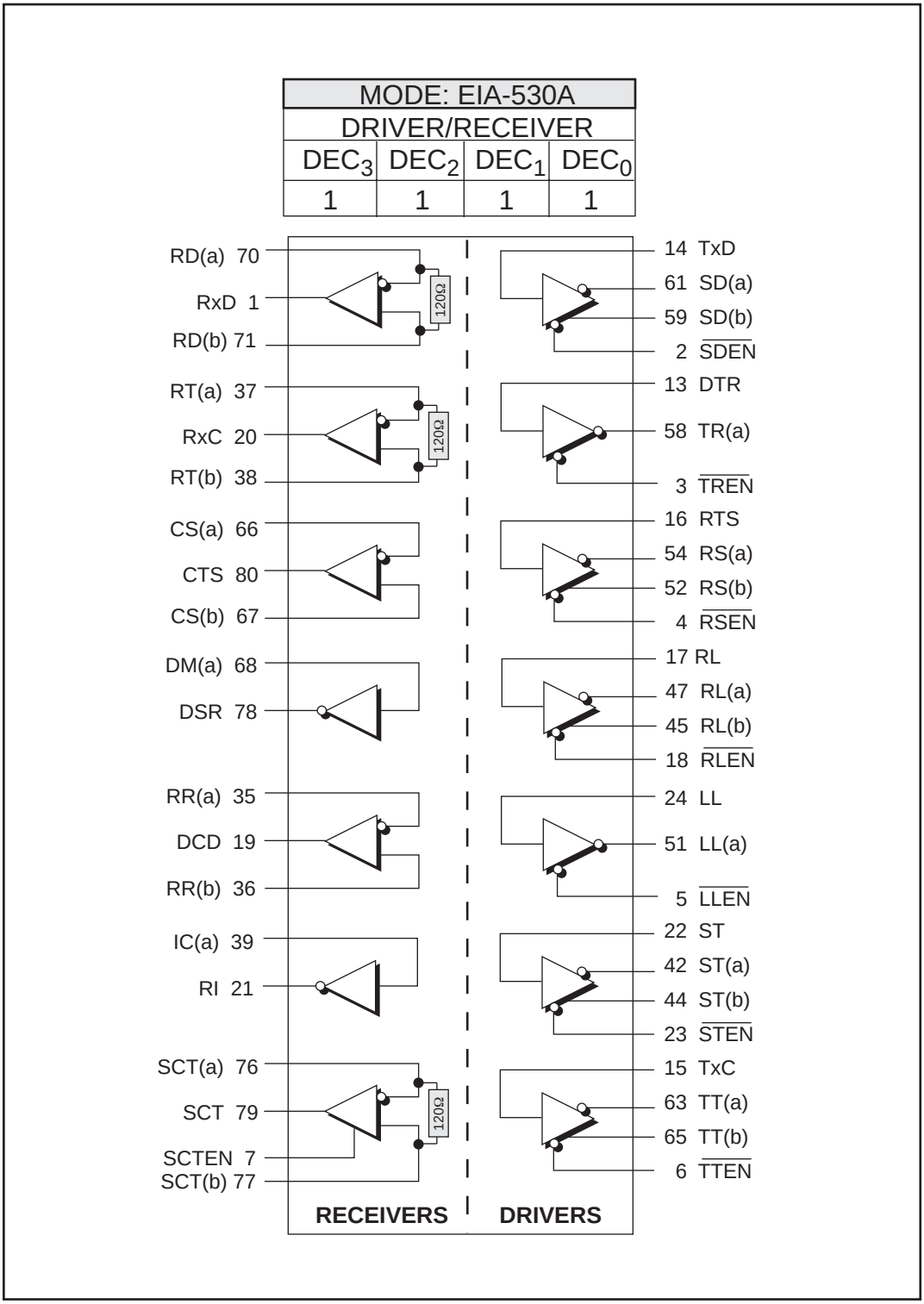


Figure 59. Mode Diagram — EIA-530A

MODE: V.36			
DRIVER/RECEIVER			
DEC_3	DEC_2	DEC_1	DEC_0
0	1	1	0

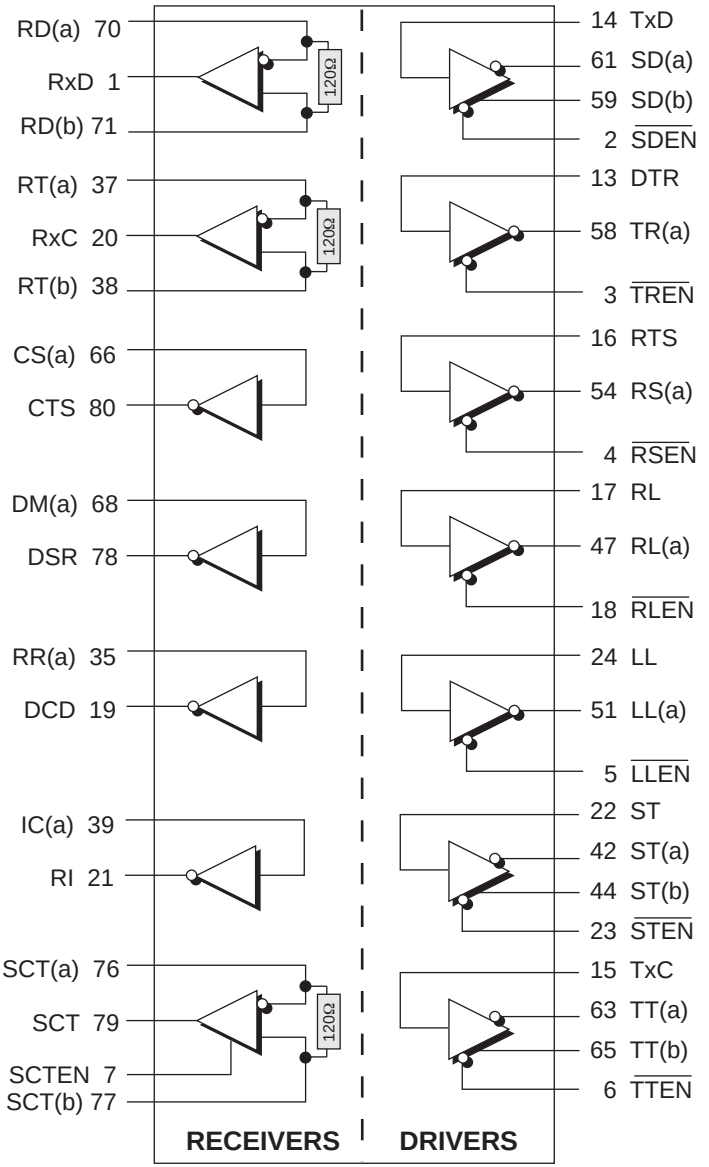
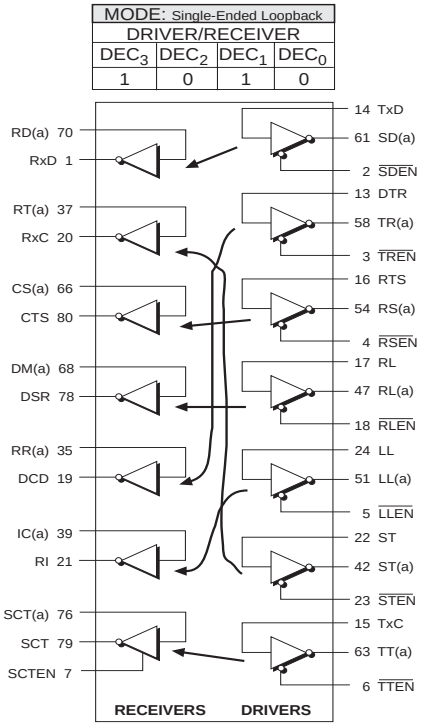


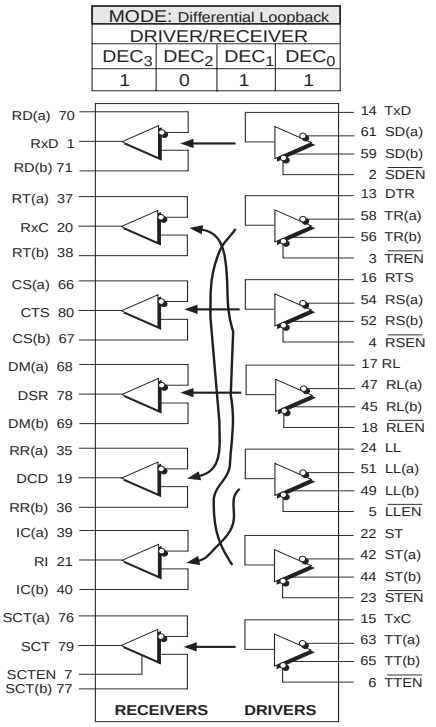
Figure 60. Mode Diagram — V.36

LOOPBACK MODE...

The **SP505** is equipped with two loopback modes. Single-ended loopback internally connects V.28 driver outputs to V.28 receiver inputs. The signal path is non-inverting and will support data rates up to 120kbps. The propagation delay times are as specified in the electrical specifications. To initiate a single-ended loopback, the code "1010" should be written to the driver decoder. Differential loopback is implemented by applying "1011" to the driver decoder. This internally connects V.11 driver outputs to V.11 receiver inputs. The signal path again is non-inverting; the differential loopback data rate can be at least 5Mbps.

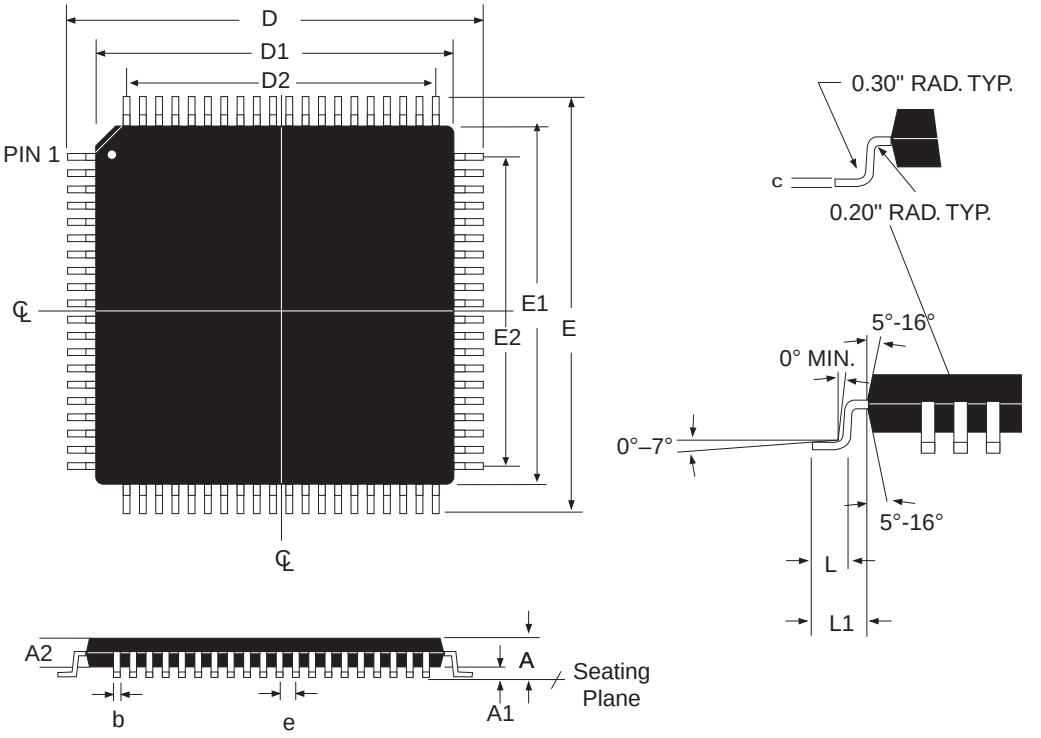
Under loopback conditions the receiver decoder is disabled. While the **SP505** is in either single-ended or differential loopback mode, the driver outputs are tri-stated and the receiver inputs are disabled.





Mode	Driver Output		Receiver Input		Driver Input	Receiver Output
	non-inverting	inverting	non-inverting	inverting		
Loopback DEC=1010	tri-state	tri-state	>10K to GND	>10K to GND	active	active
DEC=1011	tri-state	tri-state	>10K to GND	>10K to GND	active	active
Power down V_{CC}=V_{DD}=V_{SS}=0V	tri-state	tri-state	>10K to GND	>10K to GND	inactive	clamped at ±0.6V
Tri-state DEC=0000	tri-state	tri-state	>10K to GND	>10K to GND	inactive	tri-state

PACKAGE: 80 PIN MQFP



DIMENSIONS Minimum/Maximum (mm)	80–PIN MQFP JEDEC MS-22 (BEC) Variation		
SYMBOL	MIN	NOM	MAX
A			2.45
A1	0.00		0.25
A2	1.80	2.00	2.20
b	0.22		0.40
D	17.20 BSC		
D1	14.00 BSC		
D2	12.35 REF		
E	17.20 BSC		
E1	14.00 BSC		
E2	12.35 REF		
e	0.65 BSC		
N	80		

COMMON DIMENTIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.73	0.88	1.03
L1	1.60 BASIC		

80 PIN MQFP (MS-022 BC)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP505ACF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) MQFP
SP505BCF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) MQFP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
1/27/04	A	Implemented tracking revision.

ANALOG EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com