

SN54AHC595, SN74AHC595 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS373I – MAY 1997 – REVISED JUNE 2004

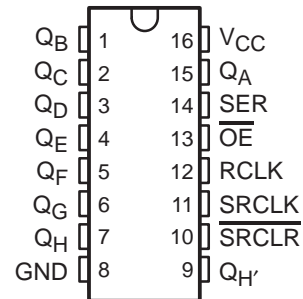
- Operating Range 2-V to 5.5-V V_{CC}
- 8-Bit Serial-In, Parallel-Out Shift
- Shift Register Has Direct Clear
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

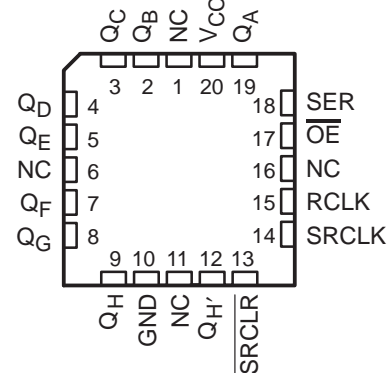
The 'AHC595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and a serial output for cascading. When the output-enable (\overline{OE}) input is high, all outputs, except $Q_{H'}$, are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

SN54AHC595 . . . J OR W PACKAGE
SN74AHC595 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC595 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC595N	SN74AHC595N
	SOIC – D	Tube	SN74AHC595D	AHC595
		Tape and reel	SN74AHC595DR	
	SOP – NS	Tape and reel	SN74AHC595NSR	AHC595
	SSOP – DB	Tape and reel	SN74AHC595DBR	HA595
	TSSOP – PW	Tube	SN74AHC595PW	HA595
		Tape and reel	SN74AHC595PWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC595J	SNJ54AHC595J
	CFP – W	Tube	SNJ54AHC595W	SNJ54AHC595W
	LCCC – FK	Tube	SNJ54AHC595FK	SNJ54AHC595FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

SN54AHC595, SN74AHC595

8-BIT SHIFT REGISTERS

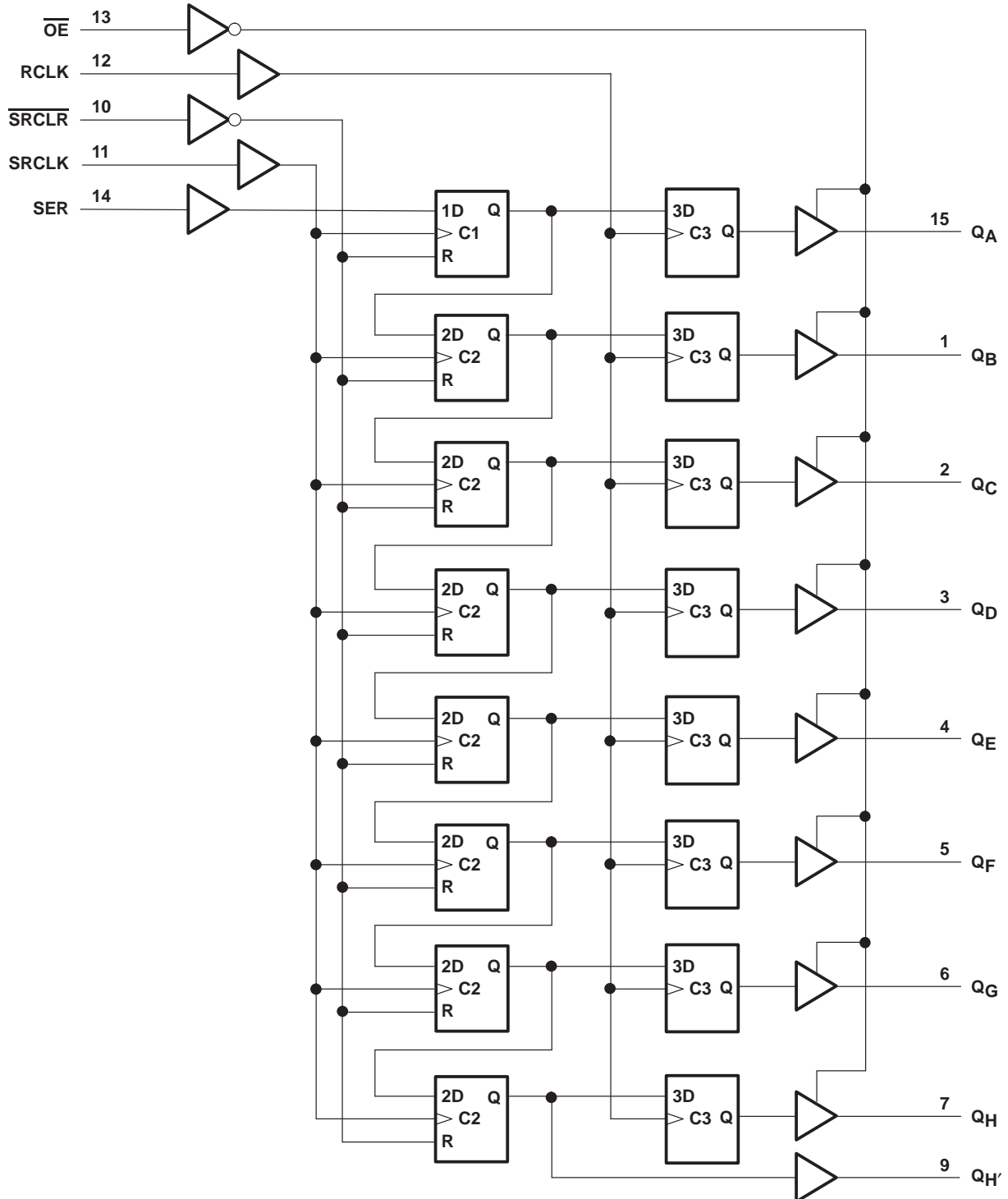
WITH 3-STATE OUTPUT REGISTERS

SCLS373I – MAY 1997 – REVISED JUNE 2004

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled.
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

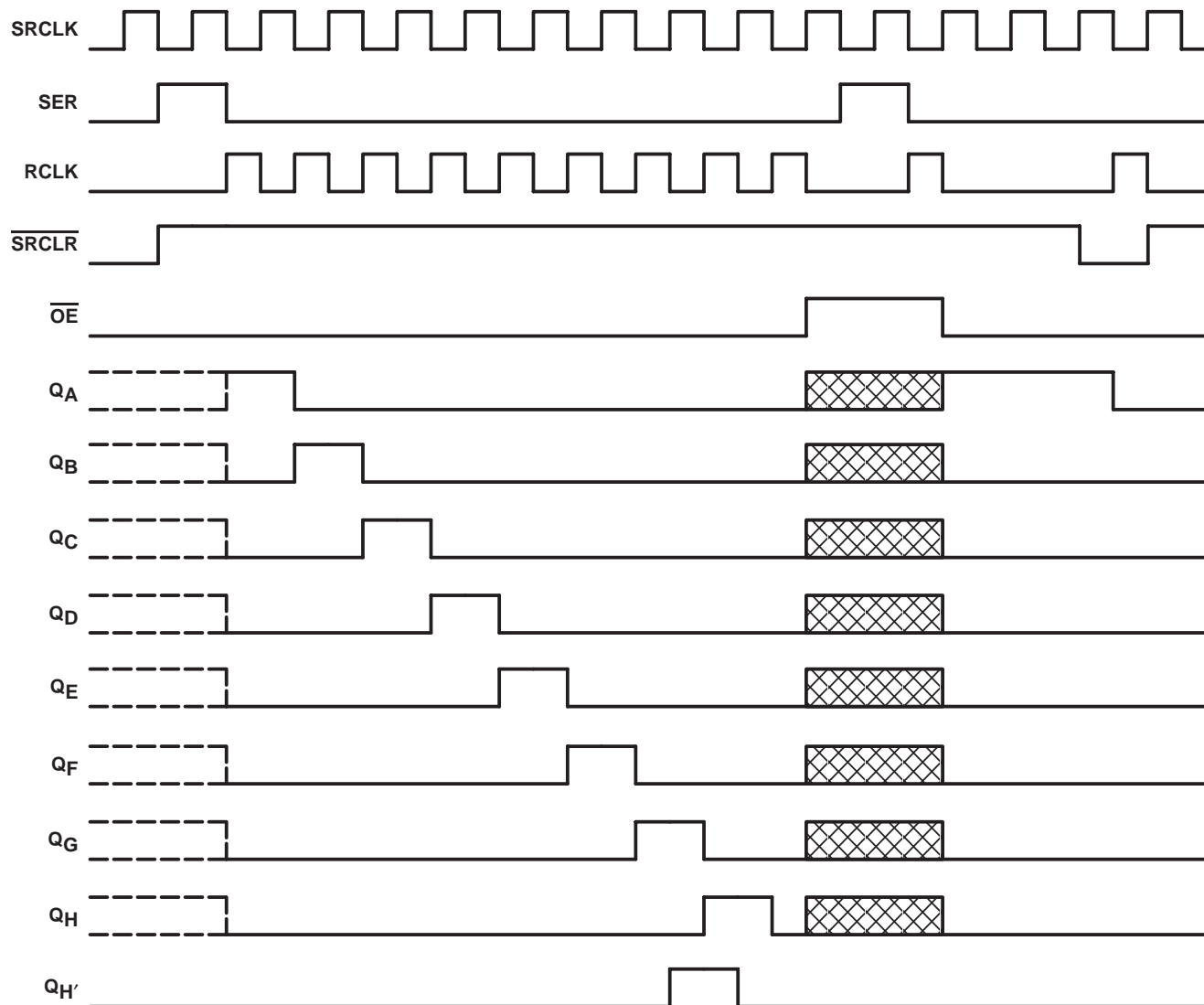
SN54AHC595, SN74AHC595

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

SCLS373I – MAY 1997 – REVISED JUNE 2004

timing diagram



NOTE:  implies that the output is in 3-State mode.

SN54AHC595, SN74AHC595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
SCLS373I – MAY 1997 – REVISED JUNE 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AHC595		SN74AHC595		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 3$ V	2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 3$ V		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		–50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		–4		–4	mA
		$V_{CC} = 5$ V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		4		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHC595, SN74AHC595

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

SCLS373I – MAY 1997 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC595		SN74AHC595		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I _{OZ}	V _I = V _{CC} or GND, V _O = V _{CC} or GND, OE = V _{IH} or V _{IL}	Q _A -Q _H	5.5 V		±0.25		±2.5		±2.5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	µA
C _i	V _I = V _{CC} or GND	5 V			3	10			10	pF
C _o	V _O = V _{CC} or GND	5 V			5.5					pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54AHC595		SN74AHC595		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	SRCLK high or low	5		5		5		ns
		RCLK high or low	5		5		5		
		SRCLR low	5		5		5		
t _{su}	Setup time	SER before SRCLK↑	3.5		3.5		3.5		ns
		SRCLK↑ before RCLK↑†	8		8.5		8.5		
		SRCLR low before RCLK↑	8		9		9		
		SRCLR high (inactive) before SRCLK↑	3		3		3		
t _h	Hold time	SER after SRCLK↑	1.5		1.5		1.5		ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54AHC595, SN74AHC595
8-BIT SHIFT REGISTERS
WITH 3-STATE OUTPUT REGISTERS
 SCLS373I – MAY 1997 – REVISED JUNE 2004

timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54AHC595		SN74AHC595		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	SRCLK high or low		5	5	5	5	ns
		RCLK high or low		5	5	5	5	
		$\overline{\text{SRCLR}}$ low		5	5	5	5	
t_{su}	Setup time	SER before SRCLK \uparrow		3	3	3	3	ns
		SRCLK \uparrow before RCLK \uparrow		5	5	5	5	
		$\overline{\text{SRCLR}}$ low before RCLK \uparrow		5	5	5	5	
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK \uparrow		2.5	2.5	2.5	2.5	
t_h	Hold time	SER after SRCLK \uparrow		2	2	2	2	ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC595		SN74AHC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	80*	120*		70*		70		MHz
			$C_L = 50\text{ pF}$	55	105		50		50		
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 15\text{ pF}$	6*	11.9*		1*	13.5*	1	13.5	ns
t_{PHL}				6*	11.9*		1*	13.5*	1	13.5	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 15\text{ pF}$	6.6*	13*		1*	15*	1	15	ns
t_{PHL}				6.6*	13*		1*	15*	1	15	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 15\text{ pF}$	6.2*	12.8*		1*	13.7*	1	13.7	ns
t_{PZH}	$\overline{\text{OE}}$	$Q_A - Q_H$	$C_L = 15\text{ pF}$	6*	11.5*		1*	13.5*	1	13.5	ns
t_{PZL}				7.8*	11.5*		1*	13.5*	1	13.5	
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50\text{ pF}$	7.9	15.4		1	17	1	17	ns
t_{PHL}				7.9	15.4		1	17	1	17	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$	9.2	16.5		1	18.5	1	18.5	ns
t_{PHL}				9.2	16.5		1	18.5	1	18.5	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$	9	16.3		1	17.2	1	17.2	ns
t_{PZH}	$\overline{\text{OE}}$	$Q_A - Q_H$	$C_L = 50\text{ pF}$	7.8	15		1	17	1	17	ns
t_{PZL}				9.6	15		1	17	1	17	
t_{PHZ}	$\overline{\text{OE}}$	$Q_A - Q_H$	$C_L = 50\text{ pF}$	8.1	15.7		1	16.2	1	16.2	ns
t_{PLZ}				9.3	15.7		1	16.2	1	16.2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

SN54AHC595, SN74AHC595

8-BIT SHIFT REGISTERS

WITH 3-STATE OUTPUT REGISTERS

SCLS373I – MAY 1997 – REVISED JUNE 2004

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC595		SN74AHC595		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	135*	170*		115*		115		MHz
			$C_L = 50\text{ pF}$	95	140		85		85		
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 15\text{ pF}$		4.3*	7.4*	1*	8.5*	1	8.5	ns
t_{PHL}					4.3*	7.4*	1*	8.5*	1	8.5	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 15\text{ pF}$		4.5*	8.2*	1*	9.4*	1	9.4	ns
t_{PHL}					4.5*	8.2*	1*	9.4*	1	9.4	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 15\text{ pF}$		4.5*	8*	1*	9.1*	1	9.1	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H	$C_L = 15\text{ pF}$		4.3*	8.6*	1*	10*	1	10	ns
t_{PZL}					5.4*	8.6*	1*	10*	1	10	
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 50\text{ pF}$		5.6	9.4	1	10.5	1	10.5	ns
t_{PHL}					5.6	9.4	1	10.5	1	10.5	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$		6.4	10.2	1	11.4	1	11.4	ns
t_{PHL}					6.4	10.2	1	11.4	1	11.4	
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$		6.4	10	1	11.1	1	11.1	ns
t_{PZH}	$\overline{\text{OE}}$	Q_A-Q_H	$C_L = 50\text{ pF}$		5.7	10.6	1	12	1	12	ns
t_{PZL}					6.8	10.6	1	12	1	12	
t_{PHZ}	$\overline{\text{OE}}$	Q_A-Q_H	$C_L = 50\text{ pF}$		3.5	10.3	1	11	1	11	ns
t_{PLZ}					3.4	10.3	1	11	1	11	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

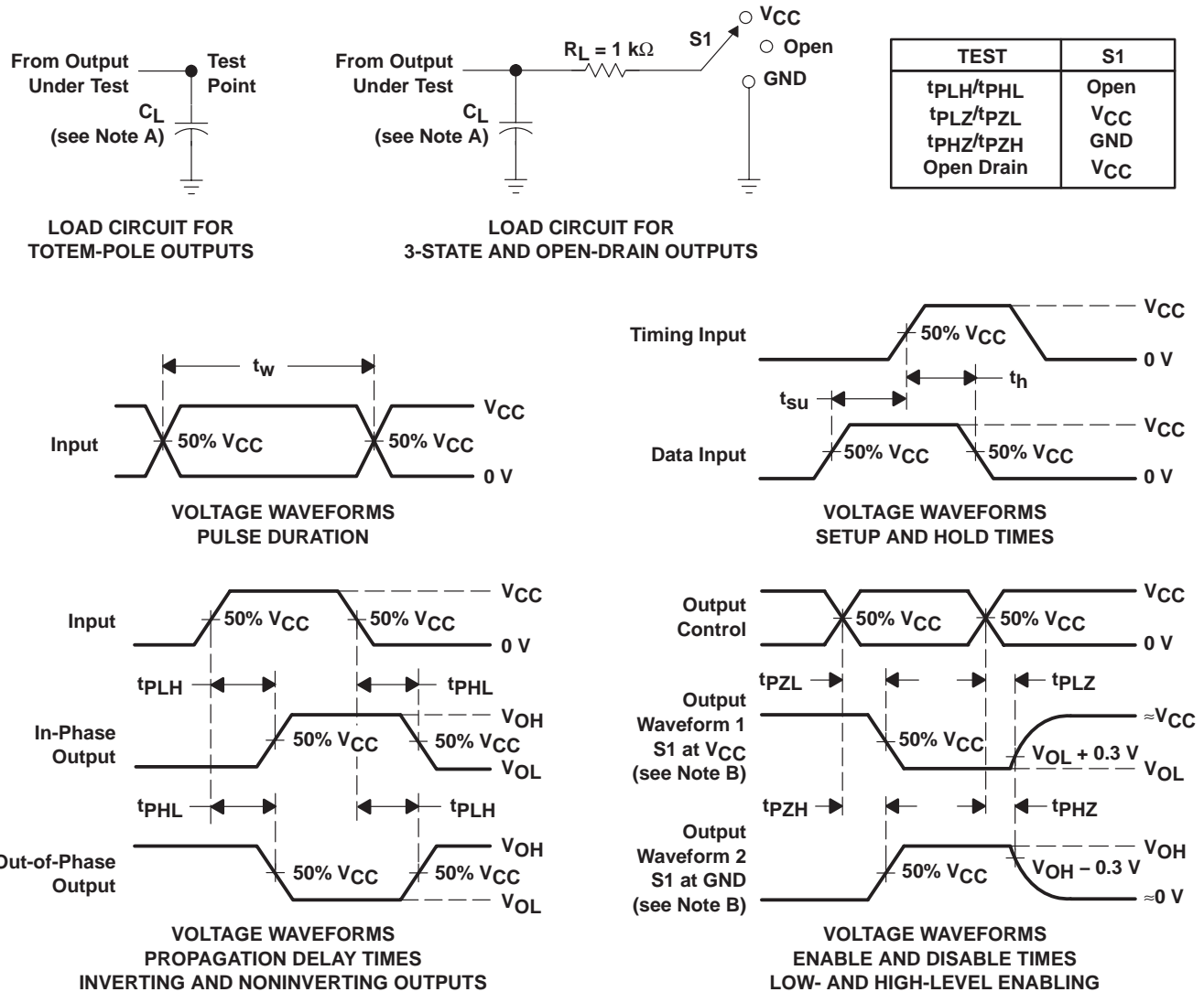
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	25.2	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AHC595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AHC595NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC595PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated