

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.0075 @ $V_{GS} = 10$ V	20
	0.0088 @ $V_{GS} = 4.5$ V	18.5

FEATURES

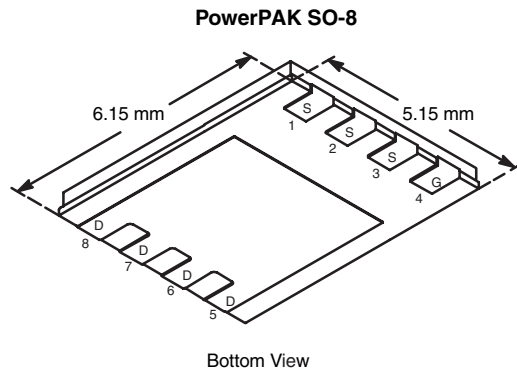
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100 % R_g Tested



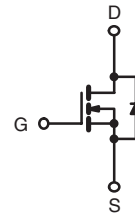
RoHS
COMPLIANT

APPLICATIONS

- Automotive Such As:
 - High-Side Switch
 - Motor Drives
 - 12-V Boardnet



Ordering Information: Si7478DP-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	60		V
Gate-Source Voltage		V _{GS}	±20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	20	15	A
	T _A = 70°C		16	12	
Pulsed Drain Current		I _{DM}	60		
Continuous Source Current (Diode Conduction) ^a		I _S	4.5	1.6	
Avalanche Current		I _{AS}	35		
Avalanche Energy		E _{AS}	61		mJ
Maximum Power Dissipation ^a	T _A = 25°C	P _D	5.4	1.9	W
	T _A = 70°C		3.4	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	18	23	$^\circ\text{C/W}$
	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.3	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

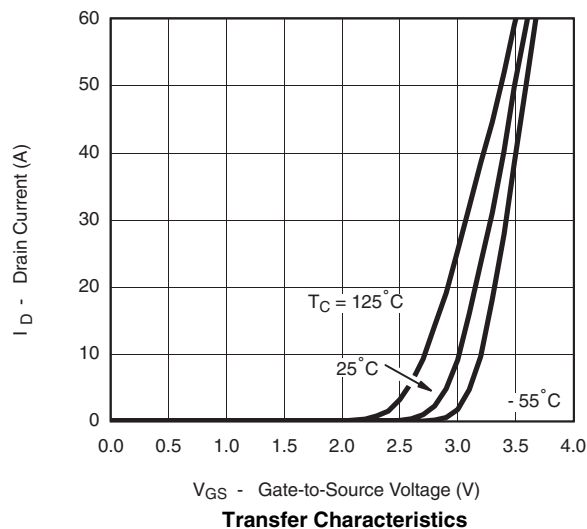
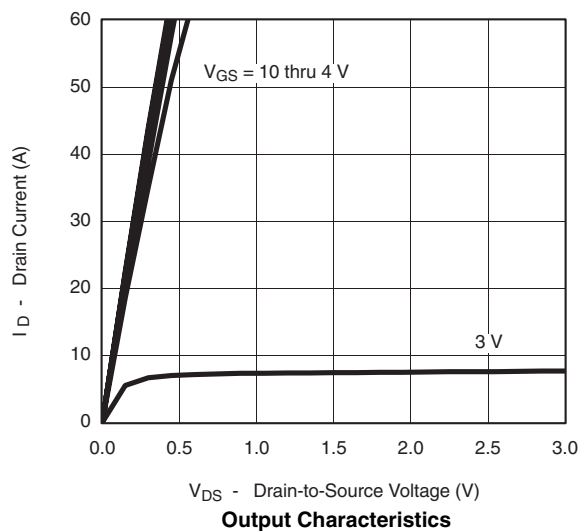
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 20\ \text{A}$		0.006	0.0075	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 18.5\ \text{A}$		0.007	0.0088	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 20\ \text{A}$		63		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.5\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.76	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 20\ \text{A}$		105	160	nC
Gate-Source Charge	Q_{gs}			22		
Gate-Drain Charge	Q_{gd}			19		
Gate Resistance	R_g		0.5	1.0	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\ \text{V}$, $R_L = 30\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		25	40	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			115	175	
Fall Time	t_f			45	70	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 4.5\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		41	70	

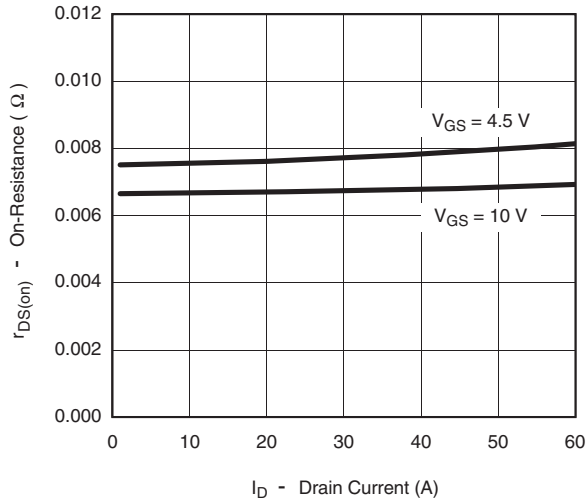
Notesa. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

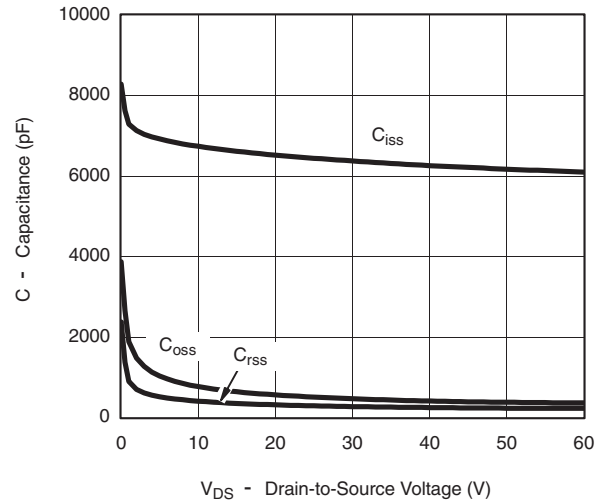
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless noted

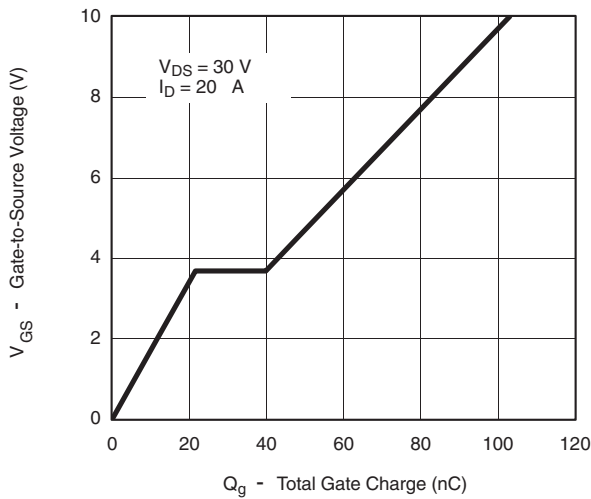
TYPICAL CHARACTERISTICS 25 °C, unless noted



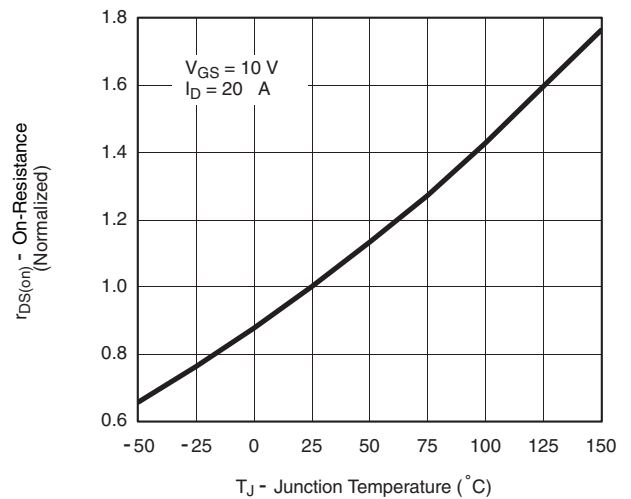
On-Resistance vs. Drain Current



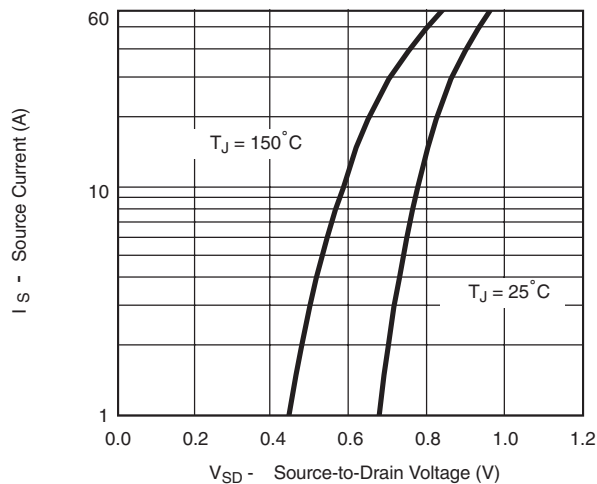
Capacitance



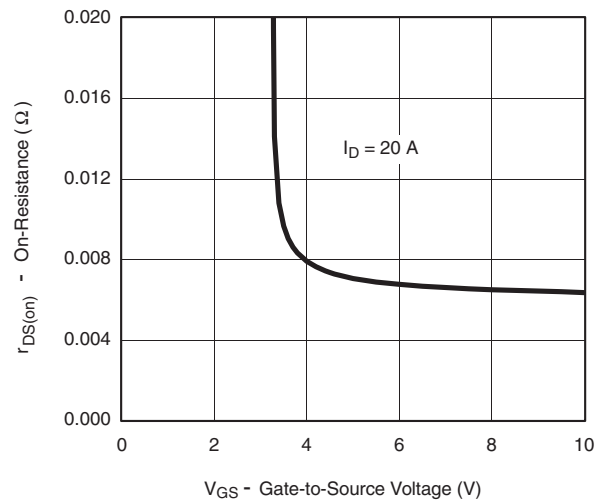
Gate Charge



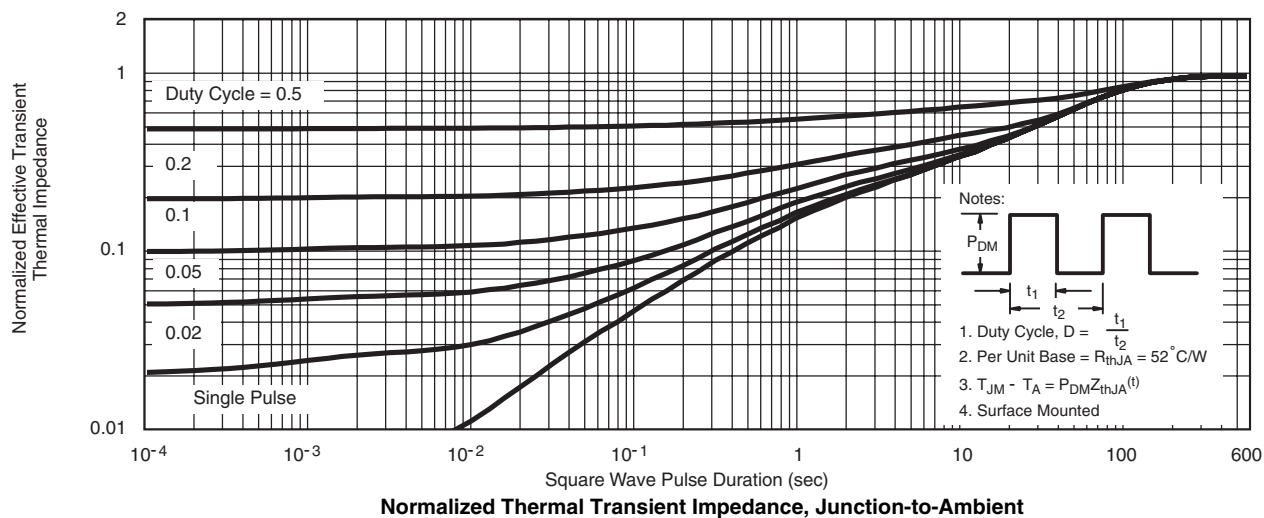
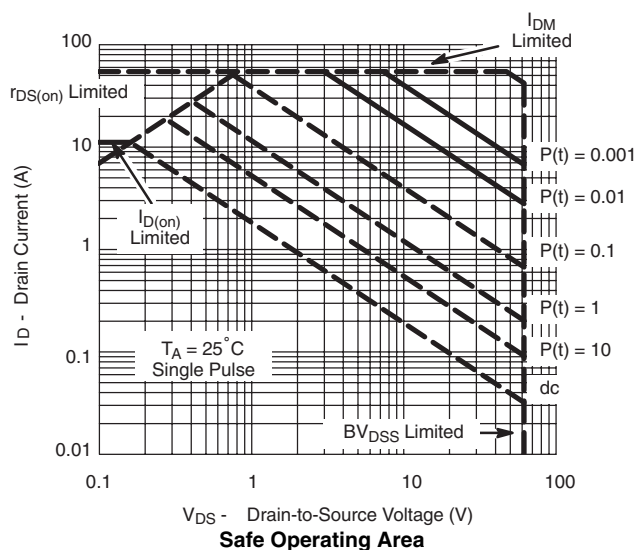
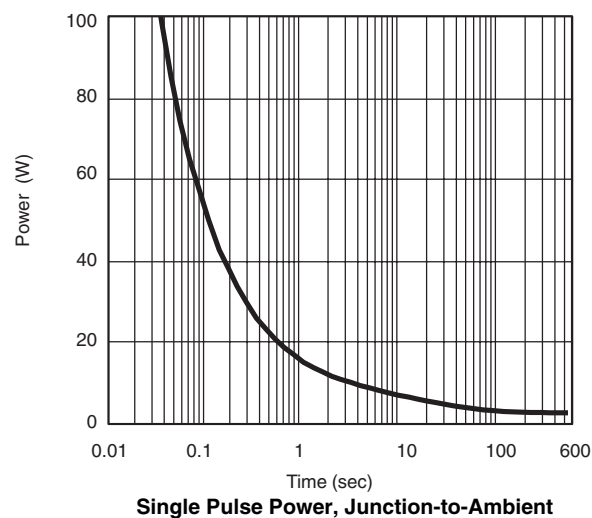
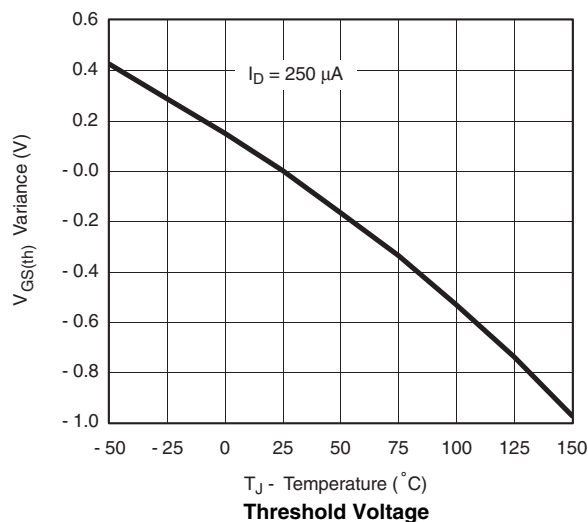
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

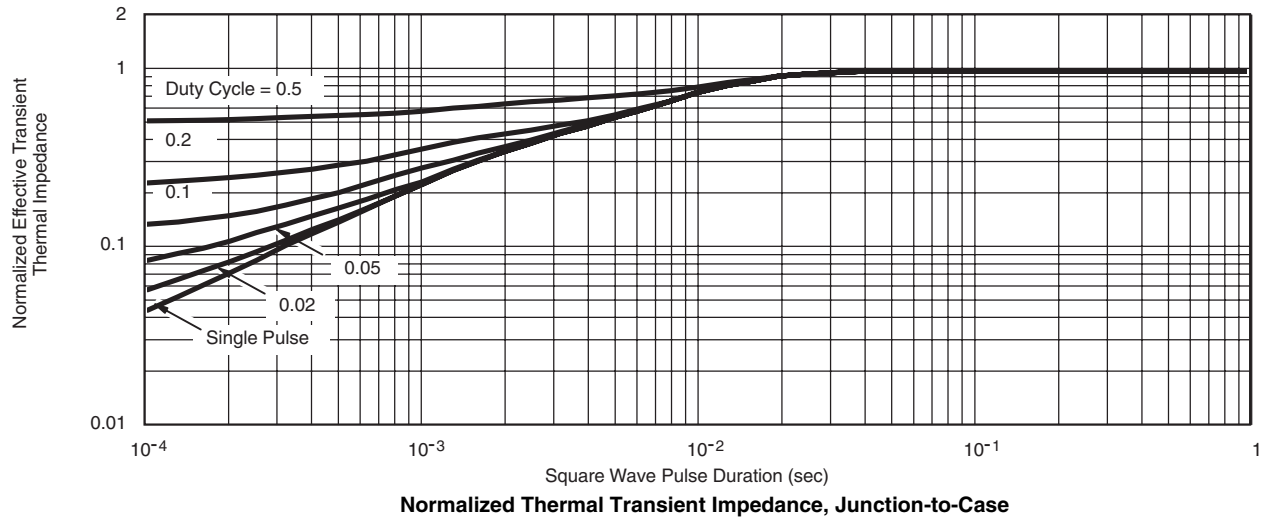


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless noted



TYPICAL CHARACTERISTICS 25 °C, unless noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72913>.