



P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.005 @ $V_{GS} = -10$ V	-24
	0.0095 @ $V_{GS} = -4.5$ V	-17

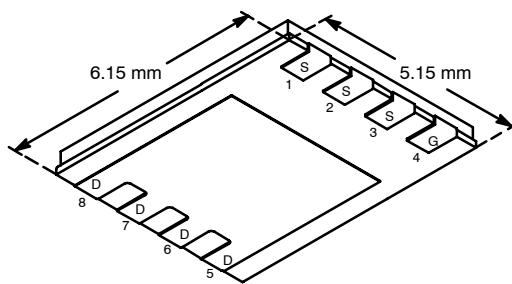
FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile

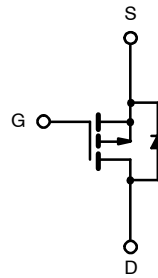
APPLICATIONS

- Battery and Load Switching
 - Notebook Computers
 - Notebook Battery Packs

PowerPAK™ SO-8



Bottom View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	-30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	-24	-14	A
	T _A = 70°C		-19	-11	
Pulsed Drain Current		I _{DM}	-60		
continuous Source Current (Diode Conduction) ^a		I _S	-4.5	-1.6	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	5.4	1.9	W
	T _A = 70°C		3.4	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	18	23	$^\circ\text{C/W}$
	Steady State		50	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.5	

Notes

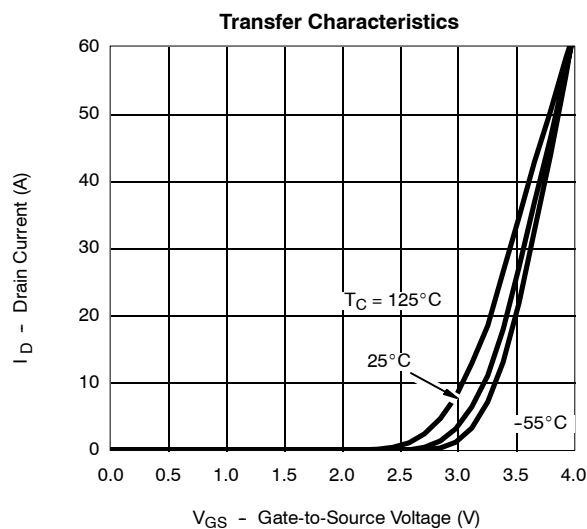
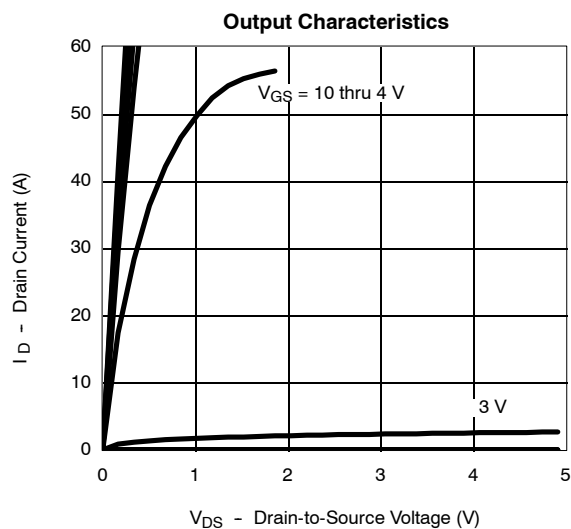
a. Surface Mounted on 1" x 1" FR4 Board.

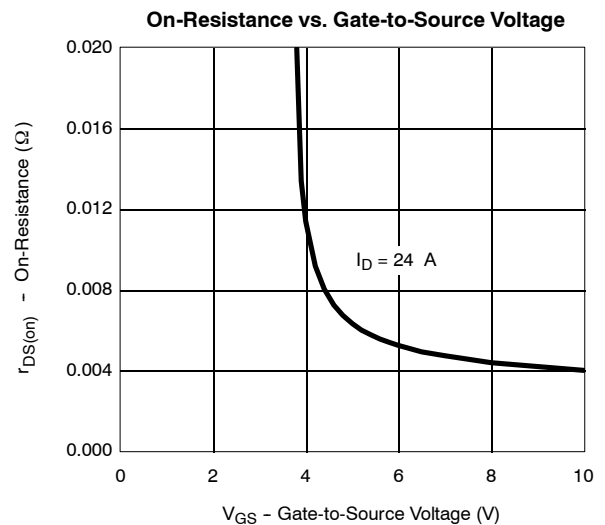
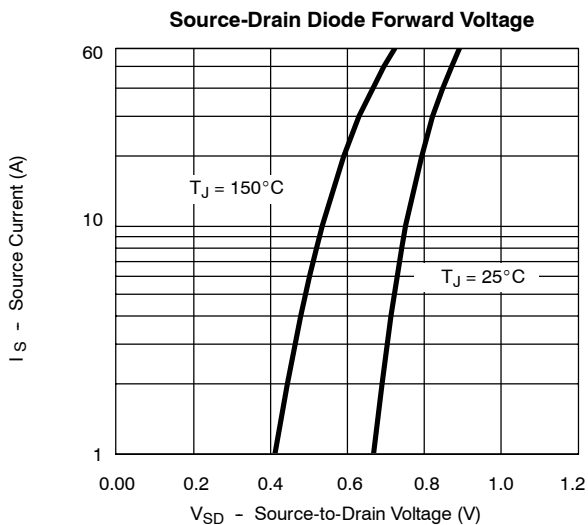
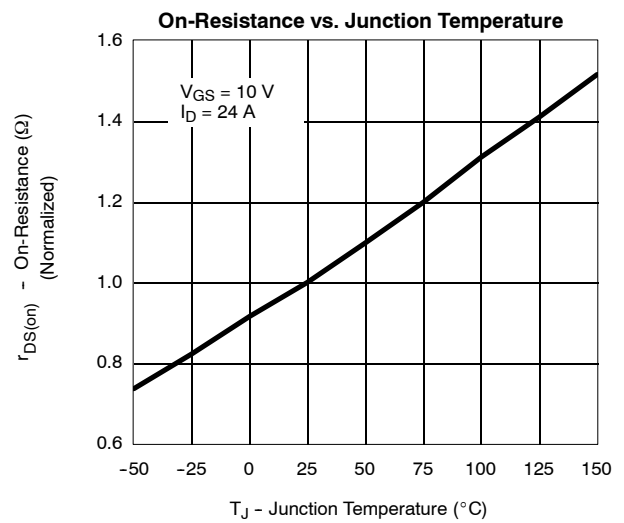
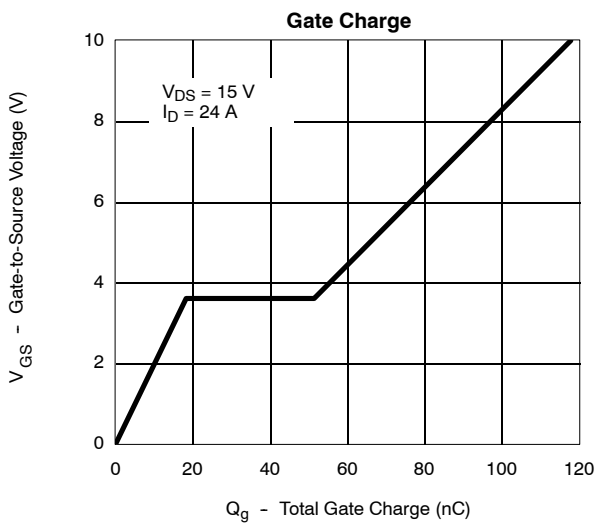
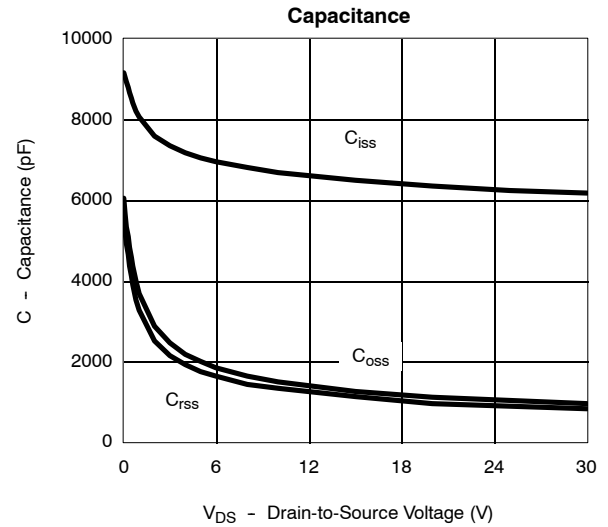
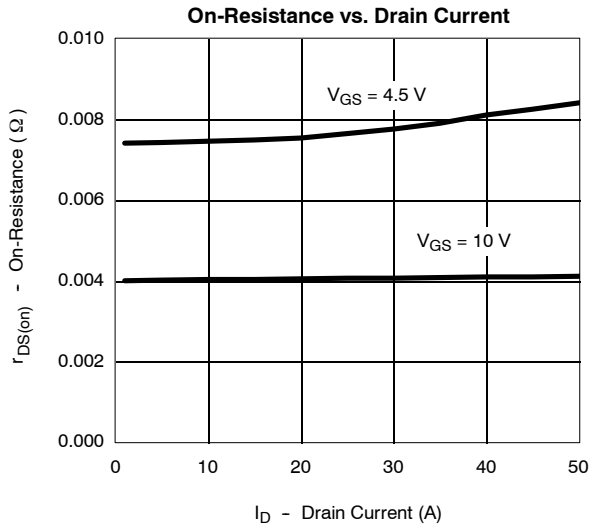
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

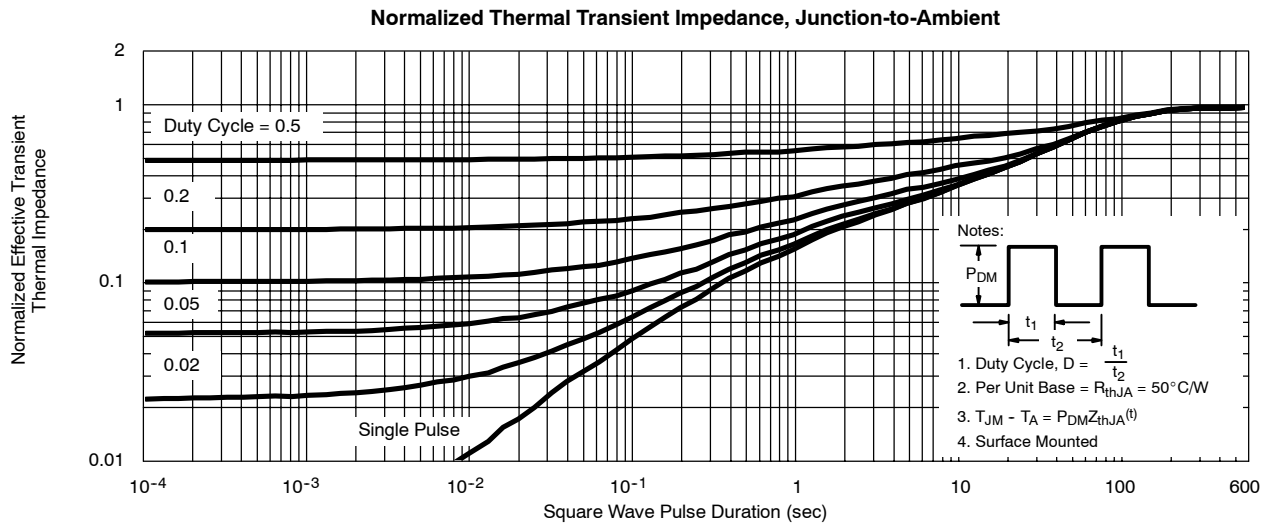
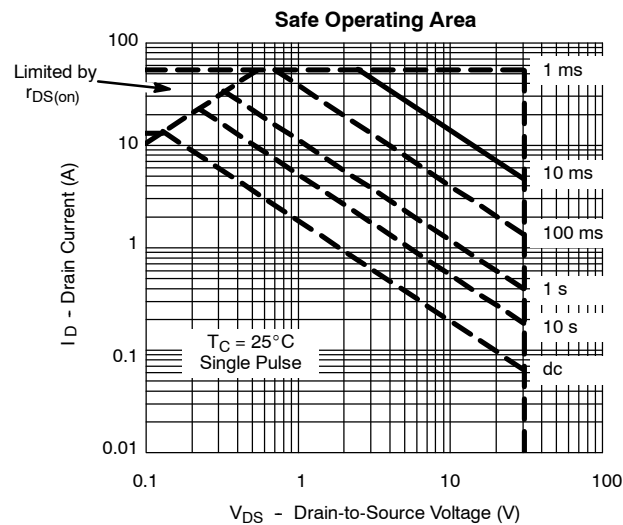
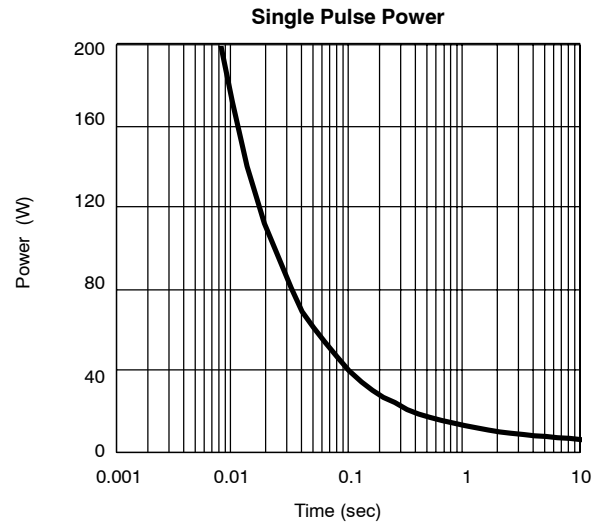
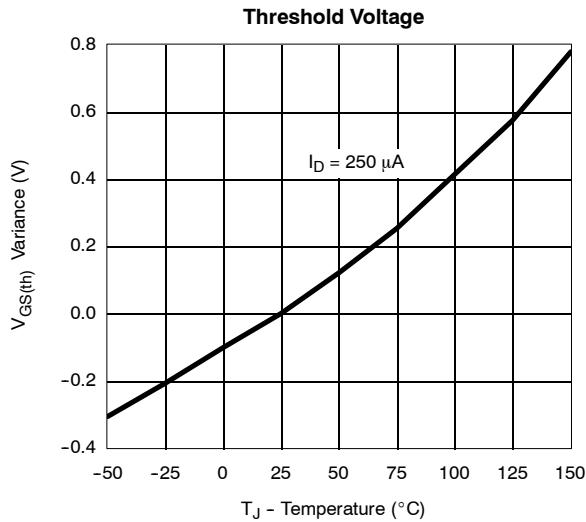
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-1.0		-3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -24\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}$, $V_{GS} = -10\ \text{V}$	-30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}$, $I_D = -24\ \text{A}$		0.0041	0.005	Ω
		$V_{GS} = -4.5\ \text{V}$, $I_D = -17\ \text{A}$		0.0077	0.0095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -24\ \text{A}$		70		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.75	-1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}$, $V_{GS} = -10\ \text{V}$, $I_D = -24\ \text{A}$		120	180	nC
Gate-Source Charge	Q_{gs}			18.3		
Gate-Drain Charge	Q_{gd}			33.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -10\ \text{V}$, $R_G = 6\ \Omega$		25	40	ns
Rise Time	t_r			40	65	
Turn-Off Delay Time	$t_{d(off)}$			220	350	
Fall Time	t_f			125	200	
Gate Resistance	R_g			4		Ω
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.9\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		87	135	ns

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

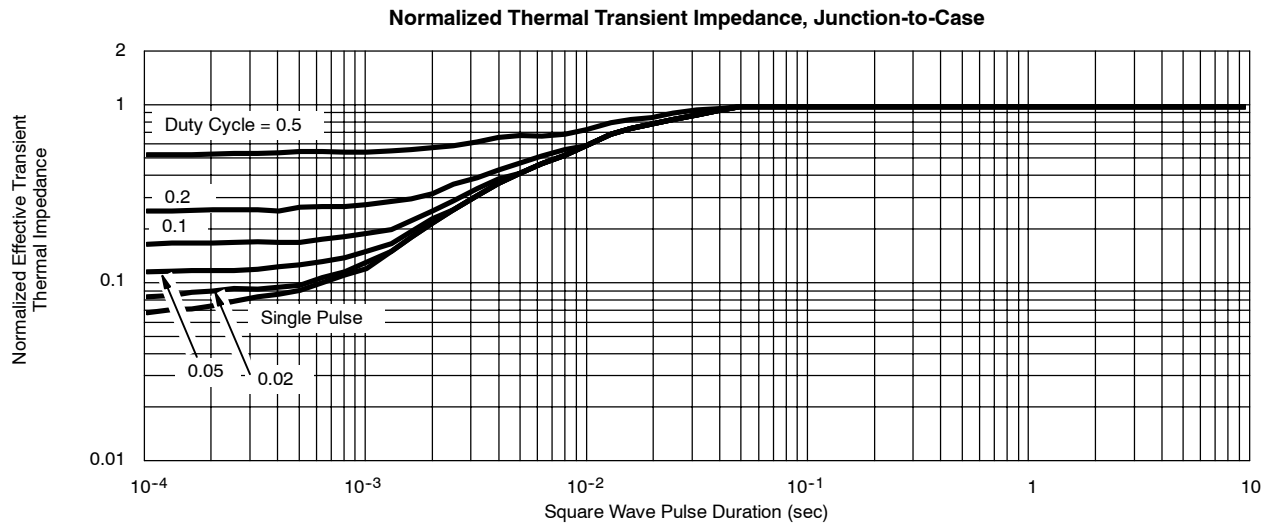
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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