FAIRCHILD SEMICONDUCTOR®

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RMPA39000

37–40 GHz GaAs MMIC Power Amplifier

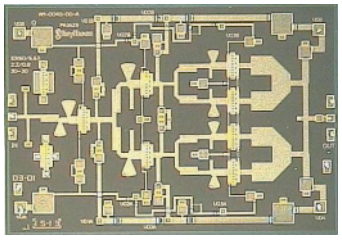
General Description

The Fairchild Semiconductor RMPA39000 is a high efficiency power amplifier designed for use in point to point and point to multi-point radios, and various communications applications. The RMPA39000 is a 3-stage GaAs MMIC amplifier utilizing our advanced 0.15µm gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.

Features

- 24dB small signal gain (typ.)
- 29dBm saturated power out (typ.)
- Circuit contains individual source vias
- Chip size 4.28mm x 2.90mm x 50µm

Device



Absolute Ratings

Symbol	Parameter	Ratings	Units
Vd	Positive DC Voltage (+5V Typical)	+6	V
Vg	Negative DC Voltage	-2	V
Vdg	Simultaneous (Vd–Vg)	+8	V
I_D	Positive DC Current	1092	mA
P_{IN}	RF Input Power (from 50Ω source)	+20	dBm
T_C	Operating Baseplate Temperature	-30 to +85	°C
T_{STG}	Storage Temperature Range	-55 to +125	°C
R_{JC}	Thermal Resistance (Channel to Backside)	17	°C/W

Electrical Characteristics 50Ω system, Vd = +5V, Quiescent current (Idq) = 700mA

Parameter	Min	Typ	Max	Units
Frequency Range	37		40	GHz
Gain Supply Voltage (Vg)[1]		-0.15		V
Gain Small Signal at Pin = 0dBm	20	24		dB
Gain Variation vs. Frequency		±1		dB
Power Output at 1dB Compression		28		dBm
Power Output Saturated (Pin = +13dBm)	27.5	29		dBm
Drain Current at Pin = 0dBm		700		mA
Drain Current at P1dB Compression		730		mA
Drain Current at Psat (Pin = +13dBm)		750		mA
Power Added Efficiency (PAE) at P1dB		17		%
OIP3 (17dBm/Tone) (10 MHz Tone Sep.)		36		dBm
Input Return Loss (Pin = -10dBm)		8		dB
Output Return Loss (Pin = -10dBm)		7		dB

Note:
1. Typical range of the negative gate voltage is -0.5V to 0.0V to set typical Idq of 700mA.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mils long corresponding to a typical 2 mil gap between the chip and the substrate material.

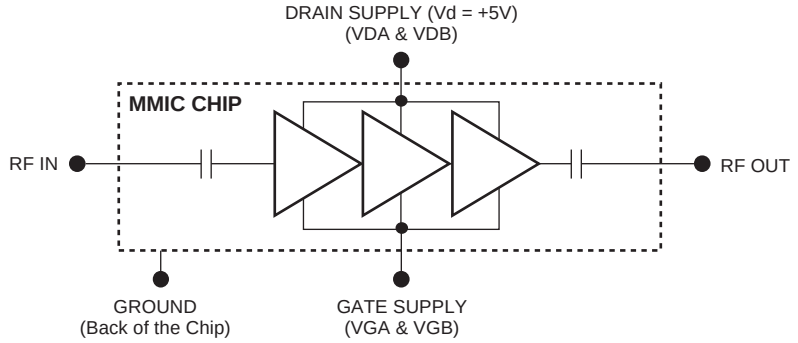
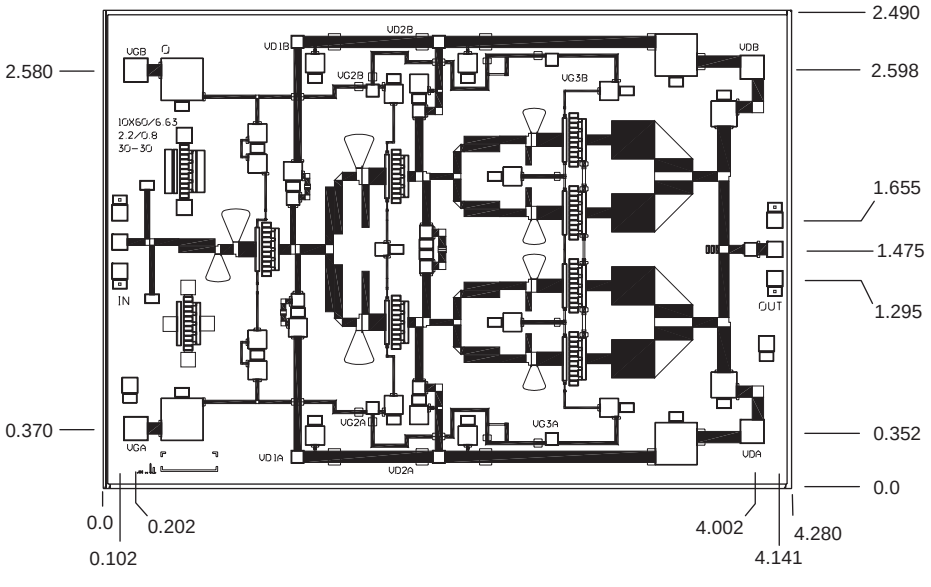


Figure 1. Functional Block Diagram



Dimensions in mm

Figure 2. Chip Layout and Bond Pad Locations
(Chip Size is 4.28mm x 2.90mm x 50µm. Back of chip is RF and DC Ground)

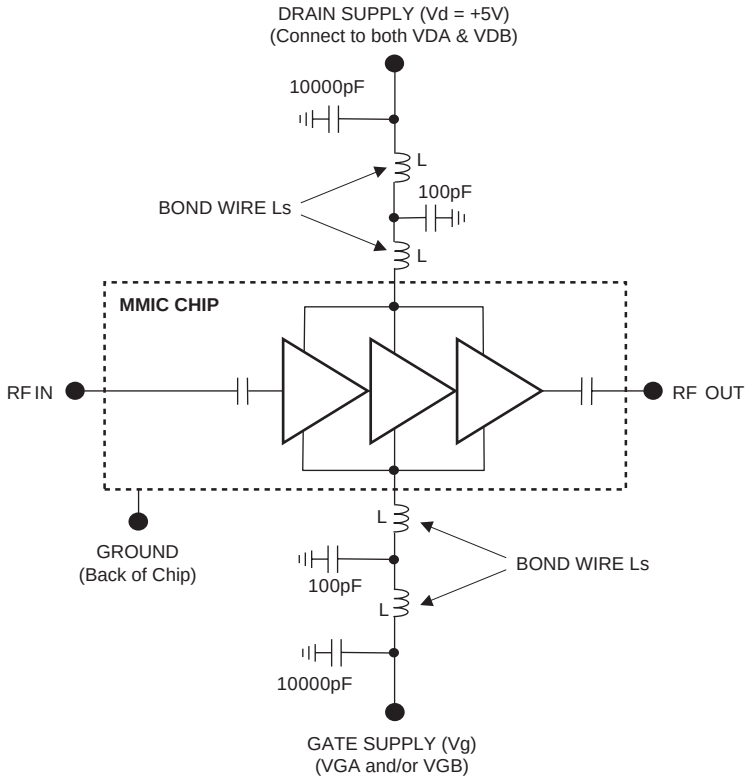
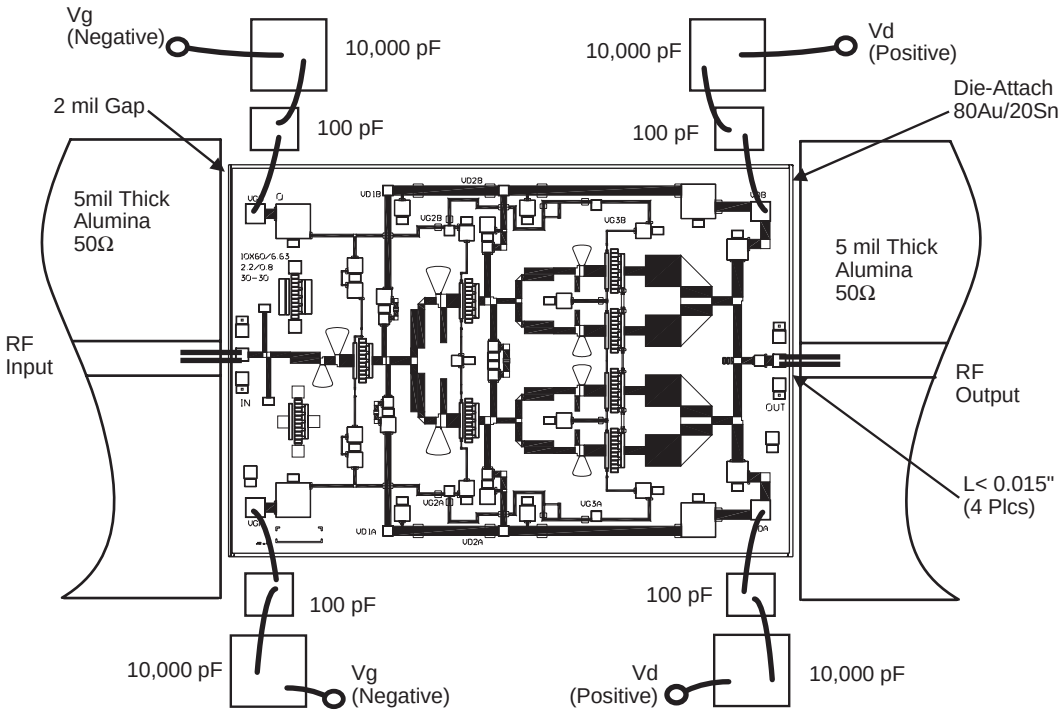


Figure 3. Recommended Application Schematic Circuit Diagram



Note:
Use 0.003" x 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief. Vd should be biased from 1 supply on both sides as shown. Vg can be biased from either or both sides from 1 supply.

Figure 4. Recommended Assembly and Bonding Diagram

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier.

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +5V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq = 700mA.

Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).

Note: An example auto bias sequencing circuit to apply negative gate voltage and positive drain voltage for the above procedure is shown below.

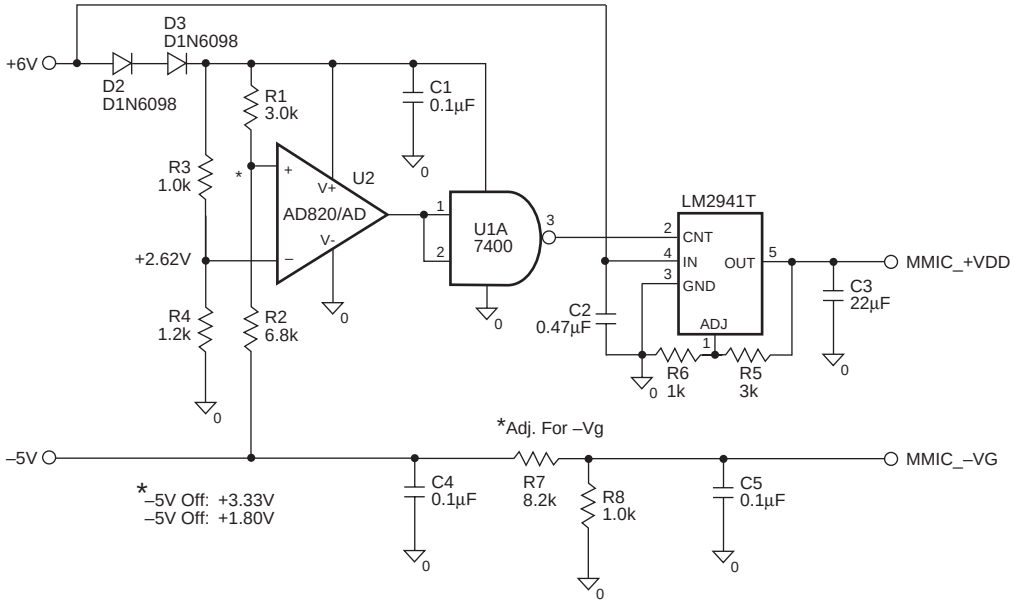
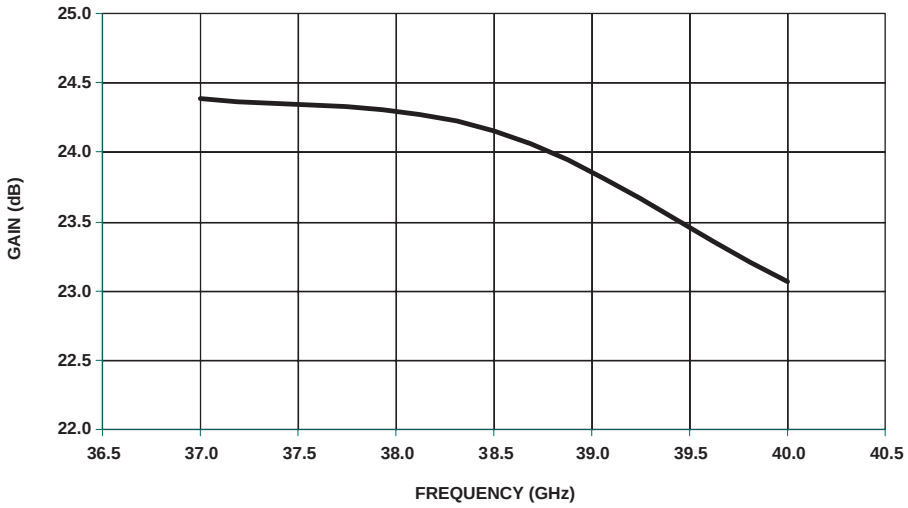


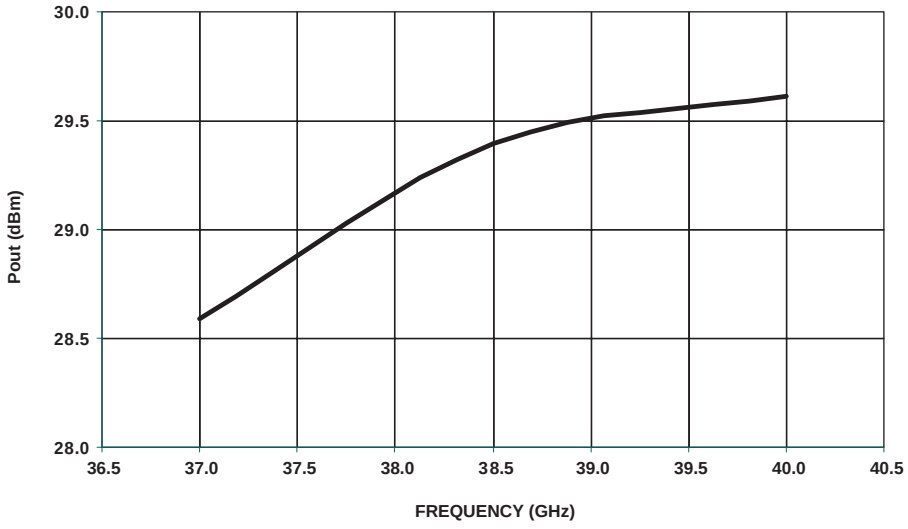
Figure 5. Application Information Auto-Bias Circuit

Typical Characteristics

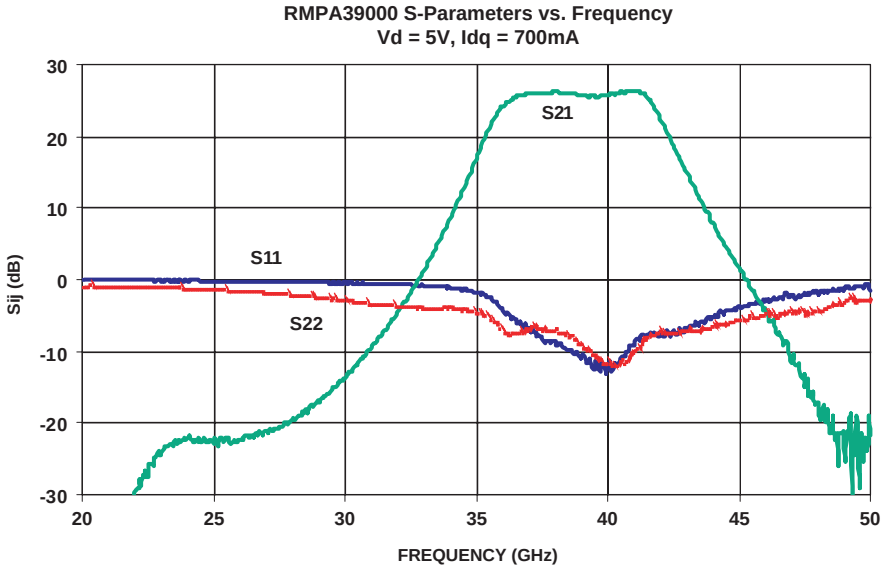
RMPA39000 Gain vs. Frequency
Vd = 5V, Id = 700mA

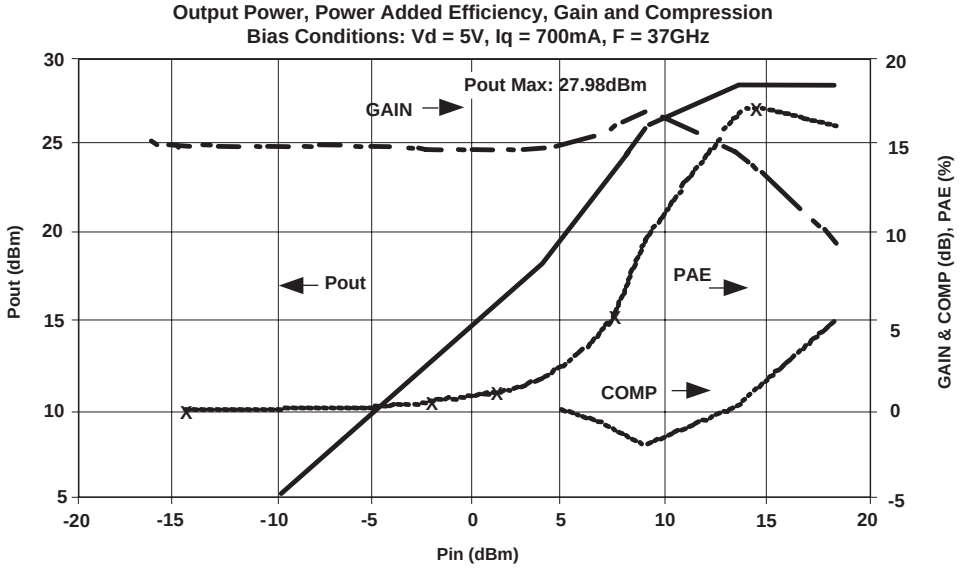


RMPA39000 Saturated Pout vs. Frequency
Vd = 5V, Id = 700mA

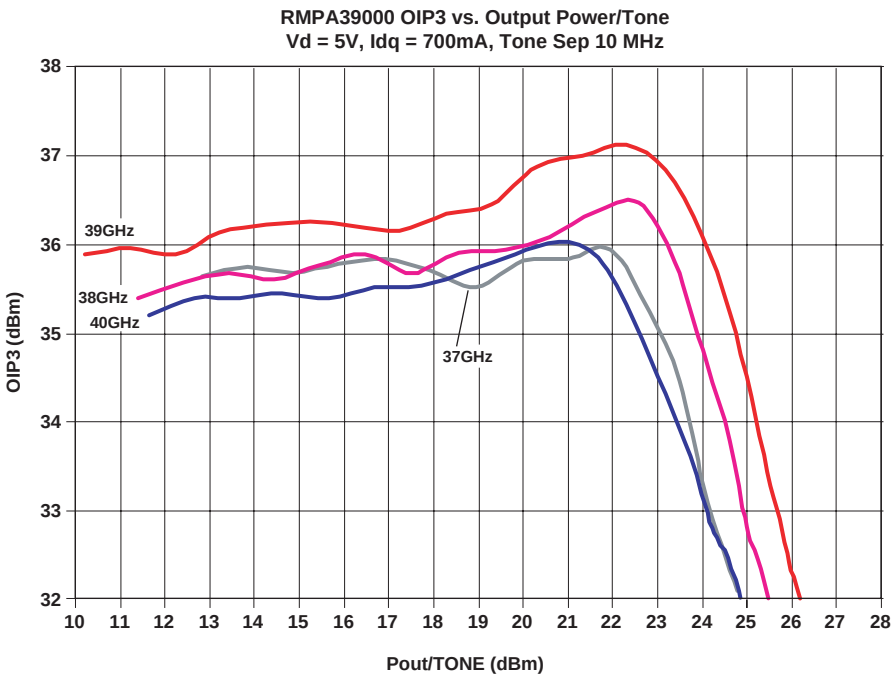


Typical Characteristics (Continued)





Typical Characteristics (Continued)



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CoolFET™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
DOME™	GTO™	MICROWIRE™	QT Optoelectronics™	TinyLogic®
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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