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# 2SJ399

Silicon P-Channel MOS FET

# HITACHI

ADE-208-267  
1st. Edition

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## Application

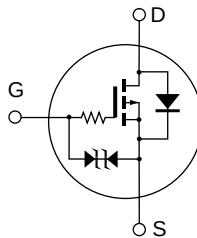
Low frequency power switching

## Features

- Low on-resistance
- Small package
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for low signal load switch.

## Outline

MPAK



1. Source
2. Gate
3. Drain

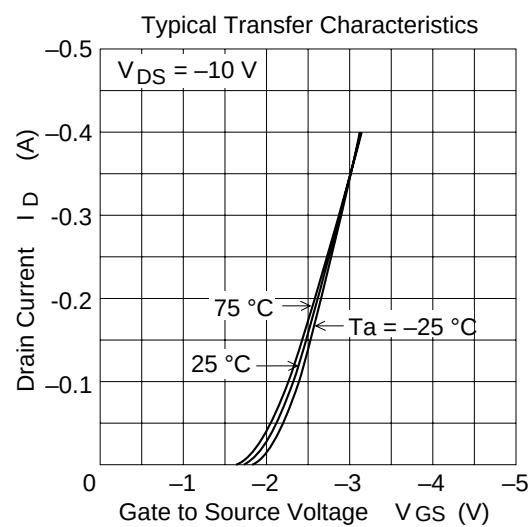
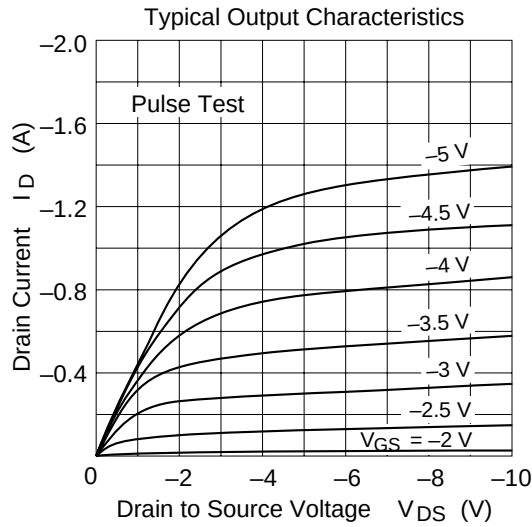
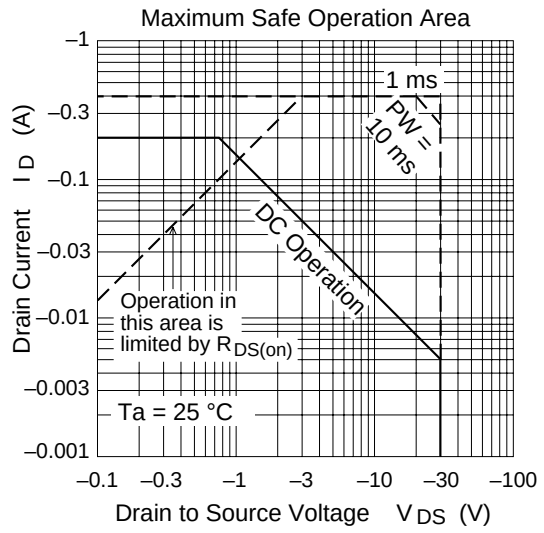
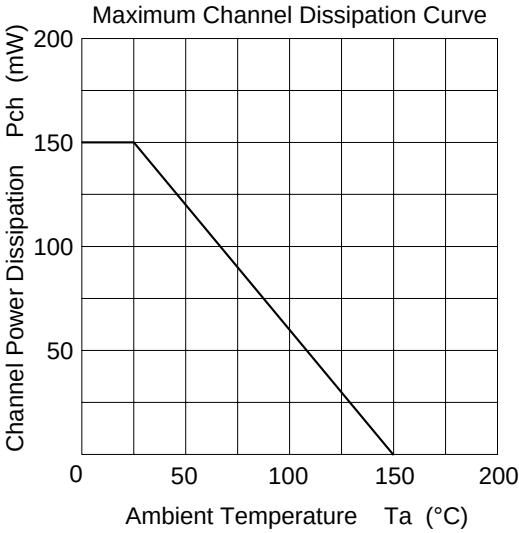
Absolute Maximum Ratings (Ta = 25°C)

| Item                                      | Symbol                              | Ratings     | Unit |
|-------------------------------------------|-------------------------------------|-------------|------|
| Drain to source voltage                   | V <sub>DSS</sub>                    | −30         | V    |
| Gate to source voltage                    | V <sub>GSS</sub>                    | ±20         | V    |
| Drain current                             | I <sub>D</sub>                      | −0.2        | A    |
| Drain peak current                        | I <sub>D(pulse)</sub> <sup>*1</sup> | −0.4        | A    |
| Body to drain diode reverse drain current | I <sub>DR</sub>                     | −0.2        | A    |
| Channel dissipation                       | Pch                                 | 150         | mW   |
| Channel temperature                       | Tch                                 | 150         | °C   |
| Storage temperature                       | Tstg                                | −55 to +150 | °C   |

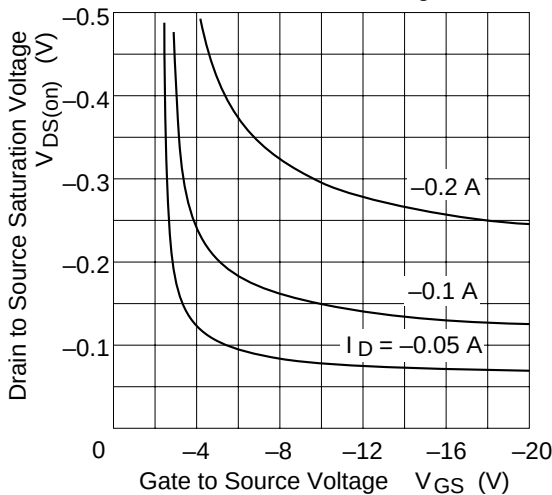
Notes: 1. PW ≤ 100 μs, duty cycle ≤ 10%  
2. Marking is “ZF–”

Electrical Characteristics (Ta = 25°C)

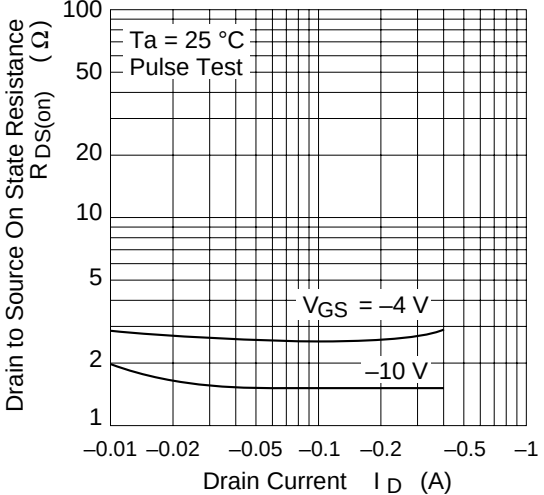
| Item                                       | Symbol               | Min  | Typ  | Max  | Unit | Test conditions                                                  |
|--------------------------------------------|----------------------|------|------|------|------|------------------------------------------------------------------|
| Drain to source breakdown voltage          | V <sub>(BR)DSS</sub> | −30  | —    | —    | V    | I <sub>D</sub> = −100 μA, V <sub>GS</sub> = 0                    |
| Gate to source breakdown voltage           | V <sub>(BR)GSS</sub> | ±20  | —    | —    | V    | I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0                    |
| Gate to source leak current                | I <sub>GSS</sub>     | —    | —    | ±2   | μA   | V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0                     |
| Zero gate voltage drain current            | I <sub>DSS</sub>     | —    | —    | −1   | μA   | V <sub>DS</sub> = −30 V, V <sub>GS</sub> = 0                     |
| Gate to source cutoff voltage              | V <sub>GS(off)</sub> | −1.0 | —    | −2.0 | V    | I <sub>D</sub> = −10 μA, V <sub>DS</sub> = −5 V                  |
| Static drain to source on state resistance | R <sub>DS(on)</sub>  | —    | 2.7  | 5.0  | Ω    | I <sub>D</sub> = −20 mA<br>V <sub>GS</sub> = −4 V <sup>*1</sup>  |
|                                            |                      | —    | 2.0  | 3.0  | Ω    | I <sub>D</sub> = −10 mA<br>V <sub>GS</sub> = −10 V <sup>*1</sup> |
| Input capacitance                          | Ciss                 | —    | 1.1  | —    | pF   | V <sub>DS</sub> = −10 V                                          |
| Output capacitance                         | Coss                 | —    | 22.3 | —    | pF   | V <sub>GS</sub> = 0                                              |
| Reverse transfer capacitance               | Crss                 | —    | 0.17 | —    | pF   | f = 1 MHz                                                        |
| Turn-on delay time                         | t <sub>d(on)</sub>   | —    | 530  | —    | ns   | I <sub>D</sub> = −0.1 A                                          |
| Rise time                                  | t <sub>r</sub>       | —    | 2170 | —    | ns   | V <sub>GS</sub> = −10 V                                          |
| Turn-off delay time                        | t <sub>d(off)</sub>  | —    | 7640 | —    | ns   | R <sub>L</sub> = 100 Ω                                           |
| Fall time                                  | t <sub>f</sub>       | —    | 7690 | —    | ns   | PW = 5 μs                                                        |



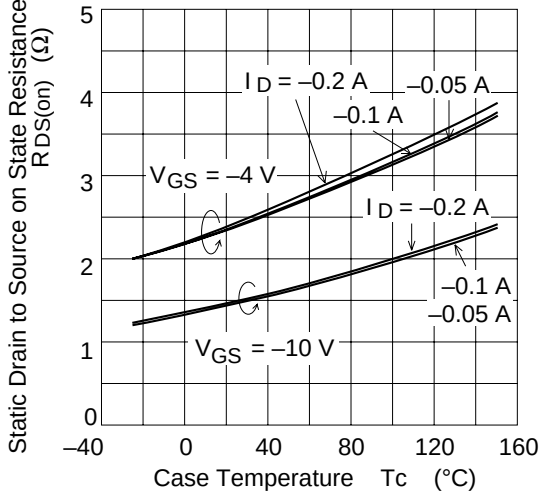
Drain to Source Saturation Voltage vs.  
Gate to Source Voltage



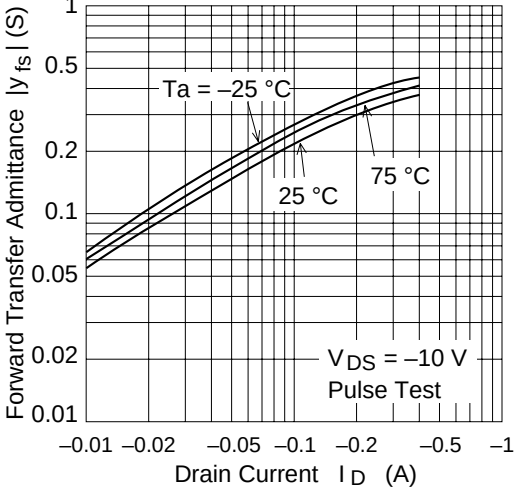
Static Drain to Source on State Resistance  
vs. Drain Current

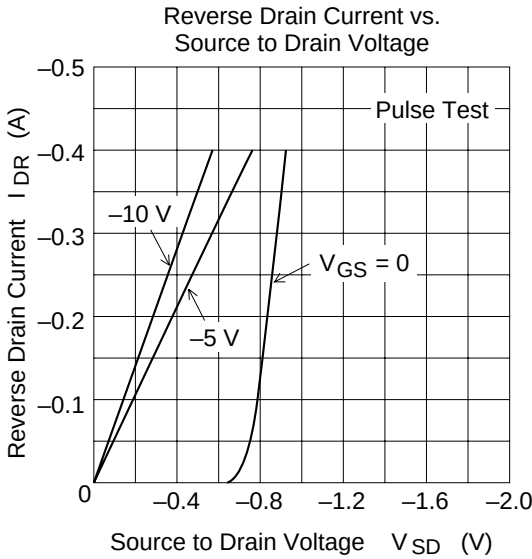
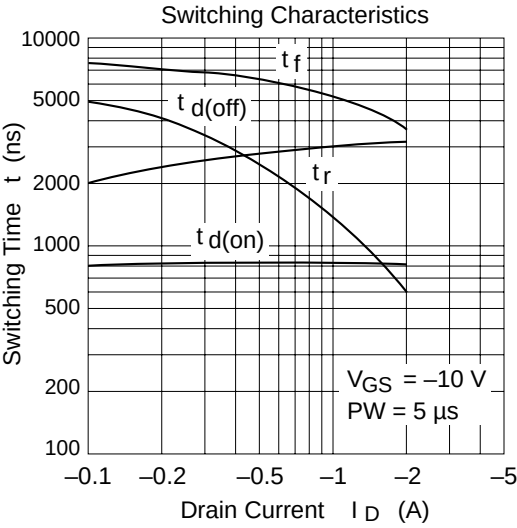
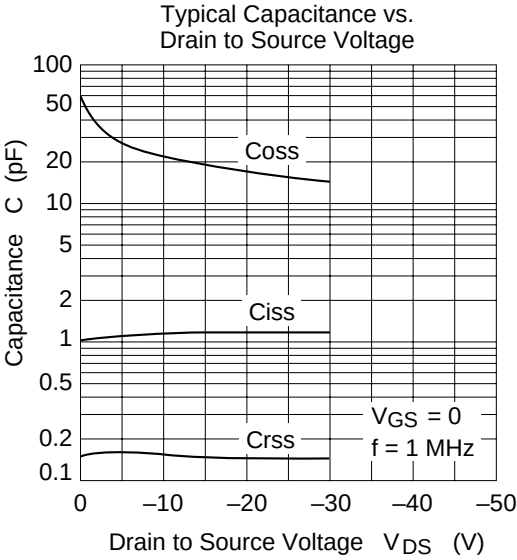


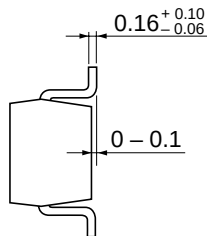
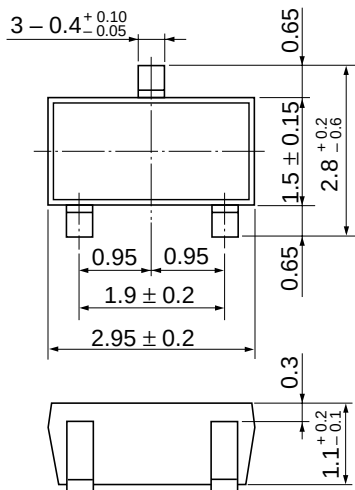
Static Drain to Source on State Resistance  
vs. Temperature



Forward Transfer Admittance vs.  
Drain Current







|                          |          |
|--------------------------|----------|
| Hitachi Code             | MPAK     |
| JEDEC                    | —        |
| EIAJ                     | Conforms |
| Weight (reference value) | 0.011 g  |

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