National Semiconductor

MF6 6th Order Switched Capacitor Butterworth Lowpass Filter

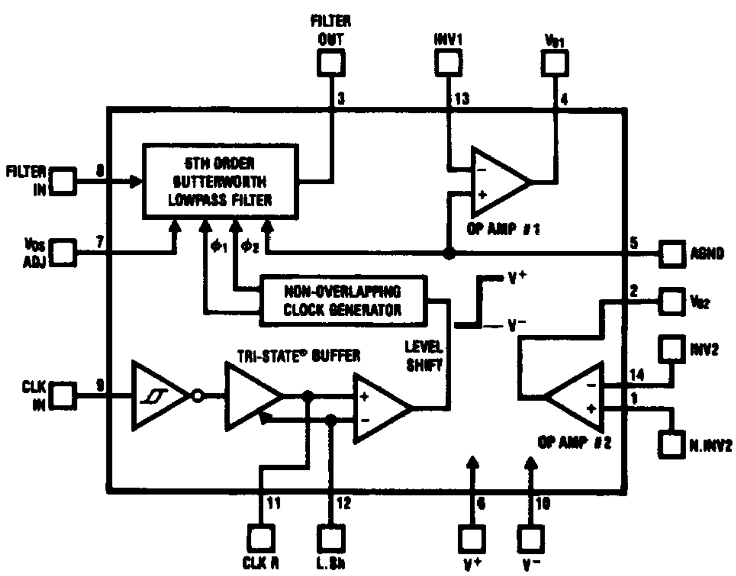
General Description

The MF6 is a versatile easy to use, precision 6th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF6-50) or 100 to 1 (MF6-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or an external TTL or CMOS logic compatible clock can be used for tighter cutoff frequency control. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF6 sections for higher order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications.

Features

- No external components
- 14-pin DIP or 14-pin wide-body S.O. package
- Cutoff frequency accuracy of ±0.3% typical
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Two uncommitted op amps available
- 5V to 14V total supply voltage
- Cutoff frequency set by external or internal clock

Block and Connection Diagrams



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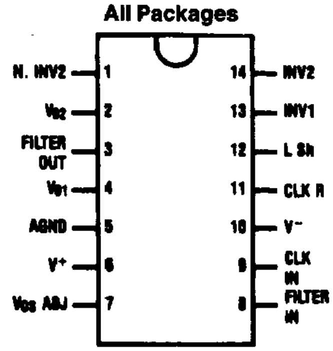
All Packages



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Top View

Order Number MF6CWM-50 or MF6CWM-100
See NS Package Number M14B

Order Number MF6CN-50 or MF6CN-100
See NS Package Number N14A

Order Number MF6CJ-50 or MF6CJ-100
See NS Package Number J14A

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Voltage at Any Pin	$V^- - 0.2V, V^+ + 0.2V$
Input Current at Any Pin (Note 13)	5 mA
Package Input Current (Note 13)	20 mA
Power Dissipation (Note 14)	500 mW
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 12)	800V
Soldering Information	
N Package (10 sec.)	260°C
J Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 11)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF6CN-50, MF6CN-100	$0°C \le T_A \le +70°C$
MF6CWM-50, MF6CWM-100	$0°C \le T_A \le +70°C$
MF6CJ-50, MF6CJ-100	$-40°C \le T_A \le +85°C$
Supply Voltage ($V_S = V^+ - V^-$)	5V to 14V

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \le 250$ kHz (see Note 3) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF6CWM-50, MF6CWM-100, MF6CN-50, MF6CN-100			MF6CJ-50, MF6CJ-100			Units
		Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V, V^- = -5V$								
f_c, Cutoff Frequency Range (Note 1) — MF6-50 Min Max MF6-100 Min Max				**0.1** **20k** **0.1** **10k**			**0.1** **20k** **0.1** **10k**	Hz
Total Supply Current	f_{CLK} = 250 kHz	4.0	6.0	**8.5**	4.0	**8.5**		mA
Maximum Clock Feedthrough — Filter Output Op Amp 1 Out Op Amp 2 Out		30 25 20			30 25 20			mV (peak-to-peak)
H_o, DC Gain	$R_{source} \le 2$ kΩ	0.0	±0.30	±**0.30**	0.0	±**0.30**		dB
f_{CLK}/f_c, Clock to Cutoff Frequency Ratio — MF6-50 MF6-100		49.27±0.3% 98.97±0.3%	49.27±1% 98.97±1%	**49.27**±**1%** **98.97**±**1%**	49.27±0.3% 98.97±0.3%	**49.27**±**1%** **98.97**±**1%**		
DC Offset Voltage — MF6-50 MF6-100		−200 −400			−200 −400			mV
Minimum Output Voltage Swing	R_L = 10 kΩ	+4.0 −4.1	+3.5 −3.8	+**3.5** −**3.5**	+4.0 −4.1	+**3.5** −**3.5**		V
Maximum Output Short Circuit Current (Note 6) — Source Sink		50 1.5	60 2.0	**80** **3.0**	50 1.5	**80** **3.0**		mA
Dynamic Range (Note 2) — MF6-50 MF6-100		83 81			83 81			dB
Additional Magnitude Response Test Points (Note 4) — MF6-50	f_{CLK} = 250 kHz f = 6000 Hz f = 4500 Hz	 −9.47 −0.92	 −9.47±0.5 −0.92±0.2	 −**9.47**±**0.65** −**0.92**±**0.3**	 −9.47 −0.92	 −**9.47**±**0.65** −**0.92**±**0.3**		dB
MF6-100	f_{CLK} = 250 kHz f = 3000 Hz f = 2250 Hz	 −9.48 −0.97	 −9.48±0.5 −0.97±0.2	 −**9.48**±**0.65** −**0.97**±**0.3**	 −9.48 −0.97	 −**9.48**±**0.65** −**0.97**±**0.3**		dB

Filter Electrical Characteristics (Continued)

The following specifications apply for $f_{CLK} \leq 250$ kHz (see Note 3) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF6CWM-50, MF6CWM-100 MF6CN-50, MF6CN-100 Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	MF6CJ-50, MF6CJ-100 Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Units
$V^+ = +5V, V^- = -5V$ (Continued)								
Attenuation Rate MF6-50	f_{CLK} = 250 kHz f_1 = 6000 Hz f_2 = 8000 Hz		−36	**−36**		**−36**		dB/ octave
Attenuation Rate MF6-100	f_{CLK} = 250 kHz f_1 = 3000 Hz f_2 = 4000 Hz		−36	**−36**		**−36**		dB/ octave
$V^+ = +2.5V, V^- = -2.5V$								
f_c, Cutoff Frequency Range (Note 1) MF6-50 Min Max MF6-100 Min Max				**0.1** **10k** **0.1** **5k**			**0.1** **10k** **0.1** **5k**	Hz
Total Supply Current	f_{CLK} = 250 kHz	2.5	4.0	**4.0**	2.5	**4.0**		mA
Maximum Clock Feedthrough Filter Output Op Amp 1 Out Op Amp 2 Out		20 15 10			20 15 10			mV (peak-to-peak)
H_o, DC Gain	$R_{source} \leq 2$ kΩ	0.0	±0.30	**±0.30**	0.0	**±0.30**		dB
f_{CLK}/f_c, Clock to Cutoff Frequency Ratio MF6-50 MF6-100		49.10 ± 0.3% 98.65 ± 0.3%	49.10 ± 2% 98.65 ± 2%	**49.10 ± 3%** **98.65 ± 2.25%**	49.10 ± 0.3% 98.65 ± 0.3%	**49.10 ± 3%** **98.65 ± 2.25%**		
DC Offset Voltage MF6-50 MF6-100		−200 −400			−200 −400			mV
Minimum Output Voltage Swing	R_L = 10 kΩ	+1.5 −2.2	+1.0 −1.7	**+1.0** **−1.5**	+1.5 −2.2	**+1.0** **−1.5**		V
Maximum Output Short Circuit Current (Note 6) Source Sink		28 0.5	40 1.0	**50** **1.5**	28 0.5	**50** **1.5**		mA
Dynamic Range (Note 2)		77			77			dB
Additional Magnitude Response Test Points (Note 4) MF6-50	f_{CLK} = 250 kHz f = 6000 Hz f = 4500 Hz	−9.54 −0.96	−9.54 ± 0.5 −0.96 ± 0.2	**−9.54 ± 0.65** **−0.96 ± 0.3**	−9.54 −0.96	**−9.54 ± 0.65** **−0.96 ± 0.3**		dB
MF6-100	f_{CLK} = 250 kHz f = 3000 Hz f = 2250 Hz	−9.67 −1.01	−9.67 ± 0.5 −1.01 ± 0.2	**−9.67 ± 0.65** **−1.01 ± 0.3**	−9.67 −1.01	**−9.67 ± 0.65** **−1.01 ± 0.3**		dB
Attenuation Rate MF6-50	f_{CLK} = 250 kHz f_1 = 6000 Hz f_2 = 8000 Hz		−36	**−36**		**−36**		dB/ octave
Attenuation Rate MF6-100	f_{CLK} = 250 kHz f_1 = 3000 Hz f_2 = 4000 Hz		−36	**−36**		**−36**		dB/ octave

Op Amp Electrical Characteristics

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Parameter		Conditions	MF6CN-50, MF6CN-100, MF6CWM-50, MF6CWM-100			MF6CJ-50, MF6CJ-100			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V, V^- = -5V$									
Input Offset Voltage			±8.0	±20	**±20**	±8.0	**±20**		mV
Input Bias Current			10			10			pA
CMRR (Op Amp #2 Only)		$V_{CM1} = 1.8V$, $V_{CM2} = -2.2V$	60	55		60	55		dB
Output Voltage Swing		$R_L = 10\ k\Omega$	+4.0 −4.5	+3.8 −4.0	**+3.6** **−4.0**	+4.0 −4.5	**+3.6** **−4.0**		V
Maximum Output Short Circuit Current (Note 6)	Source Sink		54 2.0	65 4.0	**80** **6.0**	54 2.0	**80** **6.0**		mA
Slew Rate			7.0			7.0			V/µs
DC Open Loop Gain			72			72			dB
Gain Bandwidth Product			1.2			1.2			MHz
$V^+ = +2.5V, V^- = -2.5V$									
Input Offset Voltage			±8.0	±20	**±20**	±8.0	**±20**		mV
Input Bias Current			10			10			pA
CMRR (Op-Amp #2 Only)		$V_{CM1} = +0.5V$, $V_{CM2} = -0.9V$	60	55		60	55		dB
Output Voltage Swing		$R_L = 10\ k\Omega$	+1.5 −2.2	+1.3 −1.7	**+1.1** **−1.7**	+1.5 −2.2	**+1.1** **−1.7**		V
Maximum Output Short Circuit Current (Note 6)	Source Sink		24 1.0	35 2.0	**50** **4.0**	24 1.0	**50** **4.0**		mA
Slew Rate			6.0			6.0			V/µs
DC Open Loop Gain			67			67			dB
Gain Bandwidth Product			1.2			1.2			MHz

Logic Input-Output Electrical Characteristics

The following specifications apply for $V^- = 0V$ (see Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions		MF6CN-50, MF6CN-100 MF6CWM-50, MF6CWM-100			MF6CJ-50, MF6CJ-100			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
TTL CLOCK INPUT, CLK R PIN (Note 7)										
Maximum V_{IL}, Logical "0" Input Voltage					0.8	**0.8**		**0.8**		V
Minimum V_{IH}, Logical "1" Input Voltage					2.0	**2.0**		**2.0**		V
Maximum Leakage Current at CLK R Pin		L Sh Pin at Mid- Supply			2.0	**2.0**		**2.0**		μA
SCHMITT TRIGGER										
V_{T+}, Positive Going Threshold Voltage	Min Max	$V^+ = 10V$		7.0	6.1 8.9	**6.1** **8.9**	7.0	**6.1** **8.9**		V
	Min Max	$V^+ = 5V$		3.5	3.1 4.4	**3.1** **4.4**	3.5	**3.1** **4.4**		V
V_{T-}, Negative Going Threshold Voltage	Min Max	$V^+ = 10V$		3.0	1.3 3.8	**1.3** **3.8**	3.0	**1.3** **3.8**		V
	Min Max	$V^+ = 5V$		1.5	0.6 1.9	**0.6** **1.9**	1.5	**0.6** **1.9**		V
Hysteresis ($V_{T+} - V_{T-}$)	Min Max	$V^+ = 10V$		4.0	2.3 7.6	**2.3** **7.6**	4.0	**2.3** **7.6**		V
	Min Max	$V^+ = 5V$		2.0	1.2 3.8	**1.2** **3.8**	2.0	**1.2** **3.8**		V
Minimum Logical "1" Output Voltage (Pin 11)		$I_o = -10\mu A$	$V^+ = 10V$ $V^+ = 5V$		9.0 4.5	**9.0** **4.5**		**9.0** **4.5**		V
Maximum Logical "0" Output Voltage (Pin 11)		$I_o = 10\mu A$	$V^+ = 10V$ $V^+ = 5V$		1.0 0.5	**1.0** **0.5**		**1.0** **0.5**		V
Minimum Output Source Current (Pin 11)		CLK R Tied to Ground	$V^+ = 10V$ $V^+ = 5V$	6.0 1.5	3.0 0.75	**3.0** **0.75**	6.0 1.5	**3.0** **0.75**		mA
Maximum Output Sink Current (Pin 11)		CLK R Tied to V^+	$V^+ = 10V$ $V^+ = 5V$	5.0 1.3	2.5 0.65	**2.5** **0.65**	5.0 1.3	**2.5** **0.65**		mA

Note 1: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 2: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μVrms for the MF6-50 and 250 μVrms for the MF6-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically 140 μVrms for both the MF6-50 and the MF6-100.

Note 3: The specifications for the MF6 have been given for a clock frequency (f_{CLK}) of 250 kHz and less. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±1.0% but the filter still maintains its magnitude characteristics. See Application Hints, Section 1.5.

Note 4: Besides checking the cutoff frequency (f_c) and the stopband attenuation at 2 f_c, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB.

Note 5: For simplicity all the logic levels have been referenced to $V^- = 0V$ and will scale accordingly for ±5V and ±2.5V supplies (except for the TTL input logic levels).

Note 6: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

Note 7: The MF6 is operating with symmetrical split supplies and L.Sh is tied to ground.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level.

Note 10: Design limits are guaranteed, but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 11: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified conditions.

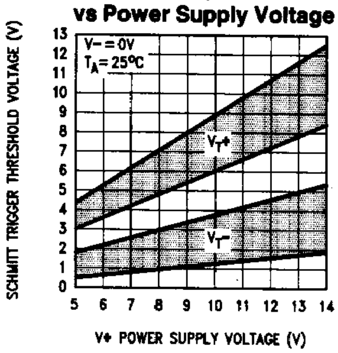
Note 12: Human body model, 100 pF discharged through a 1.5k Ω resistor.

Note 13: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

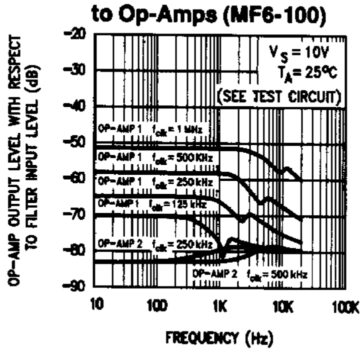
Note 14: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF6CN when board mounted is 67°C/W. For the MF6CJ this number decreases to 62°C/W. For MF6CWM, $\theta_{JA} = 78°C/W$.

Typical Performance Characteristics

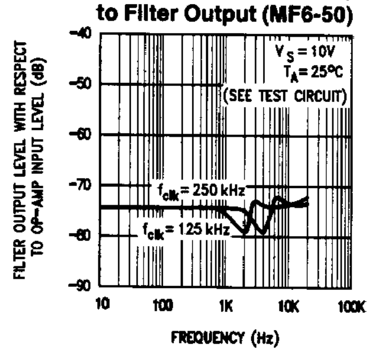
Schmitt Trigger Threshold Voltage vs Power Supply Voltage



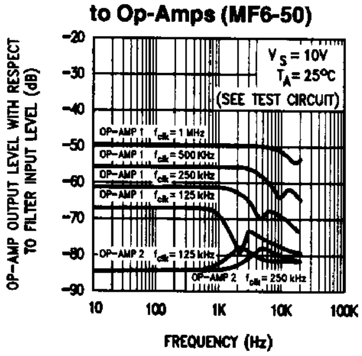
Crosstalk from Filter to Op-Amps (MF6-100)



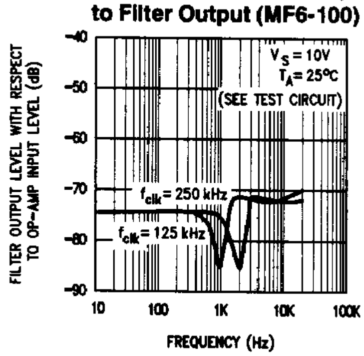
Crosstalk from Either Op-Amp to Filter Output (MF6-50)



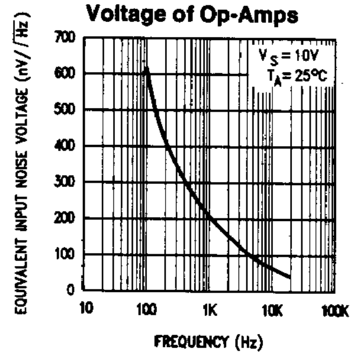
Crosstalk from Filter to Op-Amps (MF6-50)



Crosstalk from Either Op-Amp to Filter Output (MF6-100)



Equivalent Input Noise Voltage of Op-Amps



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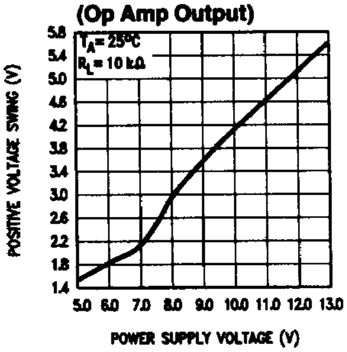
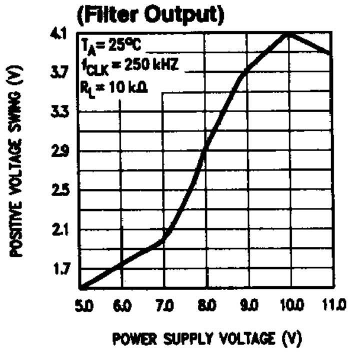
Typical Performance Characteristics (Continued)

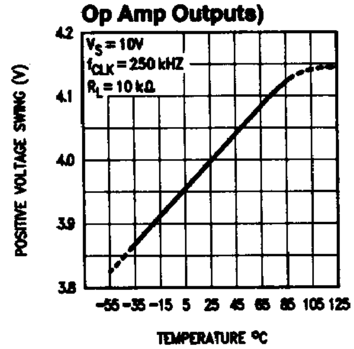
Positive Voltage Swing vs Power Supply Voltage (Op Amp Output)



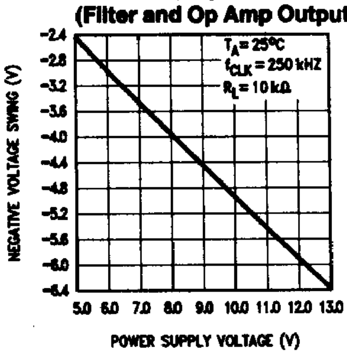
Positive Voltage Swing vs Power Supply Voltage (Filter Output)



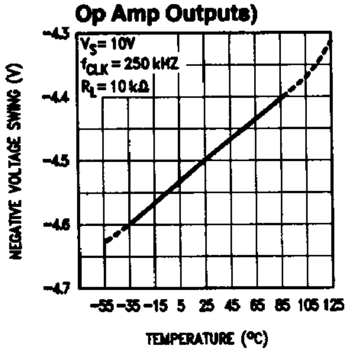
Positive Voltage Swing vs Temperature (Filter and Op Amp Outputs)



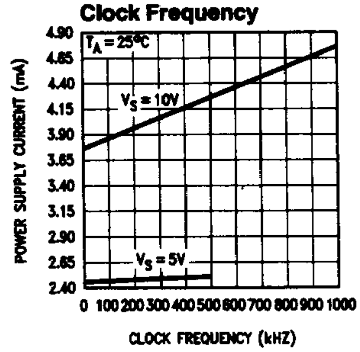
Negative Voltage Swing vs Power Supply Voltage (Filter and Op Amp Outputs)



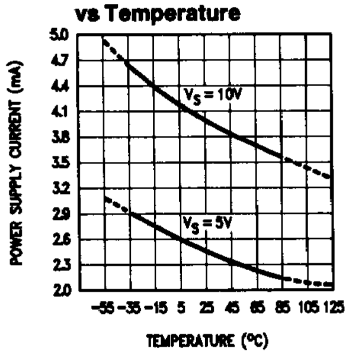
Negative Voltage Swing vs Temperature (Filter and Op Amp Outputs)



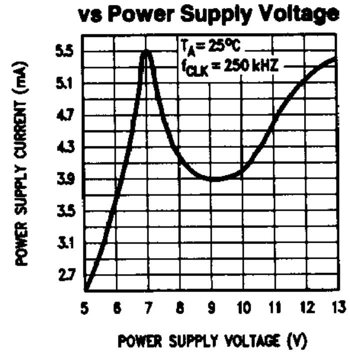
Power Supply Current vs Clock Frequency



Power Supply Current vs Temperature



Power Supply Current vs Power Supply Voltage



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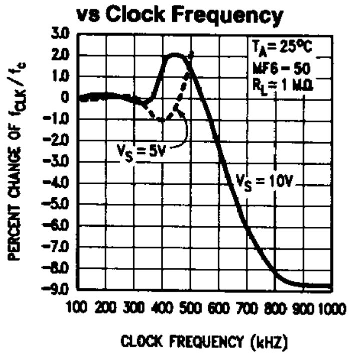
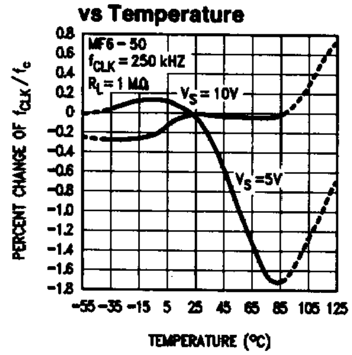
Typical Performance Characteristics (Continued)

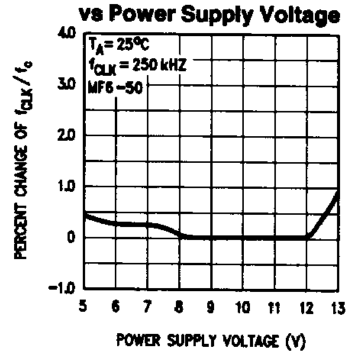
f_{CLK}/f_c Deviation vs Clock Frequency



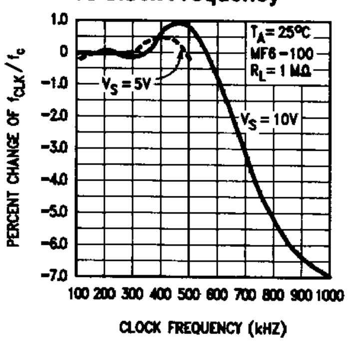
f_{CLK}/f_c Deviation vs Temperature



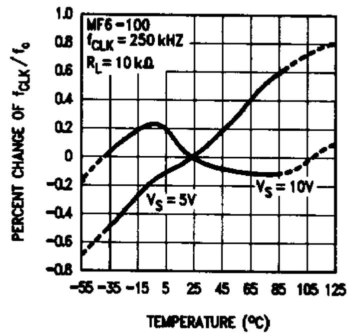
f_{CLK}/f_c Deviation vs Power Supply Voltage



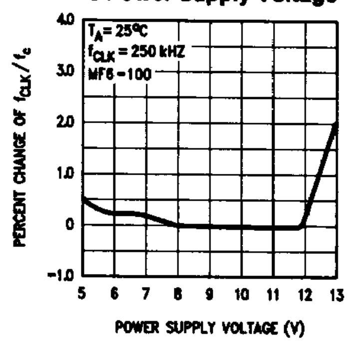
f_{CLK}/f_c Deviation vs Clock Frequency



f_{CLK}/f_c Deviation vs Temperature



f_{CLK}/f_c Deviation vs Power Supply Voltage



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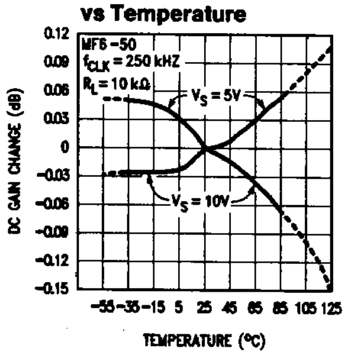
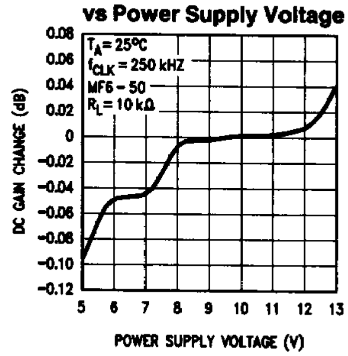
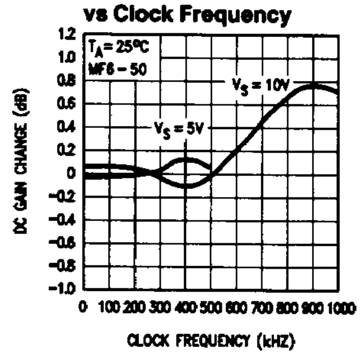
DC Gain Deviation vs Temperature



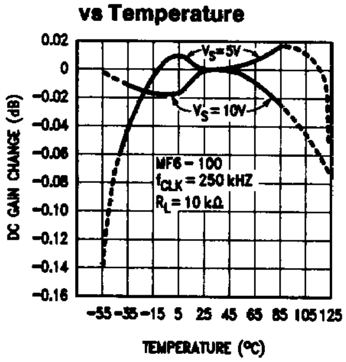
DC Gain Deviation vs Power Supply Voltage



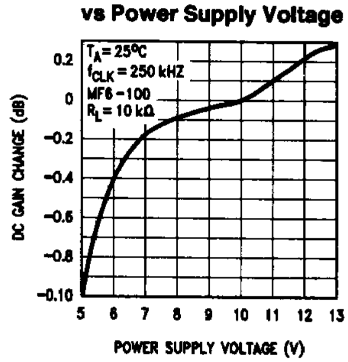
DC Gain Deviation vs Clock Frequency



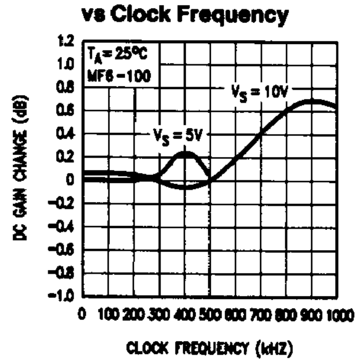
DC Gain Deviation vs Temperature



DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Clock Frequency



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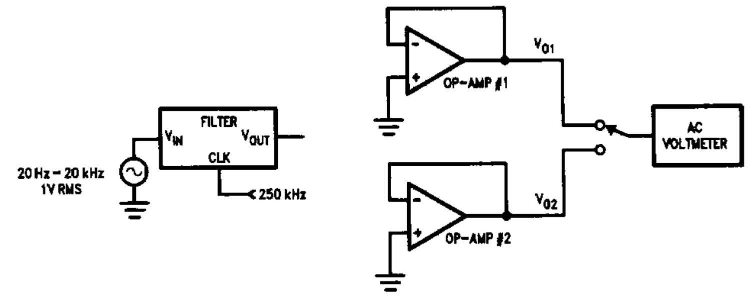
1

Crosstalk Test Circuits

From Filter to Opamps



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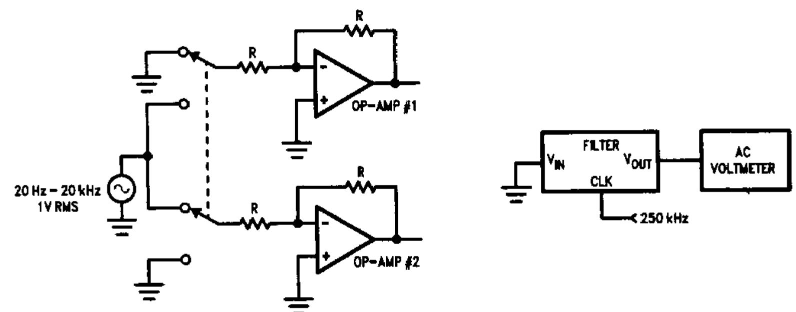
From Either Opamp to Filter Output



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Pin Descriptions (Pin Numbers)

Pin	Description
FILTER OUT (3)	The output of the lowpass filter. It will typically sink 0.9 mA and source 3 mA and swing to within 1V of each supply rail.
FILTER IN (8)	The input to the lowpass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (see section 1.4). For single supply operation the input signal must be biased to mid-supply or AC coupled.
V_{OS}ADJ (7)	This pin is used to adjust the DC offset of the filter output; if not used it must be tied to the AGND potential. (See section 1.3)
AGND (5)	The analog ground pin. This pin sets the DC bias level for the filter section and the non-inverting input of Op-Amp #1 and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see section 1.2). When tied to mid-supply this pin should be well bypassed.
V_{O1} (4), INV1 (13)	V_{O1} is the output and INV1 is the inverting input of Op-Amp #1. The non-inverting input of this Op-Amp is internally connected to the AGND pin.
V_{O2} (2), INV2 (14), NINV2 (1)	V_{O2} is the output, INV2 is the inverting input, and NINV2 is the non-inverting input of Op-Amp #2.
V^+(6), V^-(10)	The positive and negative supply pins. The total power supply range is 5V to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
CLK IN (9)	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self-clocking Schmitt-trigger oscillator (see section 1.1).
CLK R (11)	A TTL logic level clock input when in split supply operation (±2.5V to ±7V) and L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^-. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see section 1.1).
L. Sh (12)	Level shift pin, selects the logic threshold levels for the desired clock. When tied to V^- it enables an internal tri-state buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output.

Pin Descriptions (Pin Numbers) (Continued)

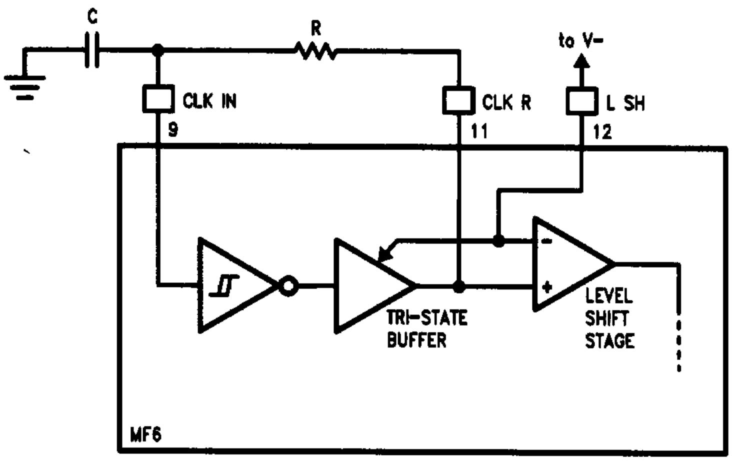
Pin	Description
L. Sh (12)	When the voltage level at this input exceeds [25%($V^+ - V^-$) + V^-] the internal tri-state buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level shift stage. The CLK R threshold level is now 2V above the voltage applied to the L. Sh pin. Driving the CLK R pin with TTL logic levels can be accomplished through the use of split supplies and by tying the L. Sh pin to system ground.

1.0 MF6 Application Hints

The MF6 is comprised of a non-inverting unity gain lowpass sixth order Butterworth switched capacitor filter section and two undedicated CMOS Op-Amps. The switched capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the lowpass filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance Section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock to cutoff frequency ratio (f_{CLK}/f_c) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock to cutoff frequency ratio (or the sampling rate) the closer this approximation is to the theoretical Butterworth response. The MF6 is available in f_{CLK}/f_c ratios of 50:1 (MF6-50) or 100:1 (MF6-100).

1.1 CLOCK INPUTS

The MF6 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. The oscillator's frequency is dependent on the buffer's threshold levels as well as on the resistor/capacitor tolerance (see *Figure 1*).



$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\frac{V_{T+}}{V_{T-}}\right]}$$

Typically for $V_{CC} = V^+ - V^- = 10V$:

$$f_{CLK} = \frac{1}{1.69\,RC}$$

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FIGURE 1. Schmitt Trigger R/C Oscillator

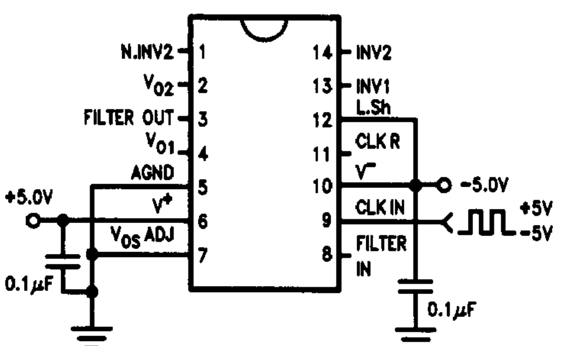

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FIGURE 2. Dual Supply Operation MF6 Driven with CMOS Logic Level Clock ($V_{IH} \geq 0.8\ V_{CC}$ and $V_{IL} \leq 0.2\ V_{CC}$ where $V_{CC} = V^+ - V^-$)

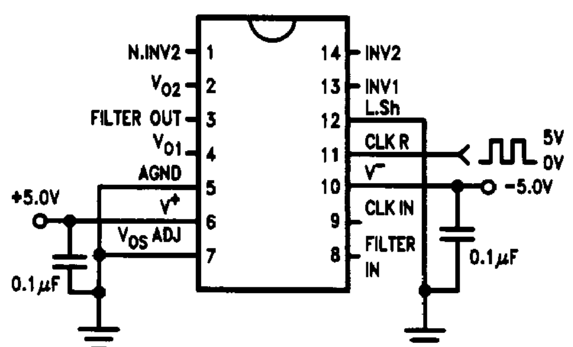

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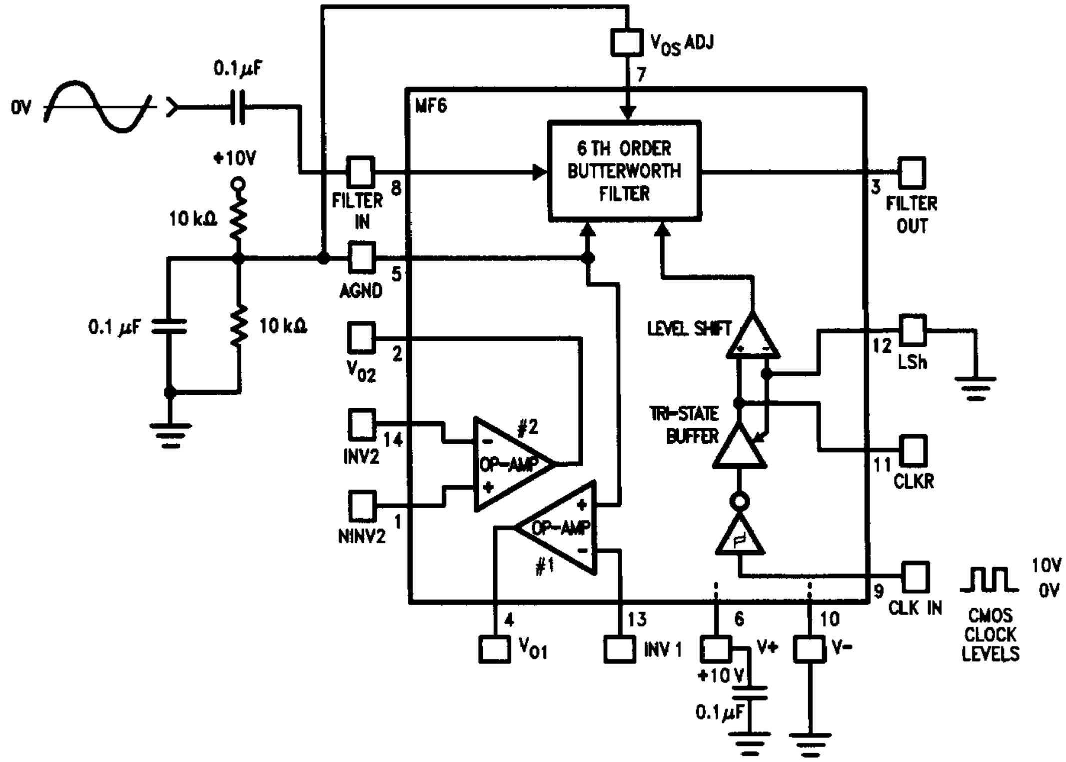
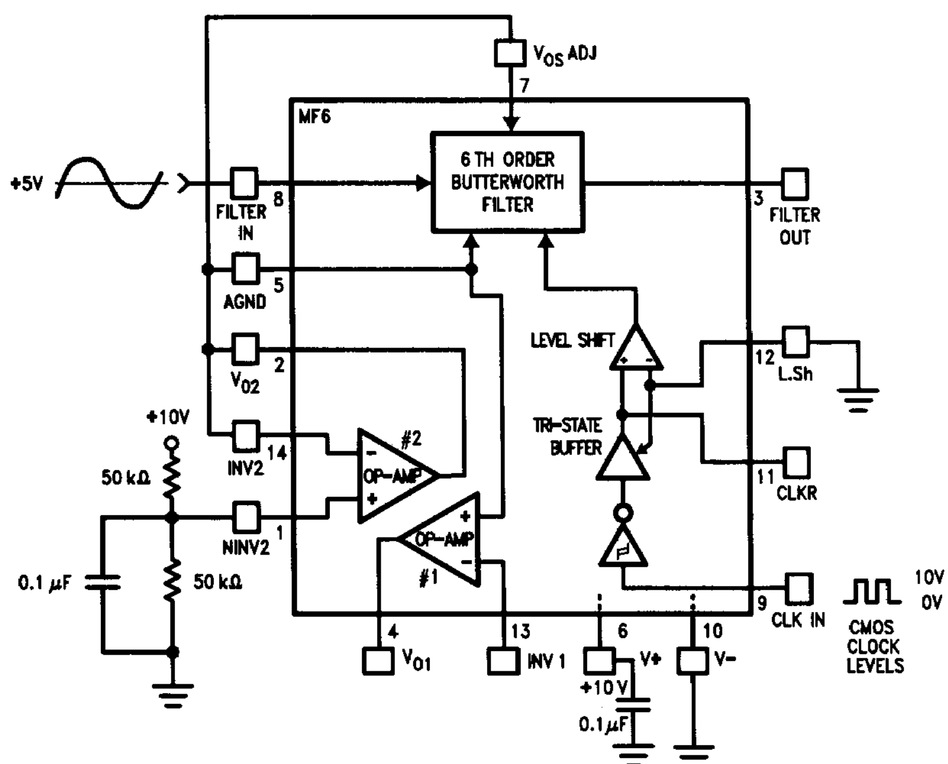
FIGURE 3. Dual Supply Operation MF6 Driven with TTL Logic Level Clock

Application Hints (Continued)



TL/H/5065–14

a) Resistor Biasing of AGND



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b) Using Op-Amp 2 to Buffer AGND

FIGURE 4. Single Supply Operation

Application Hints (Continued)

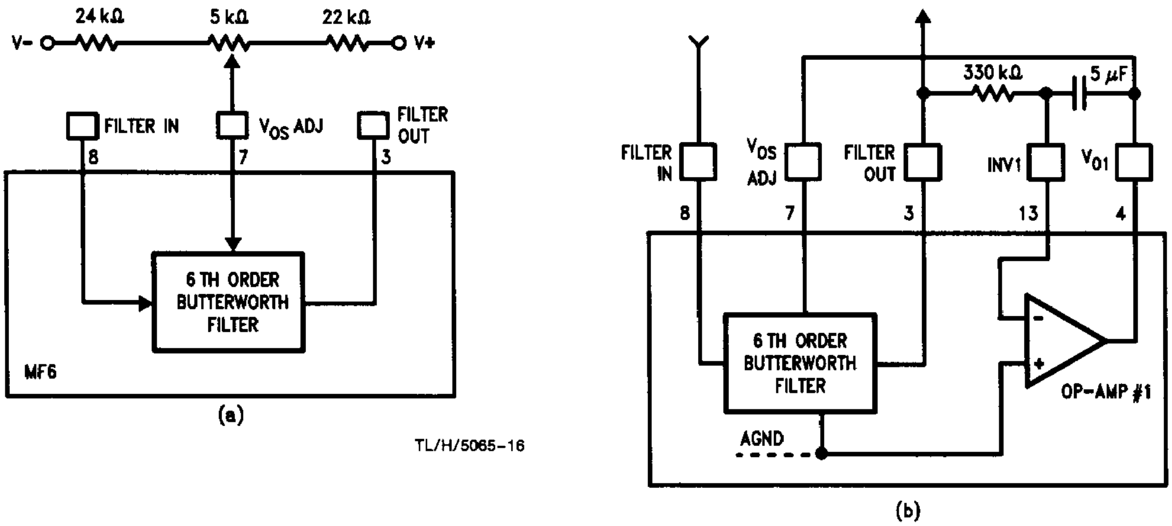


FIGURE 5. V_{OS} Adjust Schemes

Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accuracy in f_c is required an external clock can be used to drive the CLK R input of the MF6. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 μA) with split supplies and L. Sh tied to system ground. The logic level is programmed by the voltage applied to level shift (L. Sh) pin (See the Pin description for L. Sh pin).

1.2 POWER SUPPLY BIASING

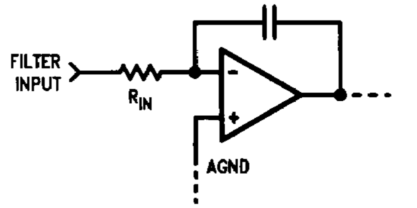
The MF6 can be biased from a single supply or dual split supplies. The split supply mode shown in *Figures 2* and *3* is the most flexible and easiest to implement. As discussed earlier split supplies, ±5V to ±7V, will enable the use of TTL or CMOS clock logic levels. *Figure 4* shows two schemes for single supply biasing. In this mode only CMOS clock logic levels can be used.

1.3 OFFSET ADJUST

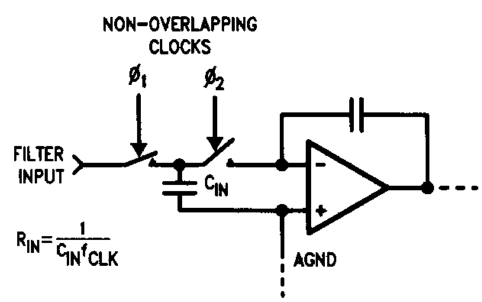
The VosADJ pin is used in adjusting the output offset level of the filter section. If this pin is not used it must be tied to the analog ground (AGND) level, either mid-supply for single ended supply operation or ground for split supply operation. This pin sets the zero reference for the output of the filter. The implementation of this pin can be seen in *Figure 5*. In 5(a), DC offset is adjusted using a potentiometer; in 5(b), the Op-Amp integrator circuit keeps the average DC output level at AGND. The circuit in 5(b) is therefore appropriate only for AC-coupled signals and signals biased at AGND.

1.4 INPUT IMPEDANCE

The MF6 lowpass filter input (FILTER IN pin) is not a high impedance buffer input. This input is a switched capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the input to the filter can be seen in *Figure 6*. The input capacitor charges to the input voltage (V_{in}) during one half of the clock period, during the second half the charge is



a) Equivalent Circuit for MF6 Filter Input



b) Actual Circuit for MF6 Filter Input

FIGURE 6. MF6 Filter Input

transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{in}V_{in}$, and since current is defined as the flow of charge per unit time the average input current becomes

$$I_{in} = Q/T$$

(where T equals one clock period) or

$$I_{in} = \frac{C_{in}V_{in}}{T} = C_{in}V_{in}f_{CLK}$$

The equivalent input resistor (R_{in}) then can be defined as

$$R_{in} = V_{in}/I_{in} = \frac{1}{C_{in}f_{CLK}}$$

The input capacitor is 2 pF for the MF6-50 and 1 pF for the

Application Hints (Continued)

MF6-100, so for the MF6-100

$$R_{in} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_c \times 100} = \frac{1 \times 10^{10}}{f_c}$$

and

$$R_{in} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

for the MF6-50. As shown in the above equations for a given cutoff frequency (f_c) the input impedance remains the same for the MF6-50 and the MF6-100. The higher the clock to center frequency ratio, the greater equivalent input resistance for a given clock frequency. As the cutoff frequency increases the equivalent input impedance decreases. This input resistance will form a voltage divider with the source impedance (R_{source}). Since R_{in} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity its overall gain is given by:

$$A_v = \frac{R_{in}}{R_{in} + R_{source}}$$

If the MF6-50 or the MF6-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{in} = \frac{1 \times 10^{10}}{10\ \text{kHz}} = 1\ \text{M}\Omega$$

In this example with a source impedance of 10k the overall gain, if the MF6 had an ideal gain of 1 or 0 dB, would be:

$$A_v = \frac{1\ \text{M}\Omega}{10\ \text{k}\Omega + 1\ \text{M}\Omega} = 0.99009 \text{ or } -86.4\ \text{mdB}$$

Since the maximum overall gain error for the MF6 is ±0.3 dB with a $R_s \le 2\ \text{k}\Omega$ the actual gain error for this case would be +0.21 dB to −0.39 dB.

1.5 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit caused by leakage currents through the internal switches discharging the stored charge on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ \text{Hz},\ I_{leakage} = 1\ \text{pA},\ C = 1\ \text{pF}$$

$$V = \frac{1\ \text{pA}}{1\ \text{pF}\ (100\ \text{Hz})} = 10\ \text{mV}$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors increases as the MF6 power supply voltage decreases. This causes a shift in the f_{CLK}/f_c ratio which will become noticeable when the clock frequency exceeds 250 kHz. The amplitude characteristic will stay within tolerance until f_{CLK} exceeds 500 kHz and will peak at about 0.5 dB at the corner frequency with a 1 MHz clock. The response of the MF6 is still a reasonable approximation of the ideal Butterworth lowpass characteristic as can be seen in *Figure 7*.

2.0 Designing with the MF6

Given any lowpass filter specification two equations will come in handy in trying to determine whether the MF6 will do the job. The first equation determines the order of the lowpass filter required:

$$n = \frac{\log (10^{0.1\,A_{min}} - 1) - \log (10^{0.1\,A_{max}} - 1)}{2 \log (f_s/f_b)} \qquad (1)$$

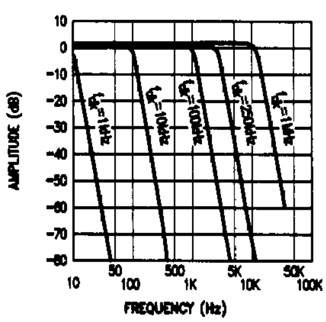


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FIGURE 7a. MF6-100 ±5V Supplies Amplitude Response

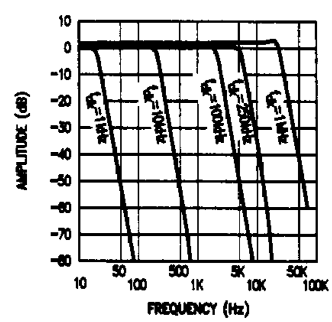

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FIGURE 7b. MF6-50 ±5V Supplies Amplitude Response

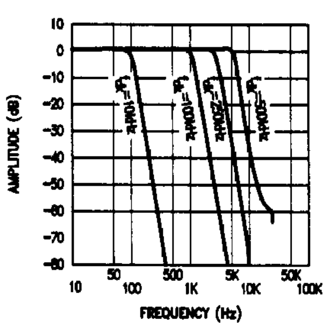

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FIGURE 7c. MF6-100 ±2.5V Supplies Amplitude Response

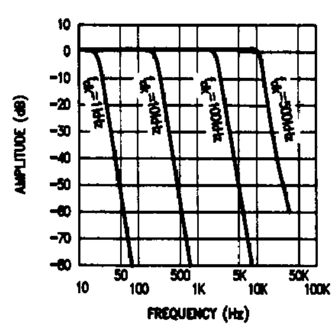

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FIGURE 7d. MF6-50 ±2.5V Supplies Amplitude Response

Designing with the MF6 (Continued)

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at frequency f_b. If the result of this equation is greater than 6, then more than a single MF6 is required.

The attenuation at any frequency can be found by the following equation:

$$Attn(f) = 10 \log [1 + (10^{0.1 A_{max}} - 1)(f/f_b)^{2n}] \text{ dB} \quad (2)$$

where n = 6 (the order of the filter).

2.1 A LOWPASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 8* is given. Can the MF6 be used? The order of the Butterworth approximation will have to be determined using eq. 1:

A_{min} = 30 dB, A_{max} = 1.0 dB, f_s = 2 kHz, and f_b = 1 kHz

$$n = \frac{\log(10^3 - 1) - \log(10^{0.1} - 1)}{2 \log(2)} = 5.96$$

Since n can only take on integer values, n = 6. Therefore the MF6 can be used. In general, if n is 6 or less a single MF6 stage can be utilized.

Likewise, the attenuation at f_s can be found using equation 2 with the above values and n = 6 giving:

$$\text{Atten (2 kHz)} = 10 \log [1 + (10^{0.1} - 1)(2 \text{ kHz}/1 \text{ kHz})^{12}] = 30.26 \text{ dB}$$

This result also meets the design specification given in *Figure 8* again verifying that a single MF6 section will be adequate.

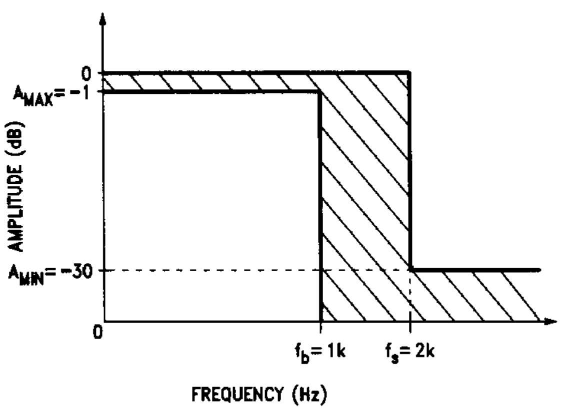

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FIGURE 8. Design Example Magnitude Response Specification Where the Response of the Filter Design Must Fall Within the Shaded Area of the Specification

Since the MF6's cutoff frequency f_c, which corresponds to a gain attenuation of −3.01 dB, was not specified in this example it needs to be calculated. Solving equation 2 where $f = f_c$ as follows:

$$f_c = f_b \left[\frac{(10^{0.1(3.01 \text{ dB})} - 1)}{(10^{0.1 A_{max}} - 1)}\right]^{1/(2n)}$$

$$= 1 \text{ kHz} \left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/12}$$

$$= 1.119 \text{ kHz}$$

where $f_c = f_{CLK}/50$ or $f_{CLK}/100$.

To implement this example for the MF6-50 the clock frequency will have to be set to f_{CLK} = 50(1.116 kHz) = 55.8 kHz or for the MF6-100 f_{CLK} = 100(1.116 kHz) = 111.6 kHz.

2.2 CASCADING MF6s

In the case where a steeper stopband attenuation rate is required two MF6's can be cascaded (*Figure 9*) yielding a 12th order slope of 72 dB per octave. Because the MF6 is a Butterworth filter and therefore has no ripple in its passband, when MF6s are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 10*.

In determining whether the cascaded MF6s will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

$$n = \frac{\log(10^{0.05 A_{min}} - 1) - \log(10^{0.05 A_{max}} - 1)}{2 \log(f_s/f_b)} \quad (3)$$

$$Attn(f) = 10 \log [1 + (10^{0.05 A_{max}} - 1)(f/f_b)^{2n}] \text{ dB} \quad (4)$$

where n = 6 (the order of each filter).

Equation 3 will determine whether the order of the filter is adequate ($n \leq 6$) while equation 4 can determine if the required stopband attenuation is met and what actual cutoff frequency (f_c) is required to obtain the particular frequency response desired. The design procedure would be identical to the one shown in section 2.1.

2.3 IMPLEMENTING A "NOTCH" FILTER WITH THE MF6

A "notch" filter with 60 dB of attenuation can be obtained by using one of the Op-Amps, available in the MF6, and three external resistors. The circuit and amplitude response are shown in *Figure 11*.

The frequency where the "notch" will occur is equal to the frequency at which the output signal of the MF6 will have the same magnitude but be 180 degrees out of phase with its input signal. For a sixth order Butterworth filter 180° phase shift occurs where $f = f_n = 0.742 f_c$. The attenuation at this frequency is 0.12 dB which must be compensated for by making $R_1 = 1.014 \times R_2$.

Since R_1 does not equal R_2 there will be a gain inequality above and below the notch frequency. At frequencies below the notch frequency ($f << f_n$), the signal through the filter has a gain of one and is non-inverting. Summing this with the input signal through the Op-Amp yields an overall gain of two or +6 dB. For $f >> f_n$, the signal at the output of the filter is greatly attenuated thus only the input signal will appear at the output of the Op-Amp. With $R_3 = R_1 = 1.014\ R_2$ the overall gain is 0.986 or −0.12 dB at frequencies above the notch.

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Designing with the MF6 (Continued)

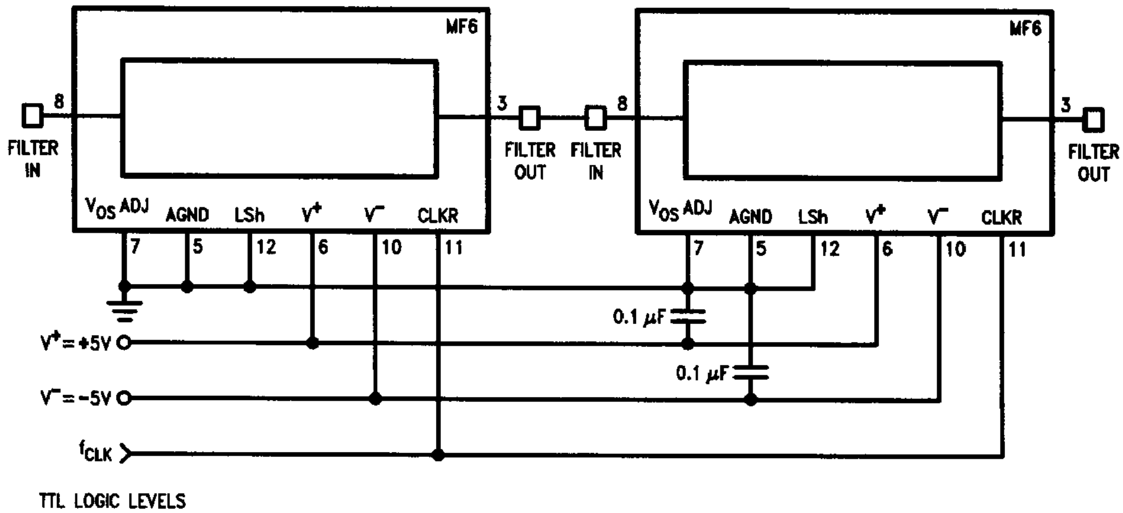

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FIGURE 9. Cascading Two MF6s

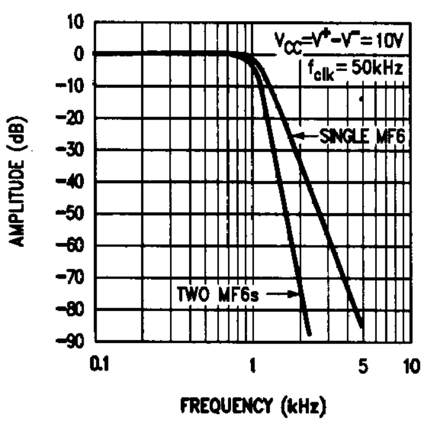

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FIGURE 10a. One MF6-50 vs. Two MF6-50s Cascaded

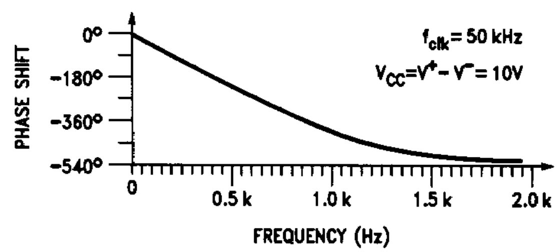

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FIGURE 10b. Phase Response of Two Cascaded MF6-50s

Designing with the MF6 (Continued)

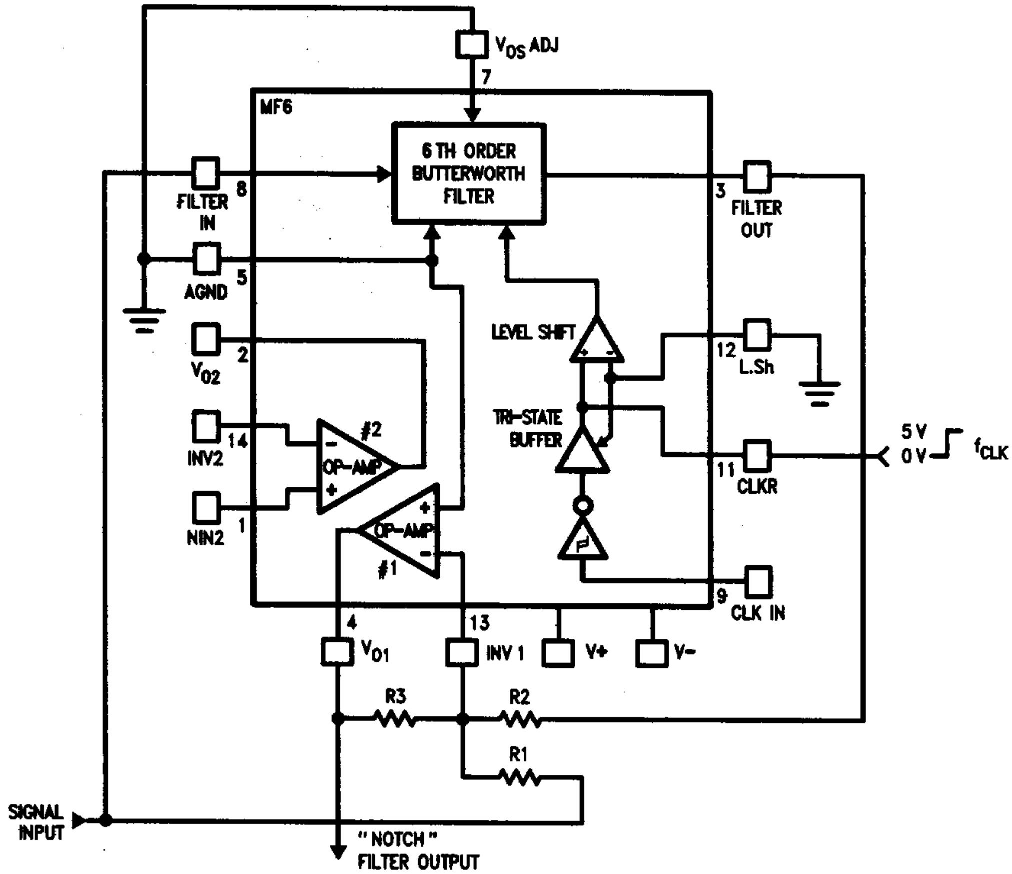

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FIGURE 11a. "Notch" Filter

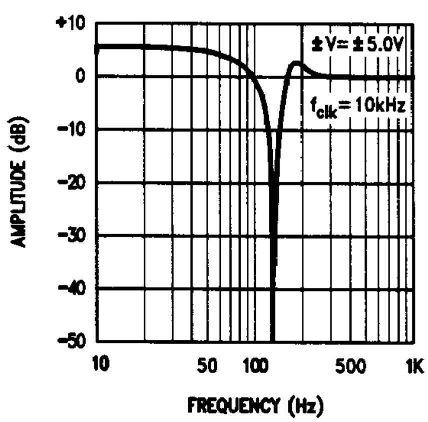

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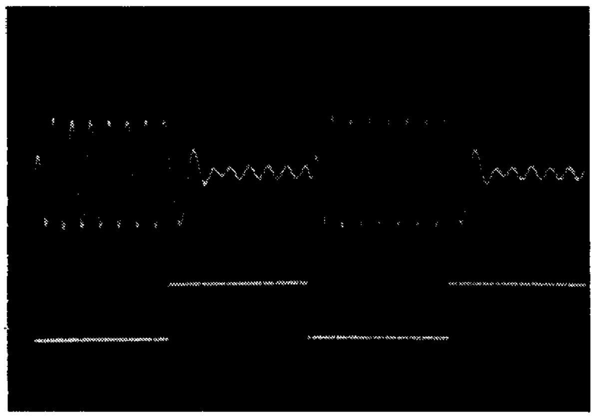
FIGURE 11b. MF6-50 "Notch" Filter Amplitude Response

Designing with the MF6 (Continued)

2.4 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The MF6 will respond favorably to a sudden change in clock frequency. Distortion in the output signal occurs at the transition of the clock frequency and lasts approximately three cutoff frequency (f_c) cycles. As shown in *Figure 12*, if the control signal is low the MF6-50 has a 100 kHz clock making f_c = 2 kHz; when this signal goes high the clock frequency changes to 50 kHz yielding 1 kHz f_c.

The transient response of the MF6 seen in *Figure 13* is also dependent on the f_c and thus the f_{CLK} applied to the filter. The MF6 responds as a classical sixth order Butterworth lowpass filter.



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f_{IN} = 1.5 kHz (scope time base = 2 ms/div)

FIGURE 12. MF6-50 Abrupt Clock Frequency Change

2.5 ALIASING CONSIDERATIONS

Aliasing effects have to be taken into consideration when input signal frequencies exceed half the sampling rate. For the MF6 this equals half the clock frequency (f_{CLK}). When

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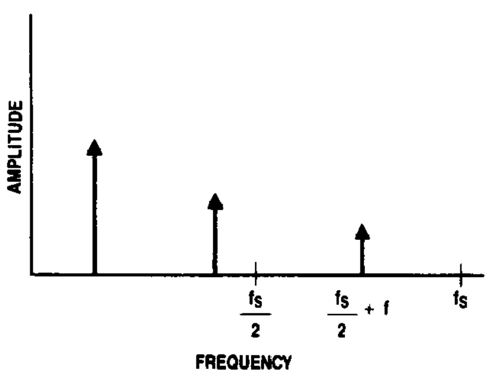
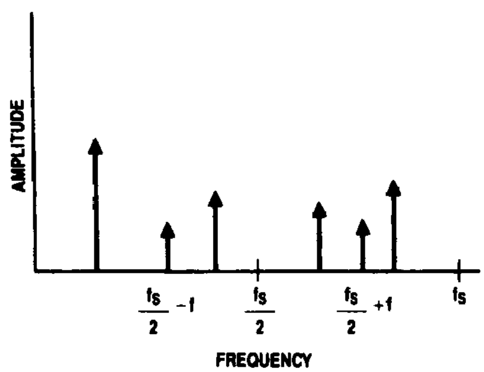
FIGURE 13. MF6-50 Step Input Response, Vertical = 2V/div., Horizontal = 1 ms/div., f_{CLK} = 100 kHz

the input signal contains a component at a frequency higher than half the clock frequency, as in *Figure 14a*, that component will be "reflected" about $f_{CLK}/2$ into the frequency range *below* $f_{CLK}/2$ as in *Figure 14b*. If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore if frequency components in the input signal exceed $f_{CLK}/2$ they must be attenuated before being applied to the MF6 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level. An example circuit is shown in *Figure 15* using one of the uncommitted Op-Amps available in the MF6.



TL/H/5065-37

(a) Input Signal Spectrum

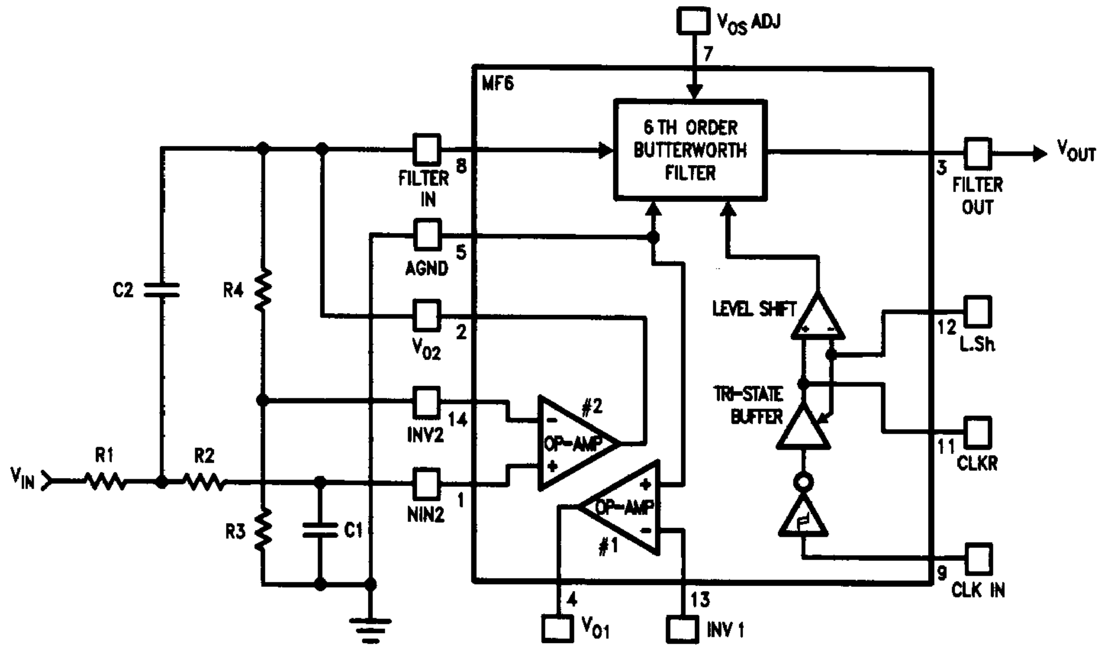


TL/H/5065-38

(b) Output Signal Spectrum. Note that the input signal at $f_s/2 + f$ causes an output signal to appear at $f_s/2 - f$.

Figure 14. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the MF6, $f_s = f_{CLK}$.

Designing with the MF6 (Continued)



TL/H/5065-34

$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$

$H_0 = R_4/R_3$ ($H_0 = 1$ when R_3 and R_4 are omitted and V_{O2} is directly tied to INV2).

Design Procedure:

pick C_1

$R_2 = \frac{1}{2QC_1\omega_0}$

for a 2nd Order Butterworth Q = 0.707

$R_2 = \frac{0.113}{C_1f_0}$

make $R_1 = R_2$

and

$C_2 = \frac{1}{(2\pi f_0R_1)^2C_1}$

Note: The parallel combination of R_4 (if used), R_1 and R_2 should be ≥ 10 kΩ in order not to load Op-Amp #2.

FIGURE 15. Second Order Butterworth Anti-Aliasing Filter Using Uncommitted Op-Amp #2

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