

High Frequency Power Supply Controller

GENERAL DESCRIPTION

The ML4823 High Frequency PWM Controller is an IC controller optimized for use in Switch Mode Power Supply designs running at frequencies to 1MHz. Propagation delays are minimal through the comparators and logic for reliable high frequency operation while slew rate and bandwidth are maximized on the error amplifier. This controller is designed for single-ended applications using voltage or current mode and provides for input voltage feed forward.

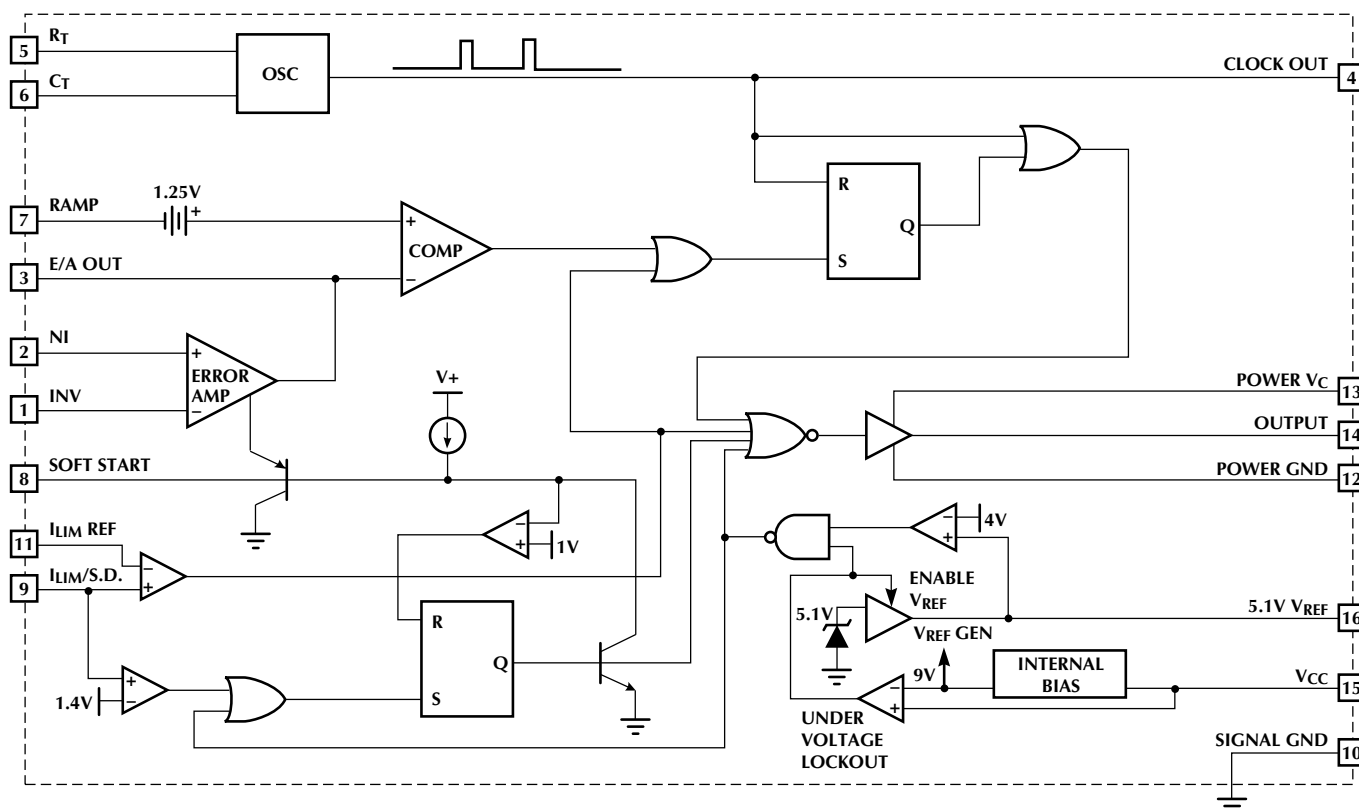
A 1V threshold current limit comparator provides cycle-by-cycle current limit and exceeding a 1.4V threshold initiates a soft-start cycle. The soft start pin doubles as a maximum duty cycle clamp. All logic is fully latched to provide jitter-free operation and prevent multiple pulsing. An under-voltage lockout circuit with 800mV of hysteresis assures low startup current and drives the outputs low during fault conditions.

This controller is an improved second source for the UC3823 controller; however, the ML4823 includes features not found on the 3823. These features are set in italics.

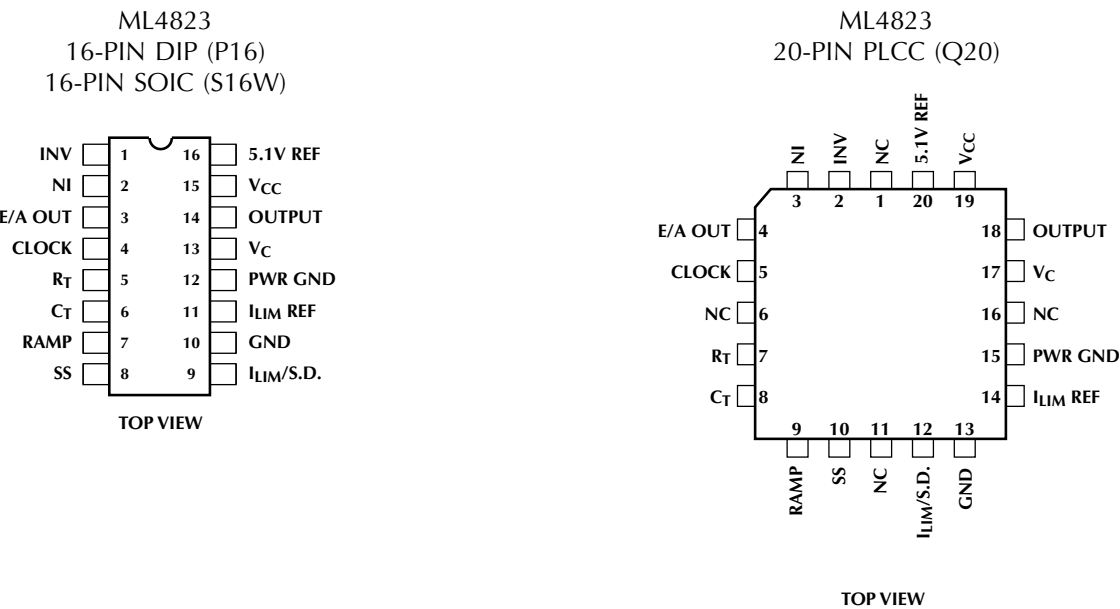
FEATURES

- Practical operation at switching frequencies to 1.0MHz
- High current (2A peak) totem pole output
- Wide bandwidth error amplifier
- Fully latched logic with double pulse suppression
- Pulse-by-pulse current limiting
- Soft start and max. duty cycle control
- Under voltage lockout with hysteresis
- 5.1V trimmed bandgap reference
- Low start-up current (1.1mA)
- Pin compatible improved replacement for UC3823
- Fast shut down path from current limit to output
- Soft start latch ensures full soft start cycle
- Outputs pull low for undervoltage lockout

BLOCK DIAGRAM (Pin Configuration Shown for 16-Pin Version)



PIN CONFIGURATION



PIN DESCRIPTION (Pin Numbers in Parentheses are for PLCC Version)

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1 (2)	INV	Inverting input to error amp.	9 (12)	ILIM/S.D.	Current limit sense pin. Normally connected to current sense resistor.
2 (3)	NI	Non-inverting input to error amp.	10 (13)	GND	Analog signal ground.
3 (4)	E/A OUT	Output of error amplifier and input to main comparator.	11 (14)	ILIM REF	Reference input for cycle-by-cycle current limit comparator.
4 (5)	CLOCK	Oscillator output.	12 (15)	PWR GND	Return for the high current totem pole output.
5 (7)	RT	Timing resistor for oscillator — sets charging current for oscillator timing capacitor (pin 6).	13 (17)	VC	Positive supply for the high current totem pole output.
6 (8)	CT	Timing capacitor for oscillator.	14 (18)	OUT B	High current totem pole output.
7 (9)	RAMP	Non-inverting input to main comparator. Connected to CT for Voltage mode operation or to current sense resistor for current mode.	15 (19)	VCC	Positive supply for the IC.
8 (10)	SS	Normally connected to soft start capacitor.	16 (20)	5.1V REF	Buffered output for the 5.1V voltage reference.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_C , V_{CC})	30V
OUTPUT Current, Source or Sink	
DC	0.5A
Pulse (0.5 μ s)	2.0A
Analog Inputs	
(INV, NI, RAMP, SS, I_{LIM})	GND –0.3V to 6V
CLOCK OUTPUT Current	–5mA
F/A OUT Current	5mA
SOFT START Sink Current	20mA
R_T Charging Current	–5mA

Junction Temperature	125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering 10 sec.)	260°C
Thermal Resistance (θ_{JA})	
Plastic DIP	80°C/W
Plastic SOIC	105°C/W
Plastic Chip Carrier (PLCC)	78°C/W

OPERATING CONDITIONS

Temperature Range	
ML4823C	0°C to 70°C
ML4823I	–40°C to 85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $R_T = 3.65k\Omega$, $C_T = 1000pF$, T_A = Operating Temperature Range, $V_{CC} = 15V$. (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Initial Accuracy	$T_J = 25^\circ C$,	360	400	440	kHz
Voltage Stability	$10V \leq V_{CC} \leq 30V$,		0.2	2	%
Temperature Stability			5		%
Total Variation	Line, temp.	340		460	kHz
Clock Out High		3.9	4.5		V
Clock Out Low			2.3	2.9	V
Ramp Peak		2.6	2.8	3.0	V
Ramp Valley		0.7	1.0	1.25	V
Ramp Valley to Peak		1.6	1.8	2.0	V
REFERENCE					
Output Voltage	$T_J = 25^\circ C$, $I_O = 1mA$	5.025	5.10	5.175	V
Line Regulation	$10V \leq V_{CC} \leq 30V$		2	20	mV
Load Regulation	$1mA \leq I_O \leq 10mA$		5	20	mV
Temperature Stability	$-40^\circ C \leq T_J \leq 150^\circ C$,		0.2	0.4	%
Total Variation	Line, load, temp.	4.975		5.225	V
Output Noise Voltage	10Hz to 10kHz		50		μV
Long Term Stability	$T_J = 125^\circ C$, 1000 hrs,		5	25	mV
Short Circuit Current	$V_{REF} = 0V$	–15	–50	–100	mA
ERROR AMPLIFIER					
Input Offset Voltage				± 30	mV
Input Bias Current			0.6	3	μA
Input Offset Current			0.1	1	μA
Open Loop Gain	$1 \leq V_O \leq 4V$	50	95		dB

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER (Continued)					
CMRR	$1.5 \leq V_{CC} \leq 5.5V$	50	80		dB
PSRR	$10 \leq V_{CC} \leq 30V$	70	100		dB
Output Sink Current	$V_{E/A\ OUT} = 1V$	1	2.5		mA
Output Source Current	$V_{E/A\ OUT} = 4V$	-0.5	-1.3		mA
Output High Voltage	$I_{E/A\ OUT} = -0.5mA$	4.0	4.7	5.0	V
Output Low Voltage	$I_{E/A\ OUT} = 1mA$	0	0.5	1.0	V
Unity Gain Bandwidth		3	5.5		MHz
Slew Rate		6	12		V/ μs
PWM COMPARATOR					
RAMP Bias Current	$V_{RAMP} = 0V$		-1	-5	μA
Duty Cycle Range		0		80	%
E/A OUT Zero DC Threshold	$V_{RAMP} = 0V$	1.1	1.25		V
Delay to Output			50	80	ns
SOFT START					
Charge Current	$V_{SOFT\ START} = 0.5V$	3	9	20	μA
Discharge Current	$V_{SOFT\ START} = 1V$	1			mA
CURRENT LIMIT/SHUTDOWN					
I_{LIM} Bias Current	$0V \leq I_{LIM} \leq 4V$			± 10	μA
Current Limit Offset	$I_{LIM\ REF} = 1.1V$	0		15	mV
$I_{LIM\ REF}$ Common Mode Range		1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	V
Delay to Output			50	80	ns
OUTPUT					
Output Low Level	$I_{OUT} = 20mA$		0.25	0.40	V
	$I_{OUT} = 200mA$		1.2	2.2	V
Output High Level	$I_{OUT} = -20mA$	12.8	13.5		V
	$I_{OUT} = -200mA$	12.0	13.0		V
Collector Leakage	$V_C = 30V$		100	500	μA
Rise/Fall Time	$C_L = 1000pF$		30	60	ns
UNDER VOLTAGE LOCKOUT					
Start Threshold		8.8	9.2	9.7	V
UVLO Hysteresis		0.4	0.8	1.2	V
SUPPLY					
Start Up Current	$V_{CC} = 8V$		1.1	2.5	mA
I_{CC}	INV, RANP, $I_{LIM} = 0V$ $NI = 1V$		22	33	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4823 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $3/R_{SET}$. When the capacitor voltage reaches the upper threshold (Ramp Peak), the comparator changes state and the capacitor discharges to the lower threshold (Ramp Valley) through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where: $T_{RAMP} = C (Ramp\ Valley\ to\ Peak)/I_{SET}$

and: $T_{DEADTIME} = C (Ramp\ Valley\ to\ Peak)/I_{Q1}$

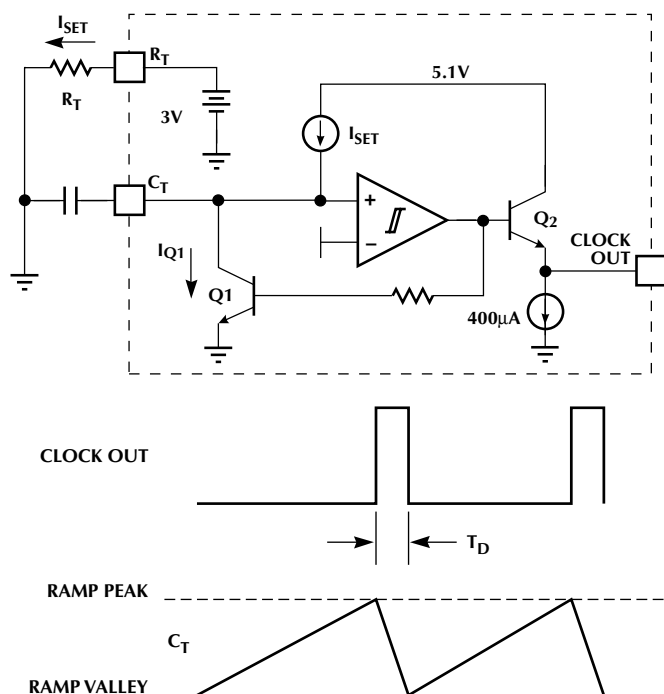


Figure 1. Oscillator Block Diagram

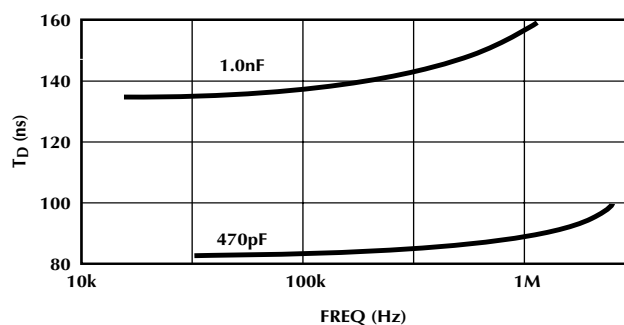


Figure 3. Oscillator Deadtime vs Frequency

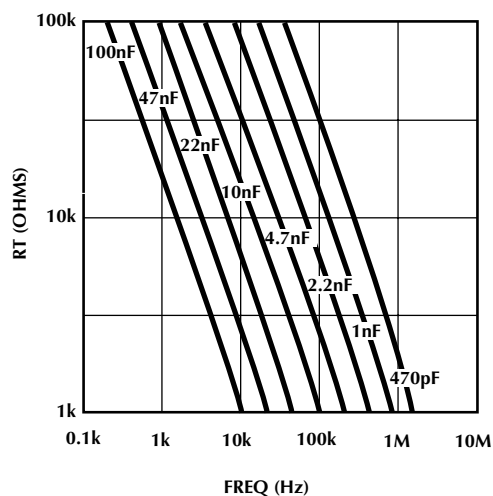


Figure 2. Oscillator Timing Resistance vs Frequency

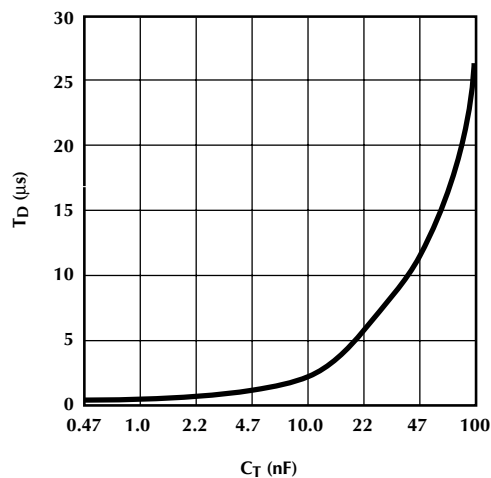


Figure 4. Oscillator Deadtime vs C_T ($3k\Omega - R_T - 100k\Omega$)

ERROR AMPLIFIER

The ML4823 error amplifier is a 5.5MHz bandwidth 12V/ μ s slew rate op-amp with provision for limiting the positive output voltage swing (Output Inhibit line) for ease in implementing the soft start function.

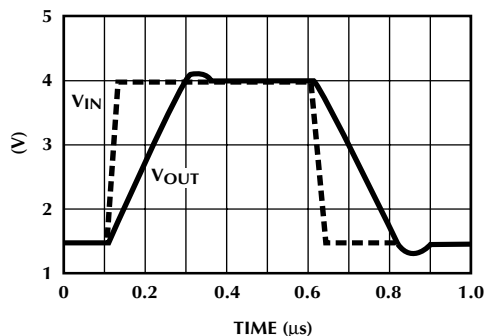


Figure 5. Unity Gain Slew Rate

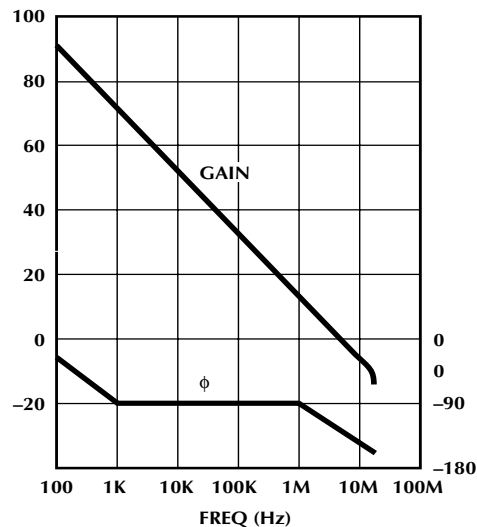


Figure 6. Open Loop Frequency Response

OUTPUT DRIVER STAGE

The ML4823 Output Driver is a 2A peak output high speed totem pole circuit designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors.

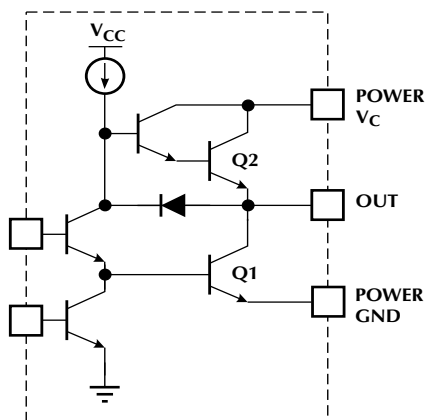


Figure 7. Simplified Schematic

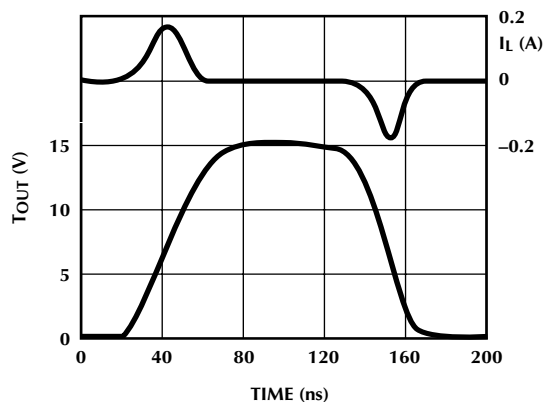


Figure 9. Rise/Fall Time ($C_L = 1000\text{pF}$)

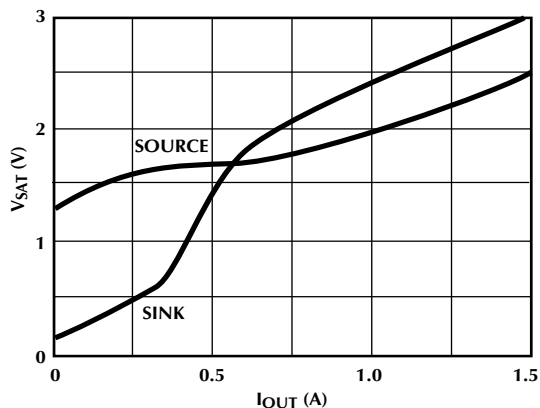


Figure 8. Saturation Curves

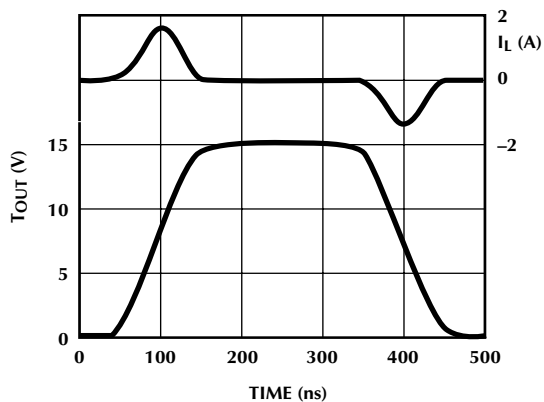


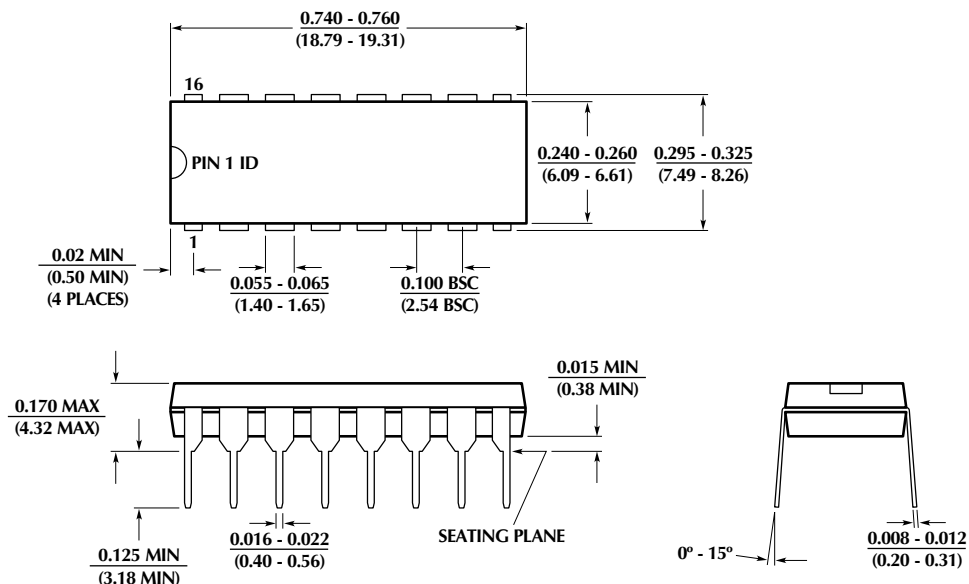
Figure 10 Rise/Fall Time ($C_L = 10,000\text{pF}$)

SOFT START AND CURRENT LIMIT

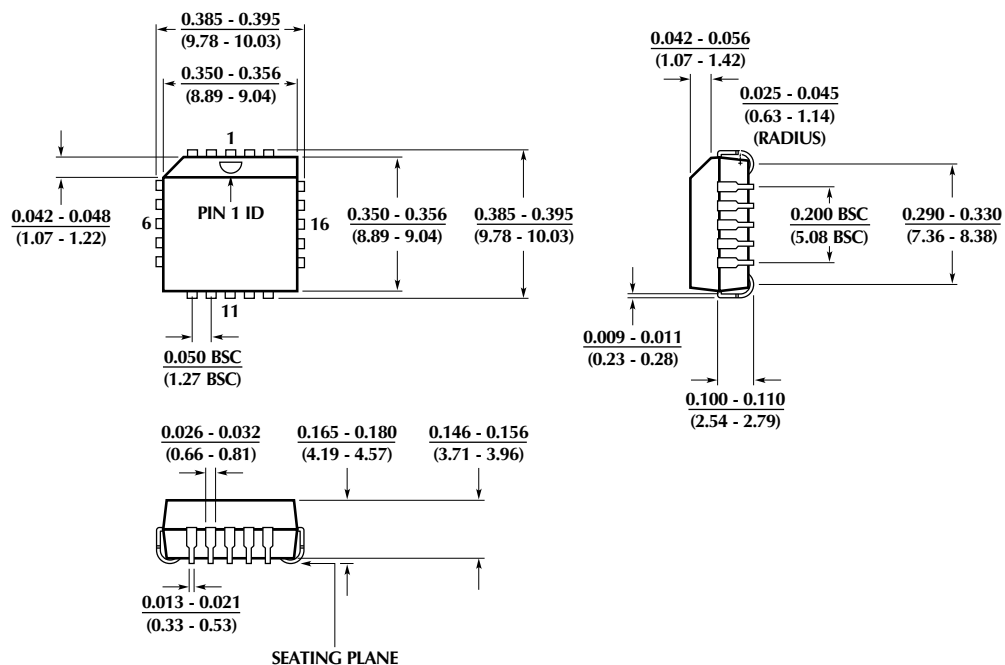
The ML4823 employs two current limits. When the voltage at I_{LIM}/SD exceeds the $I_{LIM} REF$ threshold on $I_{LIM} REF$, the outputs are immediately shut off and the cycle is terminated for the remainder of the oscillator period by resetting the RS flip flop.

If the output current is rising quickly (usually due to transformer saturation) such that the voltage on pin 9 reaches 1.4V before the outputs have turned off, a soft start cycle is initiated. The soft start capacitor is discharged and outputs are held "off" until the voltage at SS reaches 1V, ensuring a complete soft start cycle. The duty cycle on start up is limited by limiting the output voltage of the error amplifier voltage to the voltage at the SS pin.

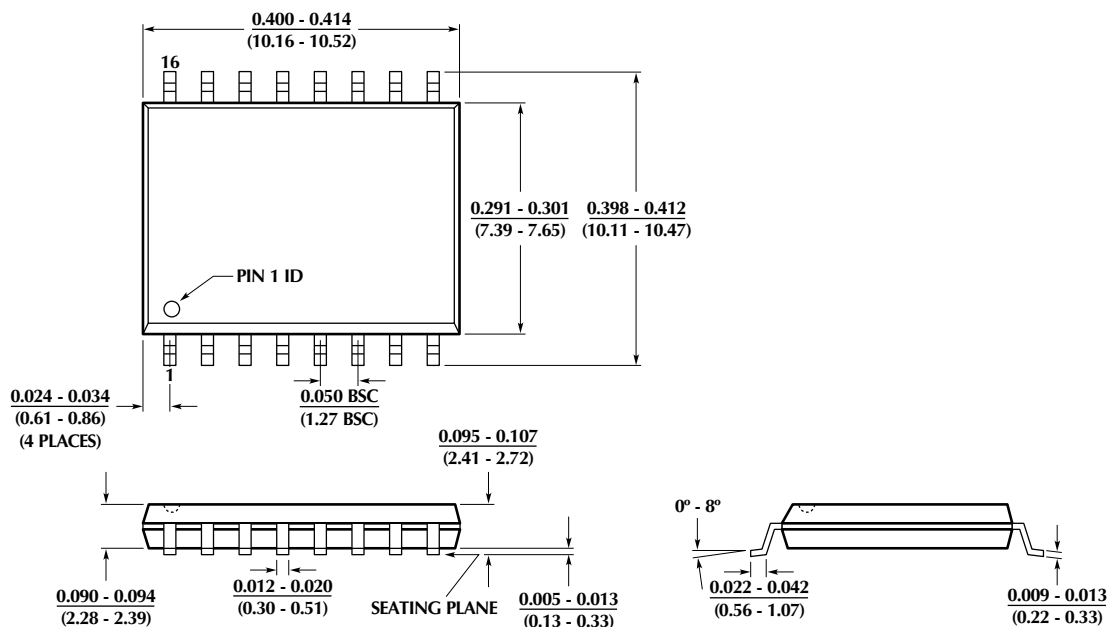
Package: P16
16-Pin PDIP



Package: Q20
20-Pin PLCC



PHYSICAL DIMENSIONS inches (millimeters)

Package: S16W
16-Pin Wide SOIC

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4823CP	0°C to 70°C	16-Pin PDIP (P16)
ML4823CQ	0°C to 70°C	20-Pin PLCC (Q20)
ML4823CS	0°C to 70°C	20-Pin Wide SOIC (S16W)
ML4823IQ	-40°C to 85°C	16-Pin PDIP (P16)
ML4823IS	-40°C to 85°C	20-Pin PLCC (Q20)
ML4823MJ	-40°C to 85°C	16-Pin Wide SOIC (S16W)

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