



Description

The MK74CB44 Buffalo™ is a monolithic CMOS high speed clock driver. It consists of four identical single input to four low-skew output, non-inverting clock drivers. When combined with ICS's MK series of low jitter clock synthesizers, the chips form an unequaled high performance clocking scheme. This monolithic solution can eliminate concern for part-to-part skew matching. The MK74CB44 is packaged in the tiny 28 pin SSOP, which uses the same board space as the narrow 16 pin SOIC.

Features

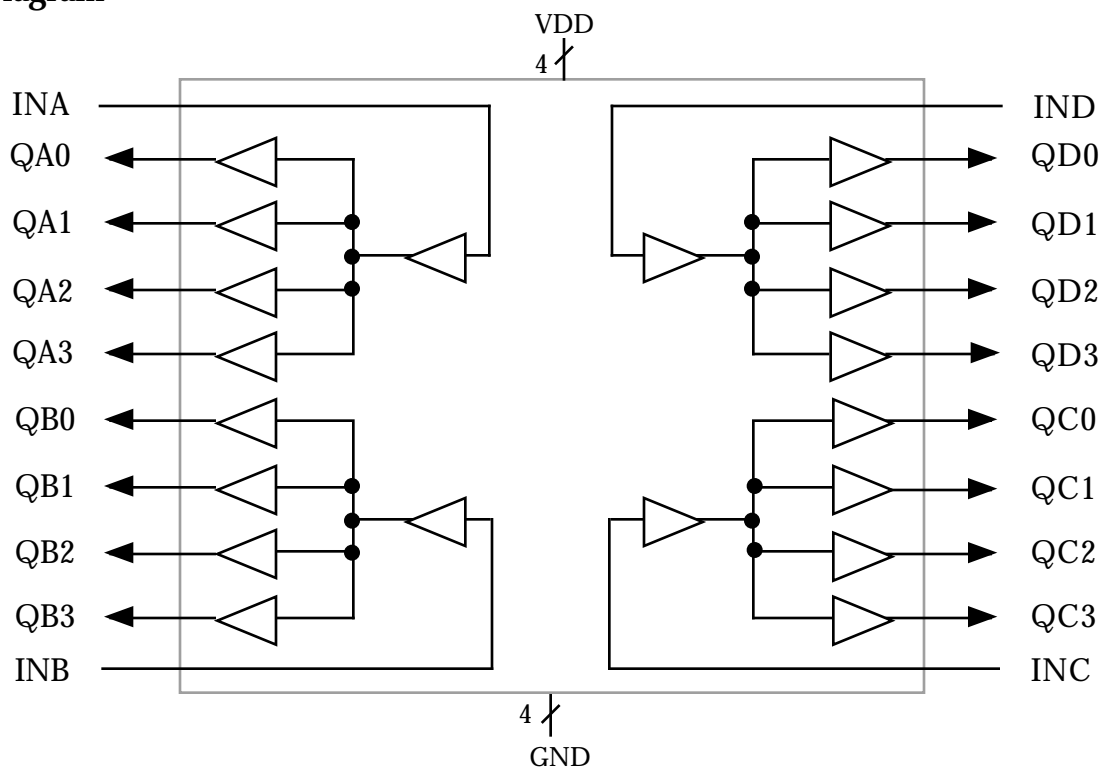


- Tiny 28 pin SSOP (150 mil) package
- Quad one input to four output clock drivers
- Outputs are skew matched to within 250ps
- A, B, C and D banks matched to 250ps
- 3.3V±10% and/or 5V±10% supply voltage
- Clock speeds up to 200 MHz
- For tighter skew matching, more outputs, or other speeds, consult ICS for other solutions

Family of ICS Parts

The MK74CB44 Buffalo™ is designed to be used with ICS's clock synthesizer devices. The inputs of the Buffalo are matched to the outputs of ICS clock synthesizers. Consult ICS for applications support.

Block Diagram

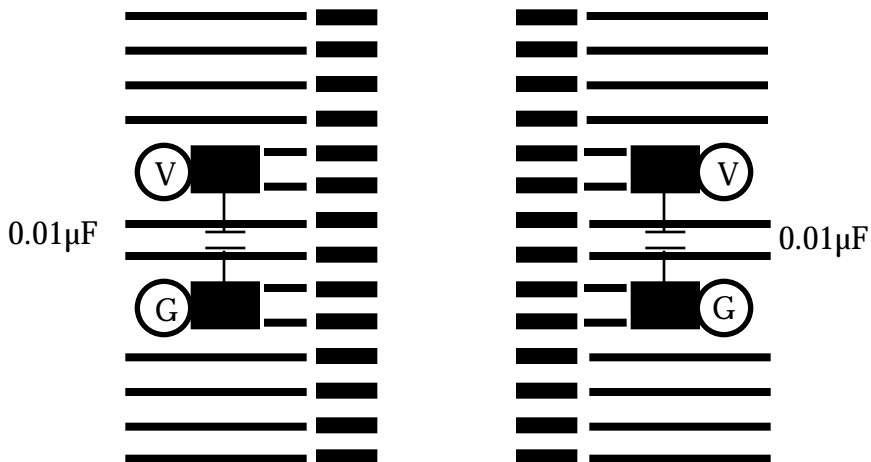




Pin Assignment

INA	1	28	IND
QA0	2	27	QD0
QA1	3	26	QD1
QA2	4	25	QD2
VDD	5	24	VDD
VDD	6	23	VDD
QA3	7	22	QD3
QB0	8	21	QC0
GND	9	20	GND
GND	10	19	GND
QB1	11	18	QC1
QB2	12	17	QC2
QB3	13	16	QC3
INB	14	15	INC

Suggested Layout



For simplicity, series terminating resistors (required) are not shown for the outputs, but should be placed as close to the device as possible. It is most critical to have the 0.01µF decoupling capacitors closest.

(V) = connect to VDD (G) = connect to GND

Pin Descriptions

Number	Name	Type	Description
1	INA	I	Clock input for four A outputs.
2, 3, 4	QA0, QA1, QA2	O	Clock A outputs.
5, 6	VDD	P	Power supply. Connect to +3.3 V or +5 V. Must be the same as pins 23, 24.
7	QA3	O	Clock A output.
8	QB0	O	Clock B output.
9, 10	GND	P	Connect to ground.
11, 12, 13	QB1, QB2, QB3	O	Clock B outputs.
14	INB	I	Clock input for four B outputs.
15	INC	I	Clock input for four C outputs.
16, 17, 18	QC3, QC2, QC1	O	Clock C outputs.
19, 20	GND	P	Connect to ground.
21	QC0	O	Clock C output.
22	QD3	O	Clock D output.
23, 24	VDD	P	Power supply. Connect to +3.3 V or +5 V. Must be the same as pins 5, 6.
25, 26, 27	QD2, QD1, QD0	O	Clock D outputs.
28	IND	I	Clock input for four D outputs.

Type: I = Input, O = output, P = power supply connection

**Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 20 seconds			260	°C
Storage Temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3.0	3.3	5.5	V
Input High Voltage, VIH		VDD-1	VDD/2		V
Input Low Voltage, VIL			VDD/2	1	V
Output High Voltage	IOH=-8mA	VDD-0.4			V
Output High Voltage	IOH=-12mA	2.4			V
Output Low Voltage	IOL=12mA			0.8	V
Operating Supply Current, IDD, at 100 MHz	No Load		55		mA
Output Impedance			14		
Short Circuit Current	Each output		50		mA
Input Capacitance			7		pF
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Clock Frequency	Note 4, 5	0		200	MHz
Propagation Delay with load=15pF			1.4	3	ns
Output Clock Rise Time	0.8 to 2.0V			2	ns
Output Clock Fall Time	2.0 to 0.8V			2	ns
Output Clock Rising Edge Skew	At VDD/2. Note 2		100	250	ps
Output Clock Bank to Bank Skew	At VDD/2. Note 3		100	250	ps

Notes:

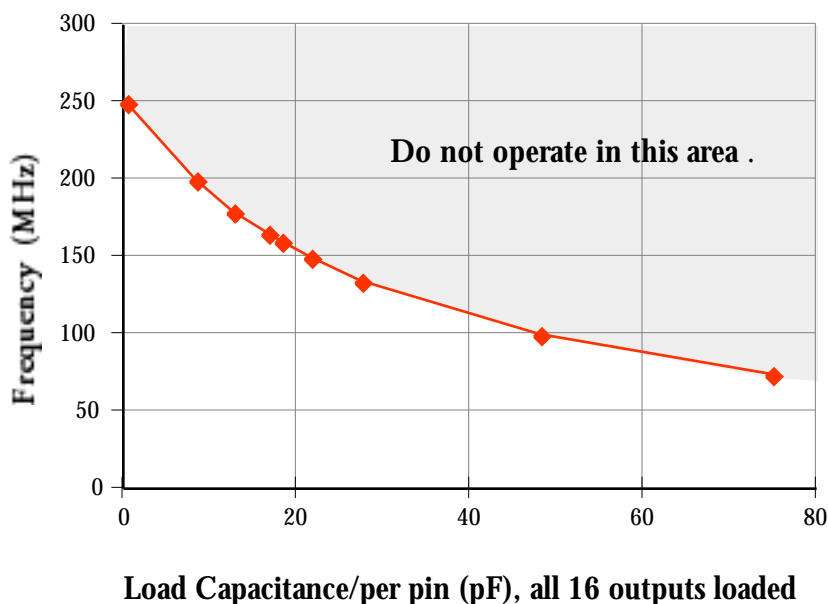
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Within any bank of four outputs, with equal loading.
3. Between any two banks of four with their inputs connected together, and equal loading.
4. At VDD = 3.3 V, 70°C, series termination of 33 Ω per pin, 8 pF load per pin.
5. See discussion and graph of speed versus load.



Maximum Speed/Application Notes

The maximum speed at which the chip can operate is limited by power dissipation of the package. Graph 1 shows the operating frequency plotted against load capacitance per pin for a die temperature of 125°C. This is at VDD = 3.3 V, 70°C and with 33 Ω series termination resistor. The termination resistors are essential because they allow a large proportion of the total power to be dissipated outside the package. Reducing or eliminating the series termination will cause an increase in die temperature. It is not recommended to operate the chip at die temperature greater than 125°C. Also note that the load capacitance per pin must include PC board parasitics such as trace capacitance. ICS has other buffers specified to 250 MHz with heavier loads.

If not all outputs of the chip are used, it is possible to operate the chip faster with larger loads. Unused outputs should be left unconnected. Consult ICS for your specific requirement.



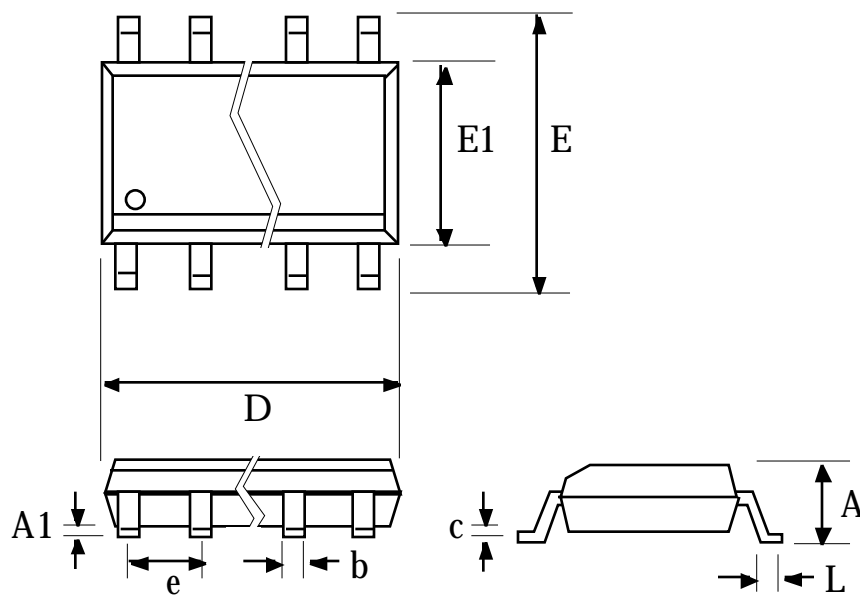
Graph 1
MK74CB44
Maximum Speed at 3.3 V



Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

28 pin SSOP



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.102	0.254
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.191	0.254
D	0.386	0.394	9.804	10.008
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
L	0.016	0.050	0.406	1.270

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK74CB44R	MK74CB44R	28 pin SSOP	0-70°C
MK74CB44RTR	MK74CB44R	Add Tape & Reel	0-70°C

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