



# MK3771-17

## VCXO and HDTV Set-Top Clock Source

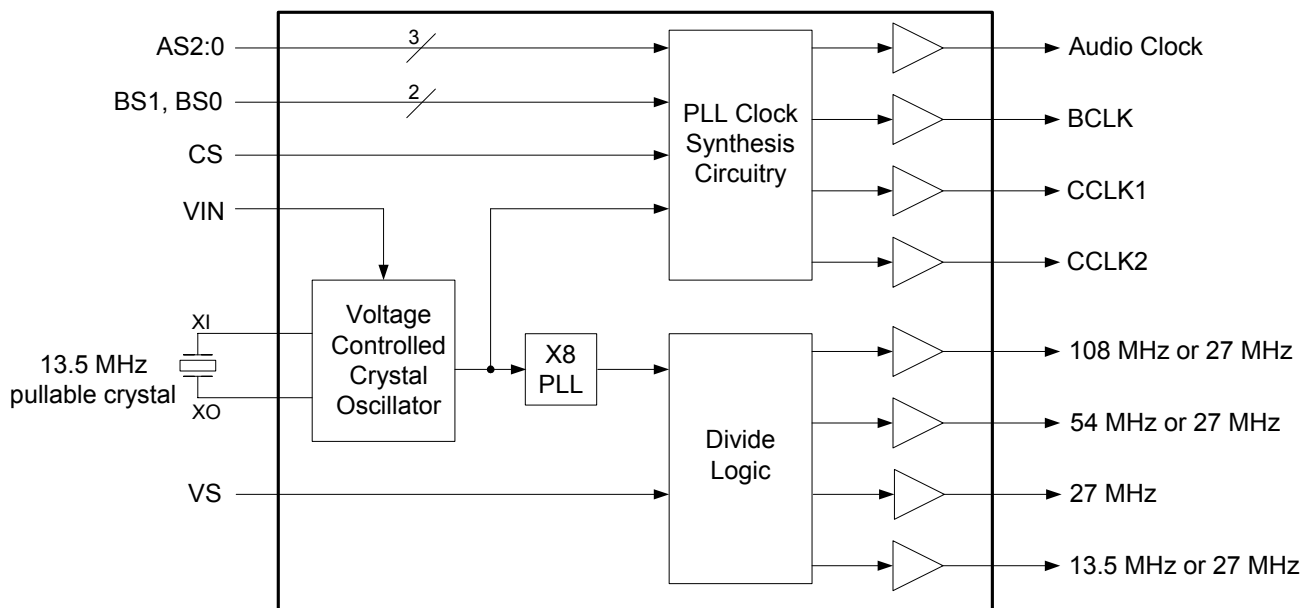
### Description

The MK3771-17 is a low cost, low jitter, high-performance VCXO and clock synthesizer designed for set-top boxes and HDTV receivers. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by  $\pm 100$  ppm. Using ICS's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 13.5 MHz crystal input to produce multiple output clocks including selectable BCLK, a selectable audio clock, two communications clocks, a 13.5 MHz clock, and three 27 MHz clocks. All clocks are frequency locked to the 27 MHz output (and to each other) with zero ppm error, so any output can be used as the VCXO output.

### Features

- Packaged in 28-pin SSOP
- Available in Pb (lead) free package
- HDTV frequencies of 74.25 and 74.175824 MHz
- On-chip patented VCXO with pull range of 200 ppm (minimum)
- VCXO tuning voltage of 0 to 3.3 V
- Supports Ethernet with 20 and 25 MHz clocks
- Modem clocks of 11.0592 and 24.576 MHz option
- Audio clocks support 32 kHz, 44.1 kHz, 48 kHz and 96 kHz sampling rates
- Zero ppm synthesis error in all clocks (all exactly track 27MHz VCXO)
- Uses an inexpensive 13.5 MHz crystal
- Full CMOS output swings with 12 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.3 V  $\pm 5\%$  operating supply

### Block Diagram





## Pin Assignment

|      |                          |    |    |                          |       |
|------|--------------------------|----|----|--------------------------|-------|
| BS0  | <input type="checkbox"/> | 1  | 28 | <input type="checkbox"/> | AS1   |
| X2   | <input type="checkbox"/> | 2  | 27 | <input type="checkbox"/> | AS0   |
| X1   | <input type="checkbox"/> | 3  | 26 | <input type="checkbox"/> | VCLK2 |
| VDD  | <input type="checkbox"/> | 4  | 25 | <input type="checkbox"/> | VCLK1 |
| VDD  | <input type="checkbox"/> | 5  | 24 | <input type="checkbox"/> | GND   |
| VIN  | <input type="checkbox"/> | 6  | 23 | <input type="checkbox"/> | VCLK4 |
| VDD  | <input type="checkbox"/> | 7  | 22 | <input type="checkbox"/> | VDD   |
| VDD  | <input type="checkbox"/> | 8  | 21 | <input type="checkbox"/> | AS2   |
| CS   | <input type="checkbox"/> | 9  | 20 | <input type="checkbox"/> | GND   |
| GND  | <input type="checkbox"/> | 10 | 19 | <input type="checkbox"/> | GND   |
| GND  | <input type="checkbox"/> | 11 | 18 | <input type="checkbox"/> | VCLK3 |
| BCLK | <input type="checkbox"/> | 12 | 17 | <input type="checkbox"/> | CCLK1 |
| VS   | <input type="checkbox"/> | 13 | 16 | <input type="checkbox"/> | BS1   |
| ACLK | <input type="checkbox"/> | 14 | 15 | <input type="checkbox"/> | CCLK2 |

## Audio Clocks (MHz)

| AS2 | AS1 | AS0 | ACLK    |
|-----|-----|-----|---------|
| 0   | 0   | 0   | 8.192   |
| 0   | 0   | 1   | 11.2896 |
| 0   | 1   | 0   | 12.288  |
| 0   | 1   | 1   | 16.9344 |
| 1   | 0   | 0   | 16.384  |
| 1   | 0   | 1   | 22.5792 |
| 1   | 1   | 0   | 18.432  |
| 1   | 1   | 1   | 24.576  |

## B and C Clocks (MHz)

| BS1 | BS0 | CS | BCLK   | CCLK1   | CCLK2  |
|-----|-----|----|--------|---------|--------|
| 0   | 0   | 0  | 74.175 | 20      | 25     |
| 0   | 0   | 1  | 74.175 | 11.0592 | 24.576 |
| 0   | 1   | 0  | 74.25  | 20      | 25     |
| 0   | 1   | 1  | 74.25  | 11.0592 | 24.576 |
| M   | 0   | 0  | 5.06   | 20      | 25     |
| M   | 0   | 1  | 5.06   | 11.0592 | 24.576 |
| M   | 1   | 0  | 10.12  | 20      | 25     |
| M   | 1   | 1  | 10.12  | 11.0592 | 24.576 |
| 1   | 0   | 0  | 48     | 20      | 25     |
| 1   | 0   | M  | 48     | 7.3728  | 24     |
| 1   | 0   | 1  | 48     | 11.0592 | 24.576 |
| 1   | 1   | 0  | 14.318 | 20      | 25     |
| 1   | 1   | M  | 14.318 | 7.3728  | 28.636 |
| 1   | 1   | 1  | 14.318 | 11.0592 | 24.576 |

## VCXO Clocks (MHz)

| VS | VCLK1 | VCLK2 | VCLK3 | VCLK4 |
|----|-------|-------|-------|-------|
| 0  | 27    | 27    | 27    | 108   |
| M  | 27    | 54    | 13.5  | 108   |
| 1  | 27    | 27    | 27    | 27    |



## Pin Descriptions

| Pin Number         | Pin Name | Pin Type | Pin Description                                                                            |
|--------------------|----------|----------|--------------------------------------------------------------------------------------------|
| 1                  | BS0      | I        | B clock select 0.                                                                          |
| 2                  | X2       | XO       | Crystal connection. Connect to a pullable 13.5 MHz crystal.                                |
| 3                  | X1       | XI       | Crystal connection. Connect to a pullable 13.5 MHz crystal.                                |
| 4, 5, 7, 8, 22     | VDD      | P        | Connect to +3.3 V.                                                                         |
| 6                  | VIN      | I        | Analog control voltage for VCXO. Pulls outputs $\pm 100$ ppm by varying from 0 to 3.3 V.   |
| 9                  | CS       | TI       | Communications Clock Select. Selects CCLK 1 and 2 per table above. Internal pull-up.       |
| 10, 11, 19, 20, 24 | GND      | P        | Connect to ground.                                                                         |
| 12                 | BCLK     | O        | B clock output. Determined by status of AS2:0 per table above.                             |
| 13                 | VS       | TI       | VCXO Clock Select. Selects frequencies on VCLK1-VCLK4 per table above.                     |
| 14                 | ACLK     | O        | Audio Clock Output. Determined by status of AS2:0 per table above.                         |
| 15                 | CCLK2    | O        | Communications Clock Output 2. Determined by status of CS per table above.                 |
| 16                 | BS1      | TI       | B Clock Select 1. Selects BCLK frequency. See table above.                                 |
| 17                 | CCLK1    | O        | Communications Clock Output 1. Determined by status of CS per table above.                 |
| 18                 | VCLK3    | O        | VCXO Clock output 3. Can be either 27 or 13.5 MHz per table above.                         |
| 21                 | AS2      | I        | Audio Clock Select pin 2. Selects Audio clock on pin 14 per table above. Internal pull-up. |
| 23                 | VCLK4    | O        | VCXO Clock output 4. Can be either 27 or 108 MHz per table above.                          |
| 25                 | VCLK1    | O        | VCXO Clock output 1. Always 27 MHz.                                                        |
| 26                 | VCLK2    | O        | VCXO Clock output 2. Can be either 27 or 54 MHz per table above.                           |
| 27                 | AS0      | I        | Audio Clock Select pin 0. Selects Audio clock on pin 14 per table above. Internal pull-up. |
| 28                 | AS1      | I        | Audio Clock Select pin 1. Selects Audio clock on pin 14 per table above. Internal pull-up. |

**KEY:**

I = Input

TI = Tri-level

O = Output

P = Power supply connection

XI, XO= Crystal connections



## External Component Selection

The MK3771-17 requires a minimum number of external components for proper operation.

### Decoupling Capacitors

Decoupling capacitors of 0.01 $\mu$ F should be connected between VDD and GND on pins 3 and 6, and on pins 13 and 14, as close to the MK3771-17 as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

When the PCB traces between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 $\Omega$  trace (a commonly used trace impedance) place a 33 $\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 $\Omega$ .

### Quartz Crystal

The MK3771-17 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters must be used, and the layout guidelines discussed in the following section must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The MK3771-17 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the MK3771-17 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3771-17. There should be no vias between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Please see application note MAN05 for recommended crystal parameters and suppliers.

## Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. Stuffing of these capacitors on the PCB is optional. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

To determine the need for and value of the crystal adjustment capacitors, you will need a PC board of your final layout, a frequency counter capable of about 1 ppm resolution and accuracy, two power supplies, and some samples of the crystals which you plan to use in production, along with measured initial accuracy for each crystal at the specified crystal load capacitance, CL.

To determine the value of the crystal capacitors:

1. Connect VDD of the MK3771-17 to 3.3 V. Connect pin 4 of the MK3771-17 to the second power supply. Adjust the voltage on pin 4 to 0V. Measure and record the frequency of the CLK output.
2. Adjust the voltage on pin 4 to 3.3 V. Measure and record the frequency of the same output.

To calculate the centering error:

$$\text{Error} = 10^6 \times \left[ \frac{(f_{3.3V} - f_{\text{target}}) + (f_{0V} - f_{\text{target}})}{f_{\text{target}}} \right] - \text{error}_{\text{xtal}}$$

Where:

$f_{\text{target}}$  = nominal crystal frequency

$\text{error}_{\text{xtal}}$  = actual initial accuracy (in ppm) of the crystal being measured

If the centering error is less than  $\pm 25$  ppm, no adjustment is needed. If the centering error is more than 25ppm negative, the PC board has excessive stray capacitance and a new PCB layout should be considered to reduce stray capacitance. (Alternately, the crystal may be re-specified to a higher load capacitance. Contact ICS for details.) If the centering error is more than 25ppm positive, add identical fixed centering capacitors from each crystal pin to ground. The value for each of these caps (in pF) is given by:

External Capacitor =

$2 \times (\text{centering error}) / (\text{trim sensitivity})$



Trim sensitivity is a parameter which can be supplied by your crystal vendor. If you do not know the value, assume it is 30 ppm/pF. After any changes, repeat the

measurement to verify that the remaining error is acceptably low (typically less than  $\pm 25$ ppm).

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3771-17. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                          | Rating              |
|-------------------------------|---------------------|
| Supply Voltage, VDD           | 7 V                 |
| All Inputs and Outputs        | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70°C          |
| Storage Temperature           | -65 to +150°C       |
| Junction Temperature          | 125°C               |
| Soldering Temperature         | 260°C               |

## Recommended Operation Conditions

| Parameter                                         | Min.  | Typ. | Max.  | Units |
|---------------------------------------------------|-------|------|-------|-------|
| Ambient Operating Temperature                     | 0     |      | +70   | °C    |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V     |



## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V  $\pm$ 5%**, Ambient Temperature 0 to +70°C

| Parameter                      | Symbol          | Conditions                             | Min.    | Typ.     | Max. | Units   |
|--------------------------------|-----------------|----------------------------------------|---------|----------|------|---------|
| Operating Voltage              | VDD             |                                        | 3.15    | 3.3      | 3.45 | V       |
| Input High Voltage             | V <sub>IH</sub> | Except TI pins                         | 2       |          |      | V       |
| Input Low Voltage              | V <sub>IL</sub> | Except TI pins                         |         |          | 0.8  | V       |
| Input High Voltage             | V <sub>IH</sub> | All TI pins                            | VDD-0.5 |          |      | V       |
| Input Low Voltage              | V <sub>IL</sub> | All TI pins                            |         |          | 0.5  | V       |
| Output High Voltage            | V <sub>OH</sub> | I <sub>OH</sub> = -12 mA               | 2.4     |          |      | V       |
| Output Low Voltage             | V <sub>OL</sub> | I <sub>OH</sub> = 12 mA                |         |          | 0.4  | V       |
| Output High Voltage            | V <sub>OH</sub> | CMOS level,<br>I <sub>OH</sub> = -8 mA | VDD-0.4 |          |      | V       |
| Operating Supply Current       | IDD             | No load, Note 1                        |         | 28       |      | mA      |
| Power Down Mode Supply Current |                 |                                        |         | 15       |      | $\mu$ A |
| Short Circuit Current          |                 | Each output                            |         | $\pm$ 50 |      | mA      |
| Input Capacitance              | C <sub>IN</sub> |                                        |         | 5        |      | pF      |
| Frequency Synthesis Error      |                 | All clocks                             |         |          | 0    | ppm     |
| VIN, VCXO Control Voltage      |                 |                                        | 0       |          | 3.3  | V       |

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V  $\pm$ 5%**, Ambient Temperature 0 to +70°C

| Parameter                           | Symbol          | Conditions                            | Min.      | Typ.      | Max. | Units |
|-------------------------------------|-----------------|---------------------------------------|-----------|-----------|------|-------|
| Input Frequency                     | F <sub>IN</sub> |                                       |           | 13.50000  |      | MHz   |
| Output Clock Rise Time              | t <sub>OR</sub> | 0.8 V to 2.0 V                        |           |           | 1.5  | ns    |
| Output Clock Fall Time              | t <sub>OF</sub> | 2.0 V to 0.8 V                        |           |           | 1.5  | ns    |
| Output Clock Duty Cycle             | t <sub>OD</sub> | At VDD/2                              | 40        |           | 60   | %     |
| Maximum Absolute Jitter, short term |                 |                                       |           | $\pm$ 250 |      | ps    |
| VCXO Gain                           |                 | VIN = VDD/2 $\pm$ 1 V                 |           | 100       |      | ppm/V |
| Crystal Pullability                 |                 | 0V $\leq$ VIN $\leq$ 3.3 V,<br>Note 2 | $\pm$ 100 |           |      | ppm   |

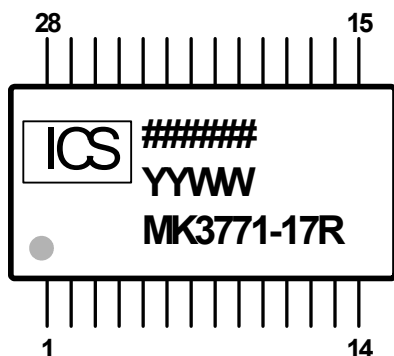
Notes: 1. With all clocks at highest MHz.  
2. With a pullable crystal that conforms to ICS' specifications.



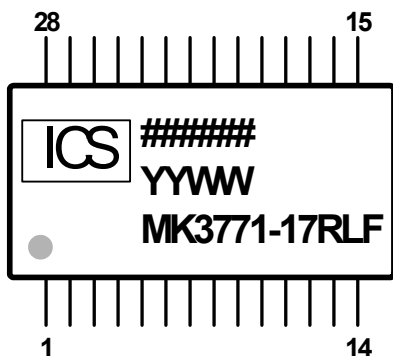
## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units |
|----------------------------------------|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 100  |      | °C/W  |
|                                        | $\theta_{JA}$ | 1 m/s air flow |      | 80   |      | °C/W  |
|                                        | $\theta_{JA}$ | 3 m/s air flow |      | 67   |      | °C/W  |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 60   |      | °C/W  |

## Marking Diagram



## Marking Diagram (Pb free)



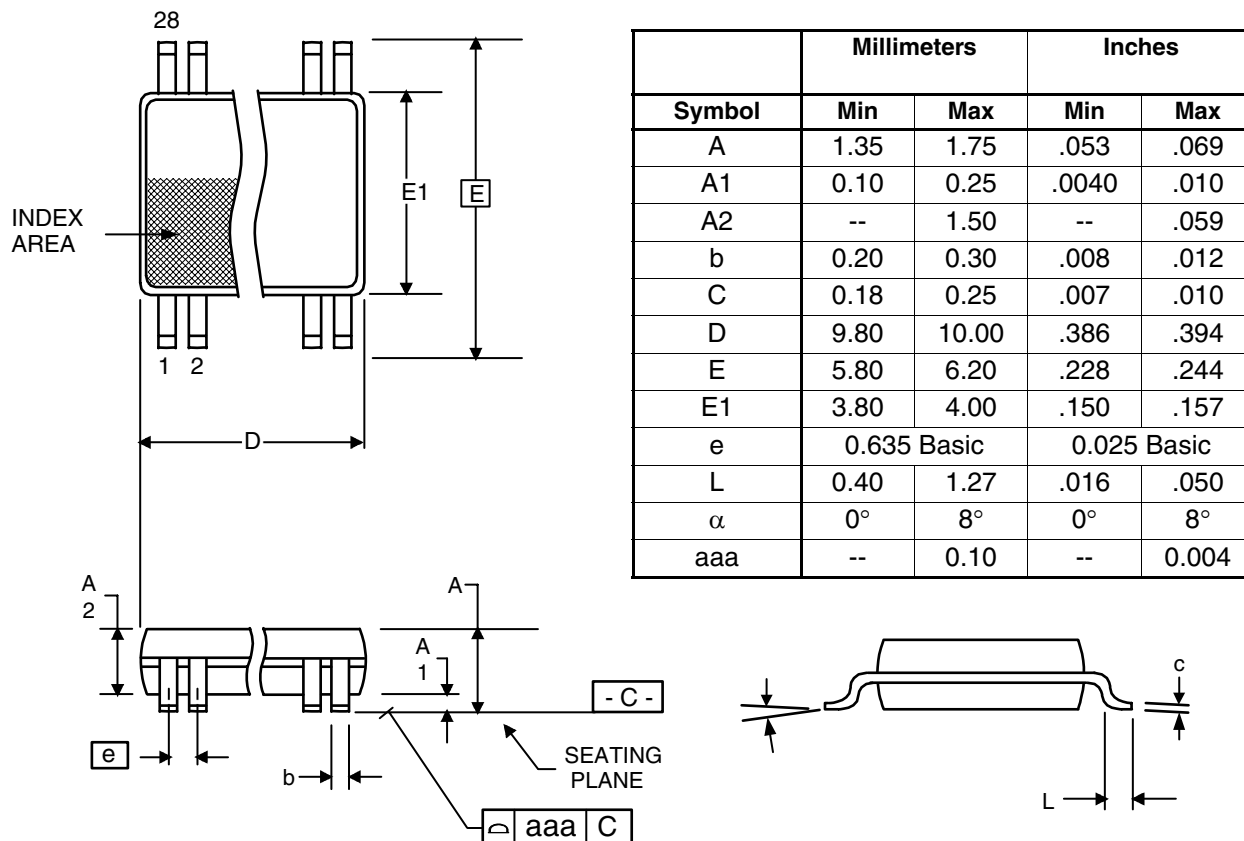
### Notes:

1. ##### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. "LF" designates Pb free packaging.



## Package Outline and Package Dimensions (28-pin SSOP, 150 mil Body, 0.025 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



## Ordering Information

| Part / Order Number | Marking      | Shipping Packaging | Package     | Temperature |
|---------------------|--------------|--------------------|-------------|-------------|
| MK3771-17R          | MK3771-17R   | Tubes              | 28-pin SSOP | 0 to +70°C  |
| MK3771-17RTR        | MK3771-17R   | Tape and Reel      | 28-pin SSOP | 0 to +70°C  |
| MK3771-17RLF        | MK3771-17RLF | Tubes              | 28-pin SSOP | 0 to +70°C  |
| MK3771-17RLFTR      | MK3771-17RLF | Tape and Reel      | 28-pin SSOP | 0 to +70°C  |

“LF” denotes Pb (lead) free package.

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