MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

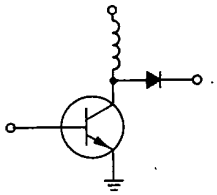
MJ13070
MJ13071

Designer's Data Sheet

SWITCHMODE II SERIES
NPN SILICON POWER TRANSISTORS

The MJ13070 and MJ13071 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 100 ns Inductive Fall Time @ 25°C (Typ)
- 150 ns Inductive Crossover Time @ 25°C (Typ)
- 400 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
- Reverse-Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

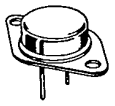
5 AMPERE

NPN SILICON POWER TRANSISTORS

400 AND 450 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



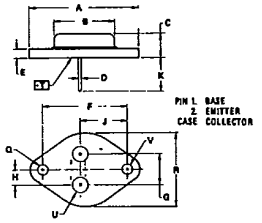
MAXIMUM RATINGS

Rating	Symbol	MJ13070	MJ13071	Unit
Collector-Emitter Voltage	V_{CEO}	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	750	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 8 0		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.0 4.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	125 71.5 0.714		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



NOTES
1. DIMENSIONS Q AND V ARE DATUMS.
2. T IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q.

⌖	Ø.13 (0.005) M	T	V M	

FOR LEADS

⌖	Ø.13 (0.005) M	T	V M	Q M

4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	8.15	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.97 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.95 BSC		0.665 BSC	
K	11.17	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.150	0.165

CASE 1-05
TO-204AA

MJ13070, MJ13071

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ13070 MJ13071	$V_{CEO(sus)}$	400 450	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	— —	0 5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 5.0 Vdc		h_{FE}	8.0	—	—	—
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	1.0 3 0 2 0	Vdc
Base-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)		$V_{BE(sat)}$	— —	— —	1 5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	—	250	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Adc, I_C = 3.0 Adc, I_{B1} = 0 4 Adc, t_p = 30 μs, Duty Cycle ≤2%, $V_{BE(off)}$ = 5.0 Vdc)	t_d	—	0.03	0.05	μs
Rise Time		t_r	—	0 10	0.40	
Storage Time		t_s	—	0.40	1 50	
Fall Time		t_f	—	0.175	0 50	
Inductive Load, Clamped (Table 1)						
Storage Time	($I_{C(pk)}$ = 3.0 A, I_{B1} = 0 4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 250 V) (T_J = 100°C)	t_{sv}	—	0 70	2 0	μs
Crossover Time		t_c	—	0.28	0 50	
Fall Time		t_{fi}	—	0.15	0 30	
Storage Time	(T_J = 25°C)	t_{sv}	—	0.40	—	
Crossover Time		t_c	—	0 15	—	
Fall Time		t_{fi}	—	0 10	—	

(1) Pulse Test PW - 300 μs, Duty Cycle ≤2%

$\beta_f = \frac{I_C}{I_B}$

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — DC CURRENT GAIN

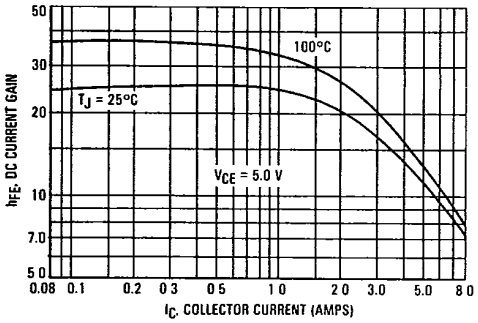


FIGURE 2 — COLLECTOR SATURATION REGION

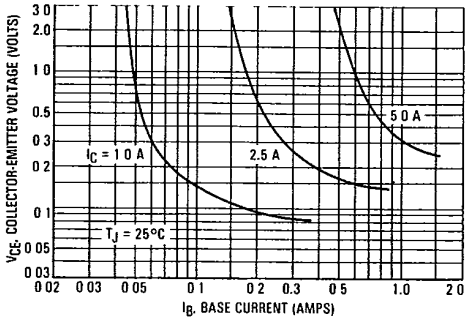


FIGURE 3 — COLLECTOR-EMITTER SATURATION VOLTAGE

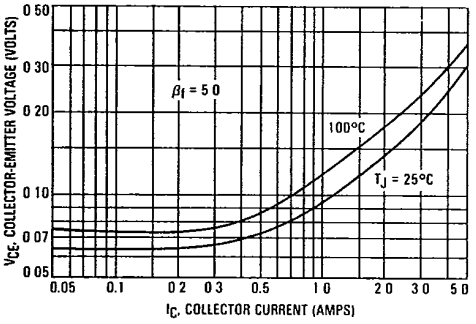


FIGURE 4 — BASE-EMITTER VOLTAGE

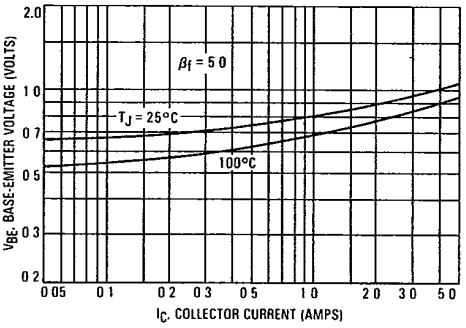


FIGURE 5 — COLLECTOR CUTOFF REGION

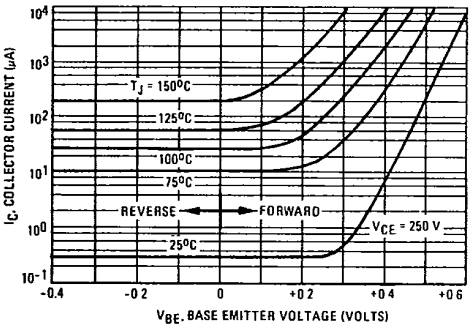


FIGURE 6 — CAPACITANCE

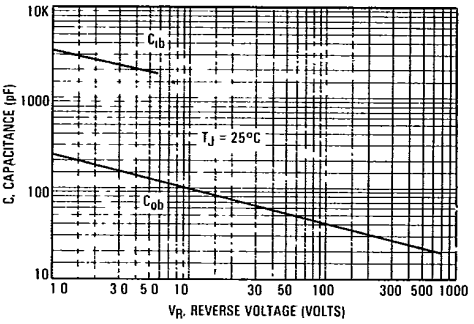


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	HP 214 or Equiv PG 0 to ≈ -35 V 0.02 μF, 100, +V ≈ 11 V, 2N6191, 20, 10 μF, R_{B1}, A, R_{B2}, 0.02 μF, 1.0 μF, 2N5337, 50, 500, 100, -V Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN ON TIME 1, 2, I_{B1} I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 83 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT, 1, Input, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, 2, R_S = 0.1 Ω See Above for Detailed Conditions	OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t V_{CE}, V_{CE} or V_{clamp}, Time, t_2, t t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 1, 2, TUT, R_L, V_{CC}

FIGURE 7 — INDUCTIVE SWITCHING MEASUREMENTS

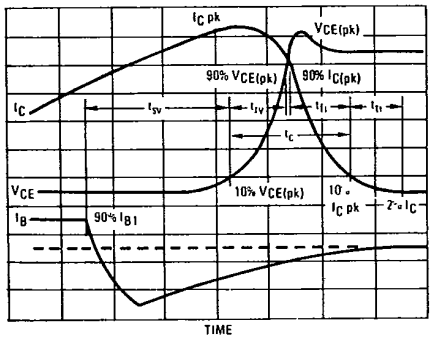
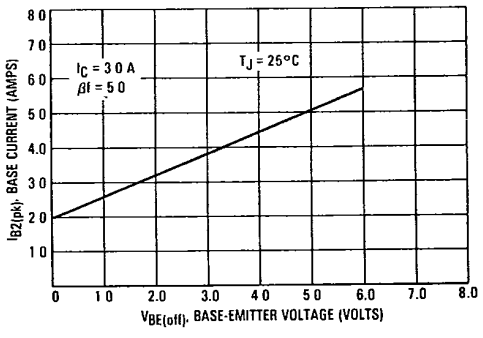


FIGURE 8 — PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

FIGURE 9 — STORAGE TIME

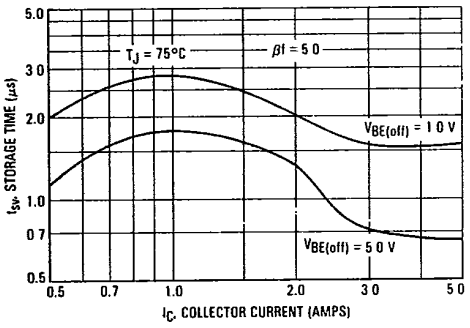


FIGURE 10 — CROSSOVER AND FALL TIMES

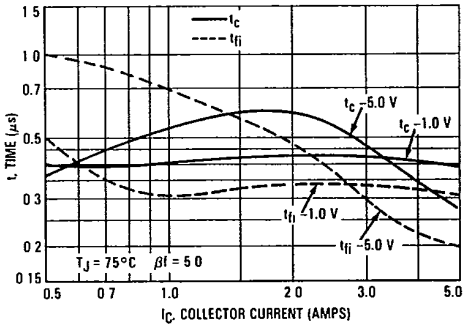
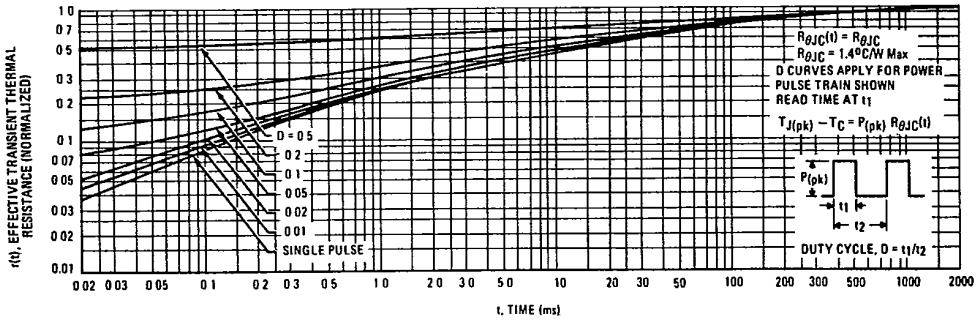


FIGURE 11 — THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

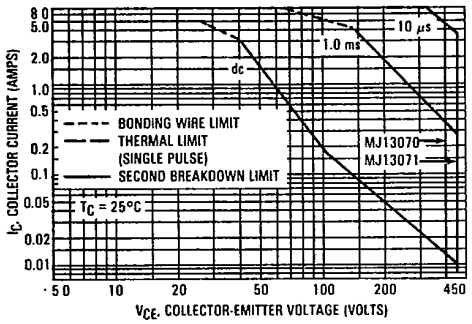
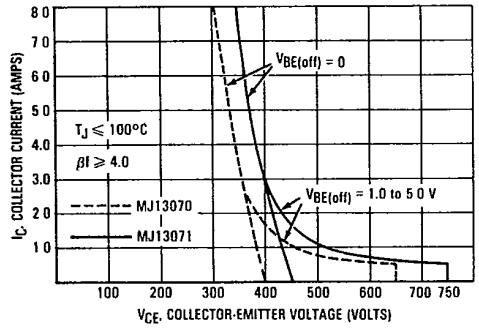


FIGURE 13 — MAXIMUM RATED REVERSE BIAS SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 — POWER DERATING