# The RF Line UHF Power Amplifiers

Capable of wide power range control as encountered in portable cellular radio applications (30 dB typical).

- MHW803-2 806-870 MHz
- Specified 7.5 Volt Characteristics RF Input Power = 1 mW (0 dBm) RF Output Power = 2 Watts Minimum Gain (V<sub>Control</sub> = 4 V) = 33 dB Harmonics = -45 dBc Max @ 2 f<sub>0</sub>
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



2 W, 806 to 905 MHz UHF POWER AMPLIFIERS



## MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit	
DC Supply Voltage (Pins 2,3,4)	V <sub>s1,2,3</sub>	10	Vdc	
DC Control Voltage (Pin 1)	VCont	4	Vdc	
RF Input Power	P <sub>in</sub>	3	mW	
RF Output Power ( $V_{s1} = V_{s2} = V_{s3} = 10 \text{ V}$ )	Pout	3	W	
Operating Case Temperature Range	тс	-30 to +100	°C	
Storage Temperature Range	T <sub>stg</sub>	-30 to +100	°C	

# **ELECTRICAL CHARACTERISTICS** V<sub>S1</sub> = V<sub>S2</sub> = V<sub>S3</sub> = 7.5 Vdc, (Pins 2,3,4), T<sub>C</sub> = 25°C, 50 $\Omega$ System

Characteristic	Symbol	Min	Max	Unit	
Frequency Range	—	806	870	MHz	
Control Voltage (P <sub>out</sub> = 2 W, P <sub>in</sub> = 1 mW) (1)	V <sub>Cont</sub>	0	4	Vdc	
Quiescent Current (V <sub>S1</sub> , Pin 2 = 7.5 Vdc) (2)	I <sub>s1(q)</sub>	—	65	mA	
Power Gain (P <sub>out</sub> = 2 W, V <sub>Cont</sub> = 4 Vdc)	G <sub>p</sub>	33	—	dB	
Efficiency (P <sub>out</sub> = 2 W, P <sub>in</sub> = 1 mW) (1)	η	37	—	%	
$\begin{array}{ll} \text{Harmonics} \left( P_{\text{out}} = 2 \text{ W} \right) \left( 1 \right) & 2 \text{ f}_{\text{o}} \\ \left( P_{\text{in}} = 1 \text{ mW} \right) & 3 \text{ f}_{\text{o}} \end{array}$	-	—	-45 -55	dBc	
Input VSWR ( $P_{out} = 2 \text{ W}, P_{in} = 1 \text{ mW}$ ), 50 $\Omega$ Ref. (1)	—	—	2.0:1	—	
Noise power 30 kHz Bandwidth, 45 MHz above fo $(P_{out} = 2 W (1)  T_C = +25^{\circ}C$ $(P_{in} = 1 mW)  T_C = +100^{\circ}C$			-85 -82	dBm dBm	
Load Mismatch ( $V_{s1} = V_{s2} = V_{s3} = 10 \text{ Vdc}$ ) VSWR = 10:1, P <sub>out</sub> = 3 W, P <sub>in</sub> = 3 mW (1)		No Degradation in Power Output			
Stability ( $P_{in} = 0.5-2 \text{ mW}$ , $V_{S1} = V_{S2} = V_{S3} = 6-9 \text{ Vdc}$ ) $P_{out}$ between 0 mW and 2 W (1) Load VSWR = 6:1, Source VSWR = 3:1)		All spurious outputs more than 60 dB below desired signal			

NOTES:

1. Adjust V<sub>cont</sub> for specified P<sub>out</sub>.

2.  $V_{Cont} = 0$  Vdc.



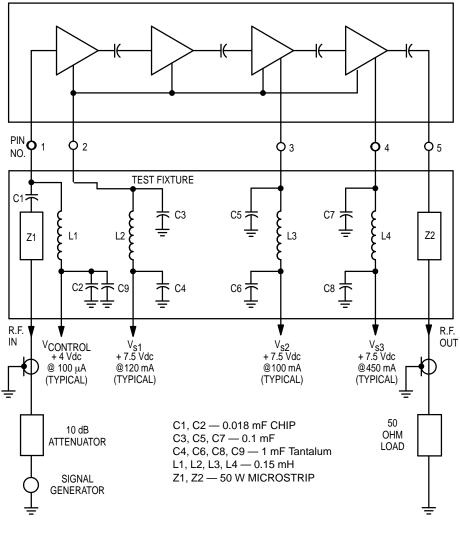
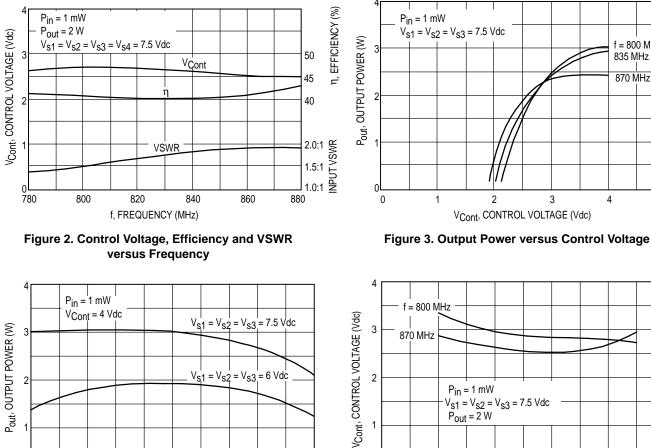


Figure 1. Power Module Test System Block Diagram

# **TYPICAL CHARACTERISTICS**

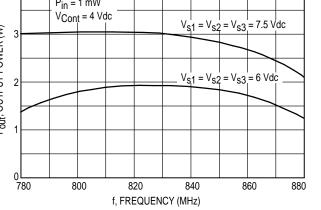


0

-60 -80

-40

-20





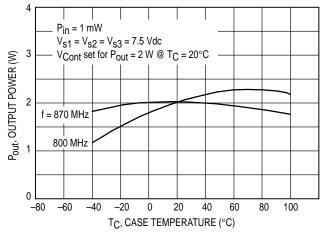


Figure 6. Output Power versus Case Temperature

Figure 5. Control Voltage versus Case Temperature

20

T<sub>C</sub>, CASE TEMPERATURE (°C)

40

60

80 100

0

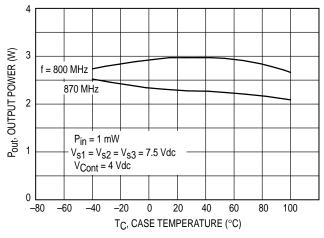


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

f = 800 MHz

835 MHz

870 MHz

4

5

### **APPLICATIONS INFORMATION**

#### NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of  $V_{S1} = V_{S2} = V_{S3} = 7.5$  Vdc (Pins 2, 3, 4) and P<sub>out</sub> equal to 2 watts. With these conditions, maximum current density on any device is  $1.5 \times 10^5$  A/cm<sup>2</sup> and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

#### GAIN CONTROL

The module output should be limited to 2 watts. The preferred method of power output control is to fix  $V_{S1} = V_{S2} = V_{S3}$ = 7.5 Vdc (Pins 2, 3, 4), P<sub>in</sub> (Pin 1) at 1 mW, and vary V<sub>Cont</sub> (Pin 1) voltage.

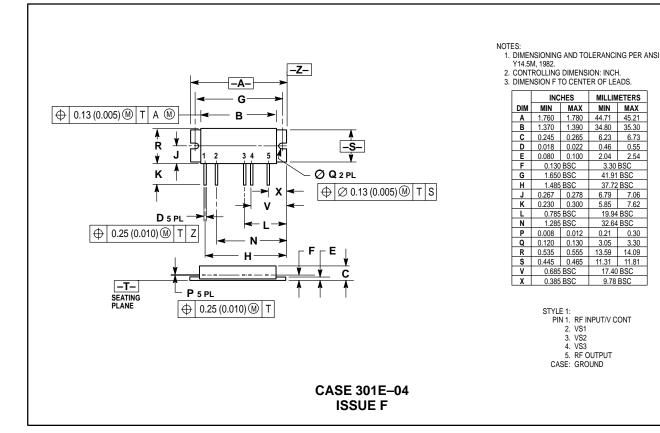
#### DECOUPLING

Due to the high gain of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018  $\mu$ F chip capacitor which is effective for frequencies from 5 MHz through 905 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

#### LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are  $V_{S1} = V_{S2} = V_{S3}$  equal to 10 Vdc, VSWR equal to 10:1, and output power equal to 3 watts.

#### PACKAGE DIMENSIONS



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MILLIMETERS

45.21

35.30

0.55

MIN MAX

34.80

6.23 6.73

2.04 2.54

3.30 BS

41.91 BSC

37.72 BSC

19.94 BSC

32.64 BSC

13.59 14.09

17.40 BS0

9.78 BSC

0.21 0.30

3.05 3.30

0.445 0.465 11.31 11.81

PIN 1. RF INPUT/V CONT 2. VS1 3. VS2 4. VS3 5 RE OUTPUT CASE: GROUND

 6.79
 7.06

 5.85
 7.62

0.46

INCHES MIN MAX

1.370 1.390

0.245 0.265

0.080 0.100

0.130 BSC

1.650 BSC

1.485 BSC

0.267 0.278 0.230 0.300

0.785 BSC

1.285 BSC

0.008 0.012

0.685 BSC

0.385 BSC

STYLE 1:

Α В

С

Е

F

J

L

Р

S V

X

1.760 1.780 44.71