Single/Dual Programmable Supply Current, R-R Output, Current Feedback Amplifiers

FEATURES

- **Programmable Supply Current and Bandwidth:** 10MHz at 300µA per Amplifier up to 200MHz at 6mA per Amplifier
- **Rail-to-Rail Output:** 0.05V to 2.85V on 3V Single Supply
- **High Slew Rate:** 700V/µs
- **High Output Drive:** ±75mA Minimum Output Current
- **C-Load™ Op Amp Drives All Capacitive Loads**
- **Low Distortion:** –70dB HD2 at 1MHz $2V_{P-P}$ –75dB HD3 at 1MHz $2V_{P-P}$
- **Fast Settling:** 20ns 0.1% Settling for 2V Step
- **Excellent Video Performance Into 150Ω Load:** Differential Gain of 0.20%, Differential Phase of 0.10°
- **Wide Supply Range:** 3V to 12V Single Supply ±1.5V to ±6V Dual Supplies
- **Small Size:** Low Profile (1mm) 6-Lead SOT-23 (ThinSOT™), 3mm x 3mm x 0.8mm DFN and 10-Lead MSOP Packages

DESCRIPTION

The LT®6210/LT6211 are single/dual current feedback amplifiers with externally programmable supply current and bandwidth ranging from 10MHz at 300µA per amplifier to 200MHz at 6mA per amplifier. They feature a low distortion rail-to-rail output stage, 700V/µs slew rate and a minimum output current drive of 75mA.

The LT6210/LT6211 operate on supplies as low as a single 3V and up to either 12V or ±6V. The I_{SET} pin allows for the optimization of quiescent current for specific bandwidth, distortion or slew rate requirements. Regardless of supply voltage, the supply current is programmable from just 300µA to 6mA per amplifier with an external resistor or current source.

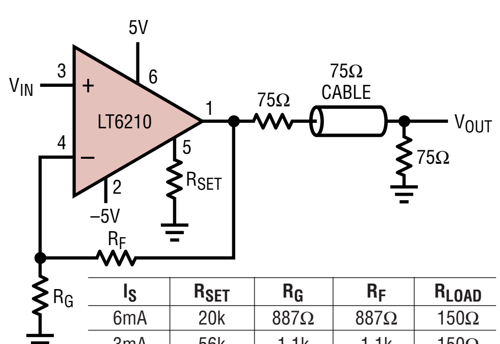
The LT6210 is available in the low profile (1mm) 6-lead SOT-23 package. The LT6211 is available in the 10-lead MSOP and the 3mm x 3mm x 0.8mm DFN packages.

APPLICATIONS

- Buffers
- Video Amplifiers
- Cable Drivers
- Mobile Communication
- Low Power/Battery Applications

TYPICAL APPLICATION

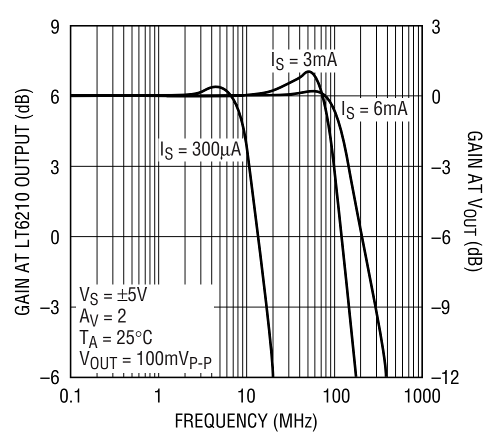
Line Driver Configuration for Various Supply Currents



I_S	R_{SET}	R_G	R_F	R_{LOAD}
6mA	20k	887Ω	887Ω	150Ω
3mA	56k	1.1k	1.1k	150Ω
300µA	1M	11k	11k	1k

6210 TA01

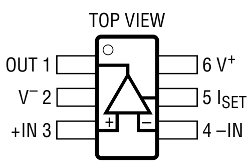
Small Signal Response vs Supply Current



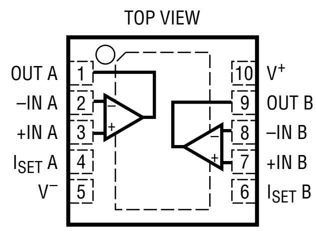
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 13.2V
Input Current .... ±10mA
Output Current .... ±80mA
Output Short-Circuit Duration (Note 2) .... Indefinite
Operating Temperature Range (Note 3) ... –40°C to 85°C
Specified Temperature Range (Note 4) .... –40°C to 85°C
Junction Temperature (Note 5) .... 150°C
Junction Temperature (DD Package) .... 125°C
Storage Temperature Range .... –65°C to 150°C
Storage Temperature Range
(DD Package) .... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

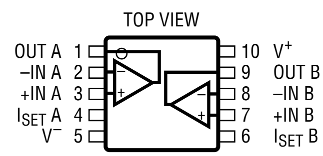
PACKAGE/ORDER INFORMATION



S6 PACKAGE
6-LEAD PLASTIC SOT-23
T_{JMAX} = 150°C, θ_{JA} = 230°C/W (NOTE 5)



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
UNDERSIDE METAL CONNECTED TO V^-
(PCB CONNECTION OPTIONAL)
T_{JMAX} = 125°C, θ_{JA} = 43°C/W (NOTE 5)



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 120°C/W (NOTE 5)

ORDER PART NUMBER	S6 PART MARKING*	ORDER PART NUMBER	DD PART MARKING*	ORDER PART NUMBER	MS PART MARKING
LT6210CS6 LT6210IS6	LTA3	LT6211CDD LT6211IDD	LBCD	LT6211CMS LT6211IMS	LTBBN LTBBP

*The temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS (I_S = 6mA per Amplifier)

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. For V^+ = 5V, V^- = –5V: R_{SET} = 20k to ground, A_V = +2, R_F = R_G = 887Ω, R_L = 150Ω; For V^+ = 3V, V^- = 0V: R_{SET} = 0Ω to V^-, A_V = +2, R_F = 887Ω, R_G = 887Ω to 1.5V, R_L = 150Ω to 1.5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		V^+ = 5V, V^- = –5V, I_S = 6mA MIN	 TYP	 MAX	V^+ = 3V, V^- = 0V, I_S = 6mA MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage		 ●		–1	±6 ±9		–1	±6.5 ±10	mV mV
$I_{IN}+$	Noninverting Input Current		 ●		–3.5	±7 ±9		–3	±6.5 ±8	µA µA
$I_{IN}–$	Inverting Input Current		 ●		–13.5	±39 ±55		2.5	±25 ±40	µA µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 887Ω, R_G = 46.4Ω, R_S = 0Ω			6.5			6.5		nV/√Hz
$+i_n$	Input Noise Current Density	f = 1kHz			4.5			4.5		pA/√Hz
$–i_n$	Input Noise Current Density	f = 1kHz			25			25		pA/√Hz
$R_{IN}+$	Noninverting Input Resistance	V_{IN} = V^+ – 1.2V to V^- + 1.2V	●	0.5	2		0.3	1.7		MΩ
$C_{IN}+$	Noninverting Input Capacitance	f = 100kHz			2			2		pF
V_{INH}	Input Voltage Range, High	(Note 10)	●	3.8	4.2		1.8	2.2		V
V_{INL}	Input Voltage Range, Low	(Note 10)	●		–4.2	–3.8		0.8	1.2	V
V_{OUTH}	Output Voltage Swing, High	R_L = 1k (Note 11) R_L = 150Ω (Note 11) R_L = 150Ω (Note 11)	 ●	 4.4 4.2	4.8 4.6		 2.65 2.6	2.85 2.75		V V V
V_{OUTL}	Output Voltage Swing, Low	R_L = 1k (Note 11) R_L = 150Ω (Note 11) R_L = 150Ω (Note 11)	 ●		–4.95 –4.8	 –4.55 –4.4		0.05 0.1	 0.3 0.35	V V V
CMRR	Common Mode Rejection Ratio	V_{IN} = V^+ – 1.2V to V^- + 1.2V	 ●	46 43	50			46		dB dB
$–I_{CMRR}$	Inverting Input Current Common Mode Rejection	V_{IN} = V^+ – 1.2V to V^- + 1.2V	 ●		0.15	±1.5 ±2		0.2		µA/V µA/V
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±6V (Note 6)	●	60	85		60	85		dB
$–I_{PSRR}$	Inverting Input Current Power Supply Rejection	V_S = ±1.5V to ±6V (Note 6)	 ●		2	±7 ±8		2	±7 ±8	µA/V µA/V
I_S	Supply Current per Amplifier		 ●		6	8.5 10		5.8	8.3 9	mA mA

ELECTRICAL CHARACTERISTICS (I_S = 6mA per Amplifier)

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. For V^+ = 5V, V^- = –5V: R_{SET} = 20k to ground, A_V = +2, R_F = R_G = 887Ω, R_L = 150Ω; For V^+ = 3V, V^- = 0V: R_{SET} = 0Ω to V^-, A_V = +2, R_F = 887Ω, R_G = 887Ω to 1.5V, R_L = 150Ω to 1.5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		V^+ = 5V, V^- = –5V, I_S = 6mA MIN	TYP	MAX	V^+ = 3V, V^- = 0V, I_S = 6mA MIN	TYP	MAX	UNITS
I_{OUT}	Maximum Output Current	R_L = 0Ω (Notes 7, 11)	●	±75			±45			mA
R_{OL}	Transimpedance, $\Delta V_{OUT}/\Delta I_{IN}$–	V_{OUT} = V^+ – 1.2V to V^- + 1.2V		65	115		65	115		kΩ
SR	Slew Rate	(Note 8)		500	700			200		V/µs
t_{pd}	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 100m$V_{P\text{-}P}$, Larger of t_{pd}+, t_{pd}–			1.5			2.4		ns
BW	–3dB Bandwidth	<1dB Peaking, A_V = 1			200			120		MHz
t_s	Settling Time	To 0.1% of V_{FINAL}, V_{STEP} = 2V			20			25		ns
t_f, t_r	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = 100m$V_{P\text{-}P}$			2			3.5		ns
dG	Differential Gain	(Note 9)			0.20			0.35		%
dP	Differential Phase	(Note 9)			0.10			0.20		Deg
HD2	2nd Harmonic Distortion	f = 1MHz, V_{OUT} = 2$V_{P\text{-}P}$			–70			–65		dBc
HD3	3rd Harmonic Distortion	f = 1MHz, V_{OUT} = 2$V_{P\text{-}P}$			–75			–75		dBc

(I_S = 3mA per Amplifier)

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. For V^+ = 5V, V^- = –5V: R_{SET} = 56k to ground, A_V = +2, R_F = R_G = 1.1k, R_L = 150Ω; For V^+ = 3V, V^- = 0V: R_{SET} = 10k to V^-, A_V = +2, R_F = 1.27k, R_G = 1.27k to 1.5V, R_L = 150Ω to 1.5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		V^+ = 5V, V^- = –5V, I_S = 3mA MIN	TYP	MAX	V^+ = 3V, V^- = 0V, I_S = 3mA MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		 ●		–1	±5.5 ±8.5		–1.5	±5.5 ±8.5	mV mV
I_{IN}+	Noninverting Input Current		 ●		–1.5	±5 ±7		–1.5	±5 ±7	µA µA
I_{IN}–	Inverting Input Current		 ●		–12	±36 ±52		–3	±15 ±20	µA µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1.1k, R_G = 57.6Ω, R_S = 0Ω			7			7		nV/√Hz
+i_n	Input Noise Current Density	f = 1kHz			1.5			1.5		pA/√Hz
–i_n	Input Noise Current Density	f = 1kHz			15			15		pA/√Hz
R_{IN}+	Noninverting Input Resistance	V_{IN} = V^+ – 1.2V to V^- + 1.2V	●	0.5	3		1	2.5		MΩ
C_{IN}+	Noninverting Input Capacitance	f = 100kHz			2			2		pF
V_{INH}	Input Voltage Range, High	(Note 10)	●	3.8	4.1		1.8	2.1		V
V_{INL}	Input Voltage Range, Low	(Note 10)	●		–4.1	–3.8		0.9	1.2	V
V_{OUTH}	Output Voltage Swing, High	R_L = 1k (Note 11) R_L = 150Ω (Note 11) R_L = 150Ω (Note 11)	 ●	 4.3 4.1	4.8 4.6		 2.6 2.55	2.9 2.8		V V V
V_{OUTL}	Output Voltage Swing, Low	R_L = 1k (Note 11) R_L = 150Ω (Note 11) R_L = 150Ω (Note 11)	 ●		–4.95 –4.8	 –4.55 –4.4		0.05 0.1	 0.3 0.35	V V V
CMRR	Common Mode Rejection Ratio	V_{IN} = V^+ – 1.2V to V^- + 1.2V	 ●	46 43	50			46		dB dB
–I_{CMRR}	Inverting Input Current Common Mode Rejection	V_{IN} = V^+ – 1.2V to V^- + 1.2V	 ●		0.3	±1.5 ±2		0.4		µA/V µA/V

ELECTRICAL CHARACTERISTICS (I_S = 3mA per Amplifier)

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. For V^+ = 5V, V^- = –5V: R_{SET} = 56k to ground, A_V = +2, R_F = R_G = 1.1k, R_L = 150Ω; For V^+ = 3V, V^- = 0V: R_{SET} = 10k to V^-, A_V = +2, R_F = 1.27k, R_G = 1.27k to 1.5V, R_L = 150Ω to 1.5V unless otherwise specified.

				V^+ = 5V, V^- = –5V, I_S = 3mA			V^+ = 3V, V^- = 0V, I_S = 3mA			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±6V (Note 6)	●	60	85		60	85		dB
$–I_{PSRR}$	Inverting Input Current Power Supply Rejection	V_S = ±1.5V to ±6V (Note 6)	 ●		1.5	±7 ±8		1.5	±7 ±8	µA/V µA/V
I_S	Supply Current per Amplifier		 ●		3	4.1 4.55		3	4.1 4.4	mA mA
I_{OUT}	Maximum Output Current	R_L = 0Ω (Notes 7, 11)	●	±70			±45			mA
R_{OL}	Transimpedance, $\Delta V_{OUT}/\Delta I_{IN}–$	V_{OUT} = V^+ –1.2V to V^- +1.2V		65	120		65	120		kΩ
SR	Slew Rate	(Note 8)		450	600			150		V/µs
t_{pd}	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 100mV_{P-P}, Larger of t_{pd}+, t_{pd}–			3.1			4.7		ns
BW	–3dB Bandwidth	<1dB Peaking, A_V = 1			100			70		MHz
t_s	Settling Time	To 0.1% of V_{FINAL}, V_{STEP} = 2V			20			25		ns
t_f, t_r	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = 100mV_{P-P}			3			5.6		ns
dG	Differential Gain	(Note 9)			0.35			0.42		%
dP	Differential Phase	(Note 9)			0.30			0.44		Deg
HD2	2nd Harmonic Distortion	f = 1MHz, V_{OUT} = 2V_{P-P}			–65			–60		dBc
HD3	3rd Harmonic Distortion	f = 1MHz, V_{OUT} = 2V_{P-P}			–65			–65		dBc

(I_S = 300µA per Amplifier)

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. For V^+ = 5V, V^- = –5V: R_{SET} = 1M to ground, A_V = +2, R_F = R_G = 11k, R_L = 1k; For V^+ = 3V, V^- = 0V: R_{SET} = 270k to V^-, A_V = +2, R_F = 9.31k, R_G = 9.31k to 1.5V, R_L = 1k to 1.5V unless otherwise specified.

				V^+ = 5V, V^- = –5V, I_S = 300µA			V^+ = 3V, V^- = 0V, I_S = 300µA			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage		 ●		–1	±4.5 ±8		–1.5	±4.5 ±8	mV mV
$I_{IN}+$	Noninverting Input Current		 ●		0.2	±1 ±2		0.2	±1 ±1.5	µA µA
$I_{IN}–$	Inverting Input Current		 ●		–3	±8.5 ±11		–0.5	±3 ±4.5	µA µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 13k, R_G = 681Ω, R_S = 0Ω			13.5			13.5		nV/√Hz
$+i_n$	Input Noise Current Density	f = 1kHz			0.75			0.75		pA/√Hz
$–i_n$	Input Noise Current Density	f = 1kHz			5			5		pA/√Hz
$R_{IN}+$	Noninverting Input Resistance	V_{IN} = V^+ – 1.2V to V^- + 1.2V (Note 8)	●	1	25		1	15		MΩ
$C_{IN}+$	Noninverting Input Capacitance	f = 100kHz			2			2		pF
V_{INH}	Input Voltage Range, High	(Note 10)	●	3.8	4.1		1.8	2.1		V
V_{INL}	Input Voltage Range, Low	(Note 10)	●		–4.1	–3.8		0.9	1.2	V
V_{OUTH}	Output Voltage Swing, High	R_L = 1k (Note 11)	 ●	4.75 4.7	4.85		2.75 2.7	2.85		V V
V_{OUTL}	Output Voltage Swing, Low	R_L = 1k (Note 11)	 ●		–4.95	–4.85 –4.8		0.05	0.15 0.2	V V

ELECTRICAL CHARACTERISTICS (I_S = 300µA per Amplifier)

The ● denotes specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C. For V^+ = 5V, V^- = –5V: R_{SET} = 1M to ground, A_V = +2, R_F = R_G = 11k, R_L = 1k; For V^+ = 3V, V^- = 0V: R_{SET} = 270k to V^-, A_V = +2, R_F = 9.31k, R_G = 9.31k to 1.5V, R_L = 1k to 1.5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		V^+ = 5V, V^- = –5V, I_S = 300µA MIN	TYP	MAX	V^+ = 3V, V^- = 0V, I_S = 300µA MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_{IN} = V^+ – 1.2V to V^- + 1.2V	 ●	46 43	50			46		dB dB
$–I_{CMRR}$	Inverting Input Current Common Mode Rejection	V_{IN} = V^+ – 1.2V to V^- + 1.2V	 ●		0.15	±1.5 ±2		0.2		µA/V µA/V
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±6V (Note 6)	●	60	85		60	85		dB
$–I_{PSRR}$	Inverting Input Current Power Supply Rejection	V_S = ±1.5V to ±6V (Note 6)	 ●		0.4	±2.2 ±4		0.4	±2.2 ±4	µA/V µA/V
I_S	Supply Current per Amplifier		 ●		0.3	0.525 0.6		0.3	0.38 0.43	mA mA
I_{OUT}	Maximum Output Current	R_L = 0Ω (Notes 7, 11)	●	±30			±10			mA
R_{OL}	Transimpedance, $\Delta V_{OUT}/\Delta I_{IN}–$	V_{OUT} = V^+ – 1.2V to V^- + 1.2V		300	660		65	120		kΩ
SR	Slew Rate	(Note 8)		120	170			20		V/µs
t_{pd}	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 100mV_{P-P}, Larger of $t_{pd}+$, $t_{pd}–$			30			50		ns
BW	–3dB Bandwidth	<1dB Peaking, A_V = 1			10			7.5		MHz
t_s	Settling Time	To 0.1% of V_{FINAL}, V_{STEP} = 2V			200			300		ns
t_f, t_r	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = 100mV_{P-P}			40			50		ns
HD2	2nd Harmonic Distortion	f = 1MHz, V_{OUT} = 2V_{P-P}			–40			–45		dBc
HD3	3rd Harmonic Distortion	f = 1MHz, V_{OUT} = 2V_{P-P}			–45			–45		dBc

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: As long as output current and junction temperature are kept below the absolute maximum ratings, no damage to the part will occur. Depending on the supply voltage, a heat sink may be required.

Note 3: The LT6210C/LT6211C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 4: The LT6210C/LT6211C is guaranteed to meet specified performance from 0°C to 70°C. The LT6210C/LT6211C is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6210I/LT6211I is guaranteed to meet specified performance from –40°C to 85°C.

Note 5: The LT6210 with no metal connected to the V^- pin has a θ_{JA} of 230°C/W, however, thermal resistances vary depending upon the amount of PC board metal attached to Pin 2 of the device. With the LT6210 mounted on a 2500mm^2 3/32" FR-4 board covered with 2oz copper on both sides and with just 20mm^2 of copper attached to Pin 2, θ_{JA} drops to 160°C/W. Thermal performance can be improved even further by using a 4-layer board or by attaching more metal area to Pin 2.

Thermal resistance of the LT6211 in MSOP-10 is specified for a 2500mm^2 3/32" FR-4 board covered with 2oz copper on both sides and with 100mm^2 of copper attached to Pin 5. Its performance can also be increased with additional copper much like the LT6210.

To achieve the specified θ_{JA} of 43°C/W for the LT6211 DFN-10, the exposed pad must be soldered to the PCB. In this package, θ_{JA} will benefit from increased copper area attached to the exposed pad.

T_J is calculated from the ambient temperature T_A and the power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The maximum power dissipation can be calculated by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + (V_S/2)^2/R_{LOAD}$$

Note 6: For PSRR and $–I_{PSRR}$ testing, the current into the I_{SET} pin is constant, maintaining a consistent LT6210/LT6211 quiescent bias point. A graph of PSRR vs Frequency is included in the Typical Performance Characteristics showing +PSRR and –PSRR with R_{SET} connecting I_{SET} to ground.

Note 7: While the LT6210 and LT6211 circuitry is capable of significant output current even beyond the levels specified, sustained short-circuit current exceeding the Absolute Maximum Rating of ±80mA may permanently damage the device.

Note 8: This parameter is guaranteed to meet specified performance through design and characterization. It is not production tested.

Note 9: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Five identical amplifier stages were cascaded giving an effective resolution of 0.02% and 0.02°.

Note 10: Input voltage range on ±5V dual supplies is guaranteed by CMRR. On 3V single supply it is guaranteed by design and by correlation to the ±5V input voltage range limits.

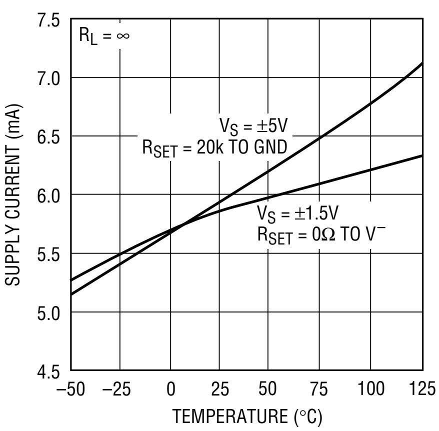
Note 11: This parameter is tested by forcing a 50mV differential voltage between the inverting and noninverting inputs.

TYPICAL AC PERFORMANCE

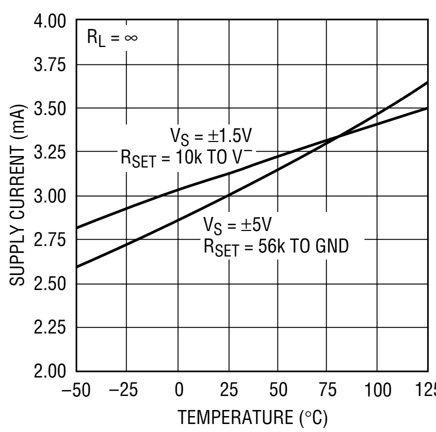
V_S (V)	I_S (mA) per Amplifier	R_{SET} (Ω)	A_V	R_L (Ω)	R_F (Ω)	R_G (Ω)	SMALL-SIGNAL –3dB BW, <1dB PEAKING (MHz)	SMALL-SIGNAL ±0.1dB BW (MHz)
±5	6	20k	1	150	1200	—	200	30
±5	6	20k	2	150	887	887	160	30
±5	6	20k	–1	150	698	698	140	20
±5	3	56k	1	150	1690	—	100	15
±5	3	56k	2	150	1100	1100	100	15
±5	3	56k	–1	150	1200	1200	80	15
±5	0.3	1MEG	1	1k	13.7k	—	10	2
±5	0.3	1MEG	2	1k	11k	11k	10	2
±5	0.3	1MEG	–1	1k	10k	10k	10	1.8
3, 0	6	0	1	150	1100	—	120	20
3, 0	6	0	2	150	887	887	100	20
3, 0	6	0	–1	150	806	806	100	20
3, 0	3	10k	1	150	1540	—	70	15
3, 0	3	10k	2	150	1270	1270	60	15
3, 0	3	10k	–1	150	1200	1200	60	15
3, 0	0.3	270k	1	1k	13k	—	7.5	2
3, 0	0.3	270k	2	1k	9.31k	9.31k	7	1.5
3, 0	0.3	270k	–1	1k	10k	10k	7	1.5

TYPICAL PERFORMANCE CHARACTERISTICS

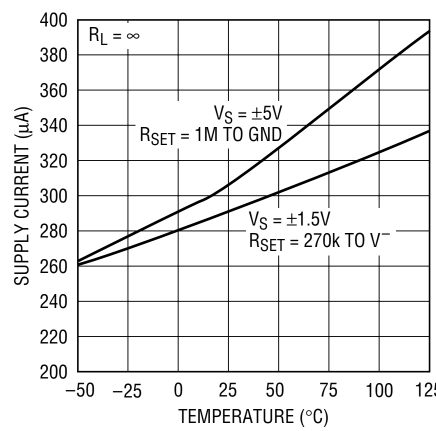
Supply Current per Amplifier vs Temperature



Supply Current per Amplifier vs Temperature

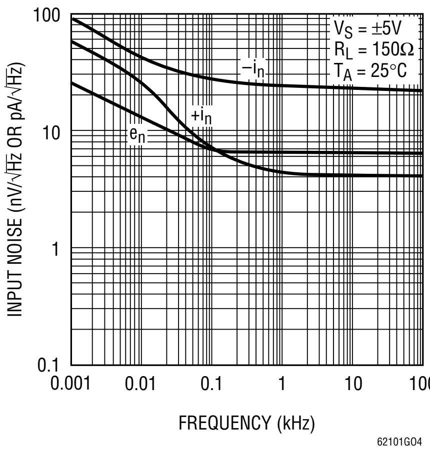


Supply Current per Amplifier vs Temperature

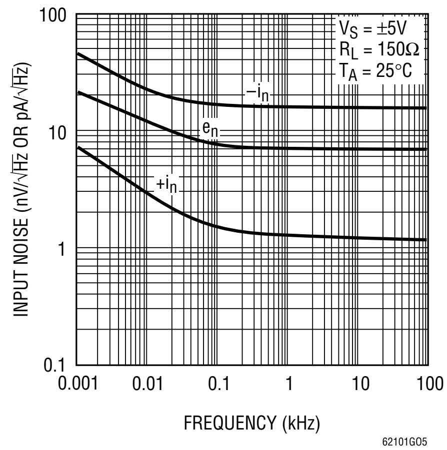


TYPICAL PERFORMANCE CHARACTERISTICS (Supply Current Is Measured Per Amplifier)

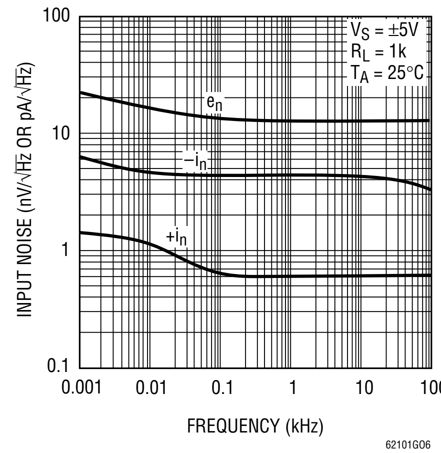
Input Noise Spectral Density (I_S = 6mA per Amplifier)



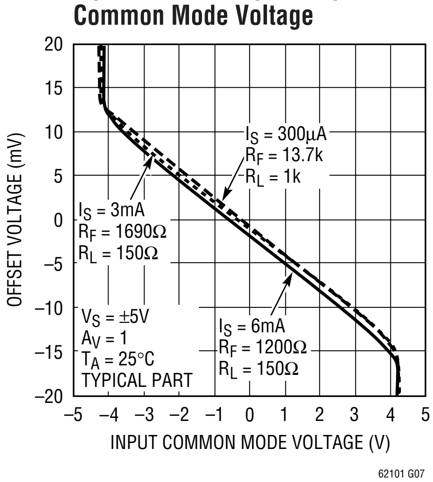
Input Noise Spectral Density (I_S = 3mA per Amplifier)



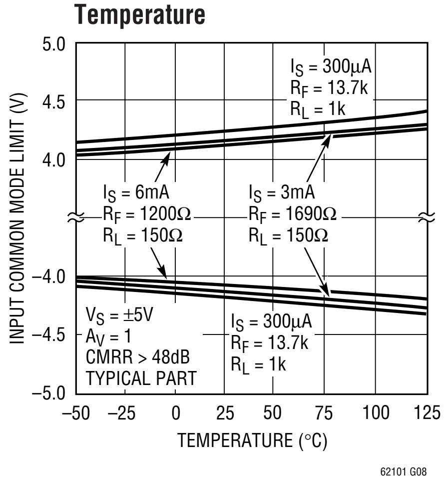
Input Noise Spectral Density (I_S = 300μA per Amplifier)



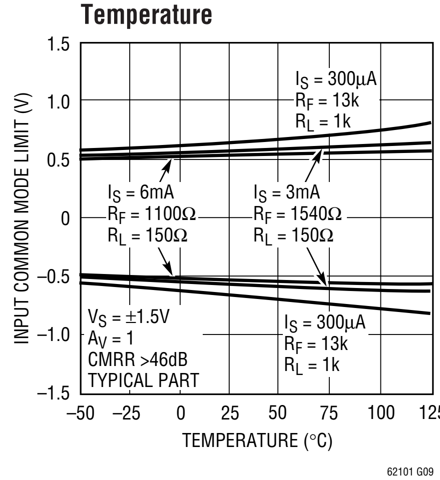
Input Offset Voltage vs Input Common Mode Voltage



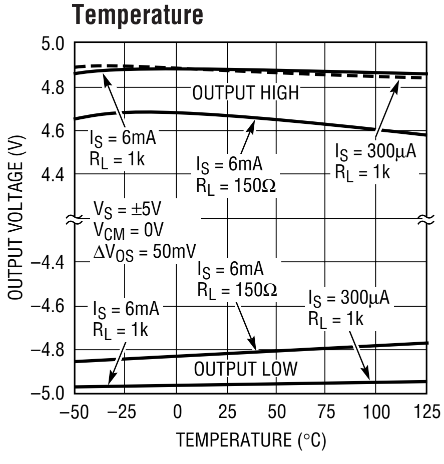
Input Common Mode Range vs Temperature



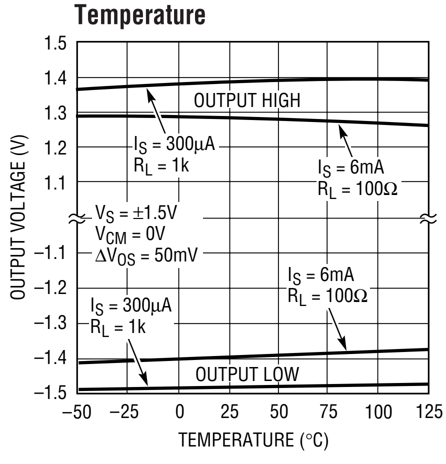
Input Common Mode Range vs Temperature



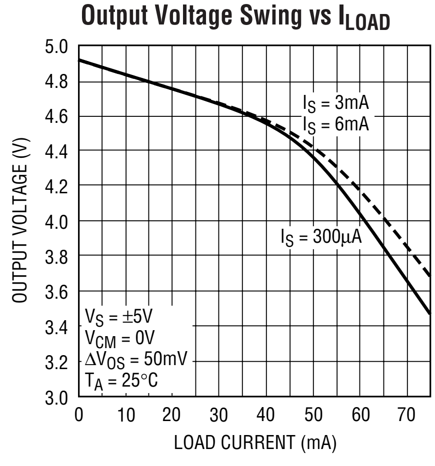
Output Voltage Swing vs Temperature



Output Voltage Swing vs Temperature

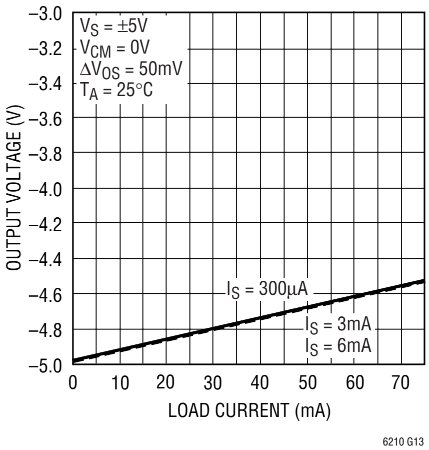


Output Voltage Swing vs I_{LOAD}

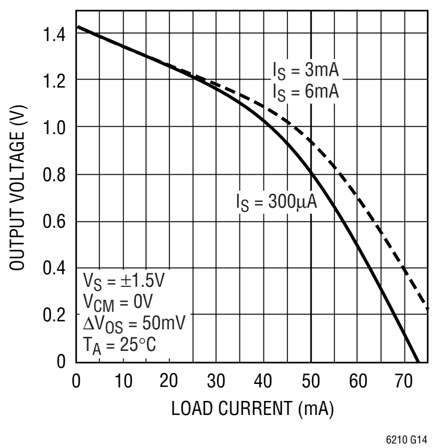


TYPICAL PERFORMANCE CHARACTERISTICS (Supply Current Is Measured Per Amplifier)

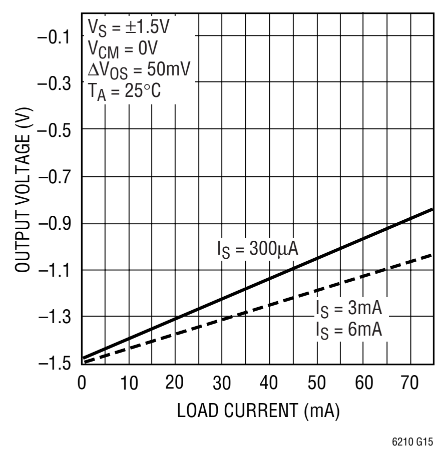
Output Voltage Swing vs I_{LOAD}



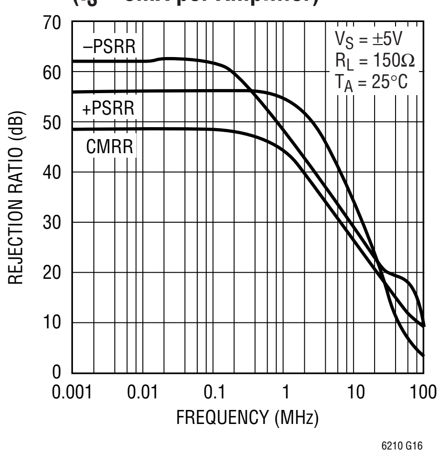
Output Voltage Swing vs I_{LOAD}



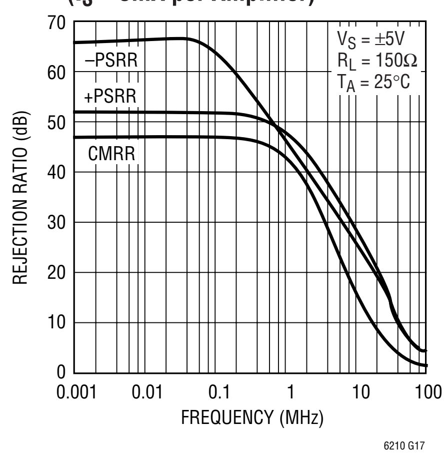
Output Voltage Swing vs I_{LOAD}



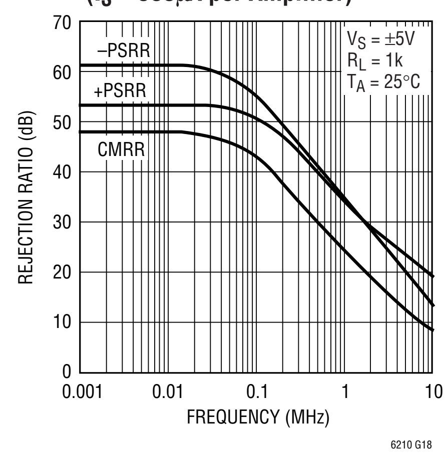
CMRR and PSRR vs Frequency (I_S = 6mA per Amplifier)



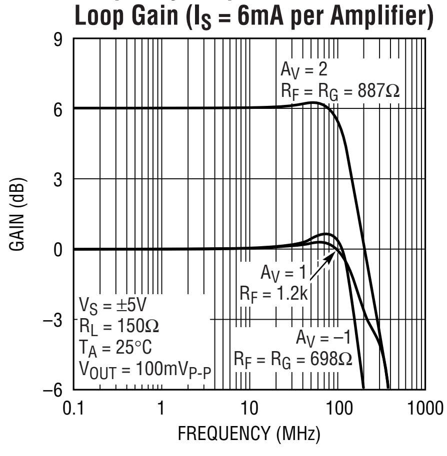
CMRR and PSRR vs Frequency (I_S = 3mA per Amplifier)



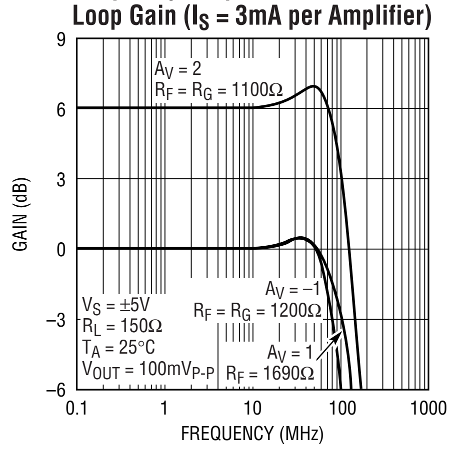
CMRR and PSRR vs Frequency (I_S = 300µA per Amplifier)



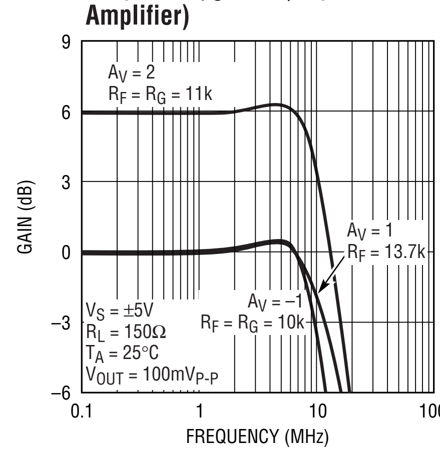
Frequency Response vs Closed Loop Gain (I_S = 6mA per Amplifier)



Frequency Response vs Closed Loop Gain (I_S = 3mA per Amplifier)

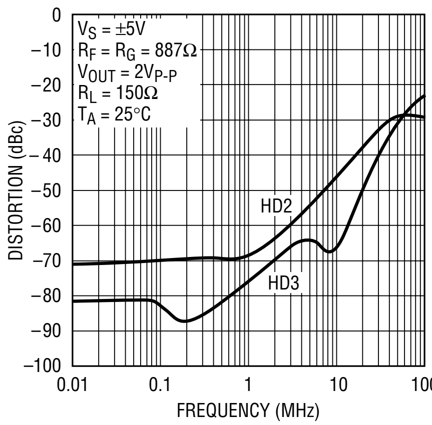


Frequency Response vs Closed Loop Gain (I_S = 300µA per Amplifier)



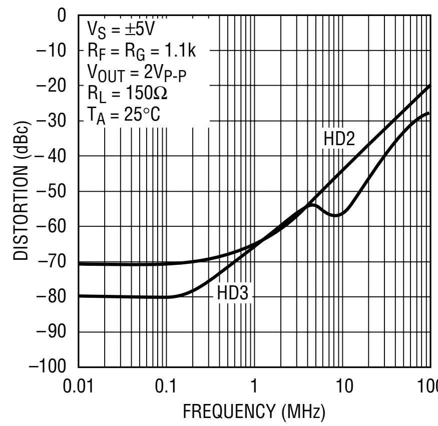
TYPICAL PERFORMANCE CHARACTERISTICS (Supply Current Is Measured Per Amplifier)

2nd and 3rd Harmonic Distortion vs Frequency (I_S = 6mA per Amplifier)



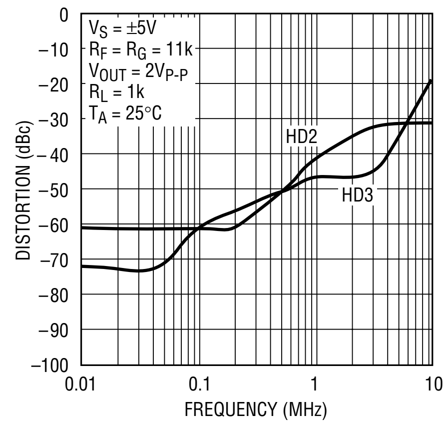
6210 G22

2nd and 3rd Harmonic Distortion vs Frequency (I_S = 3mA per Amplifier)



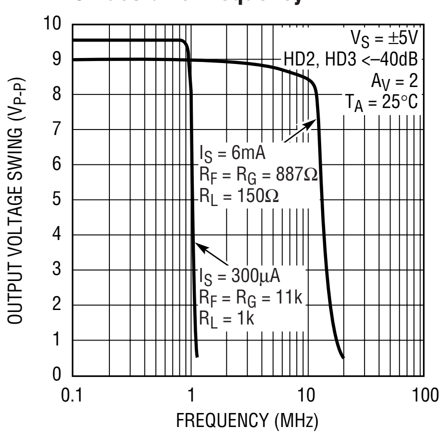
6210 G23

2nd and 3rd Harmonic Distortion vs Frequency (I_S = 300µA per Amplifier)



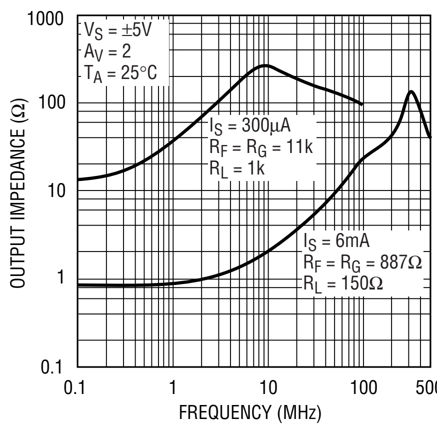
6210 G24

Maximum Undistorted Output Sinusoid vs Frequency



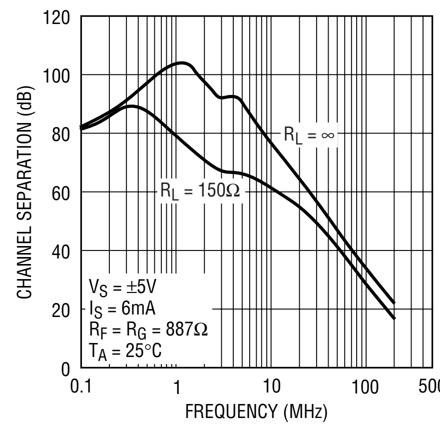
6210 G25

Output Impedance vs Frequency



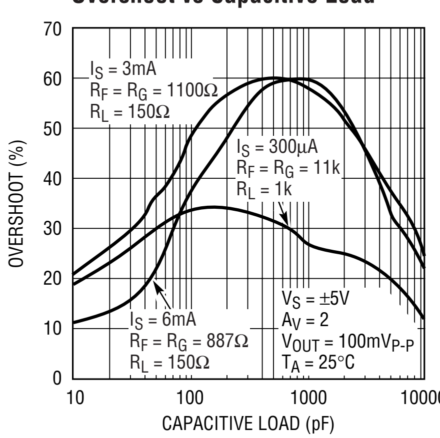
6210 G26

LT6211 Channel Separation vs Frequency



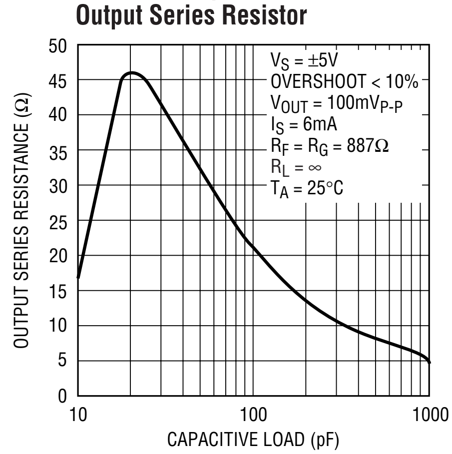
6210 G27

Overshoot vs Capacitive Load



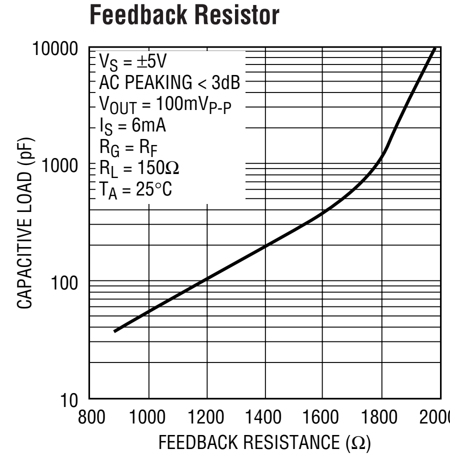
6210 G28

Maximum Capacitive Load vs Output Series Resistor



6210 G29

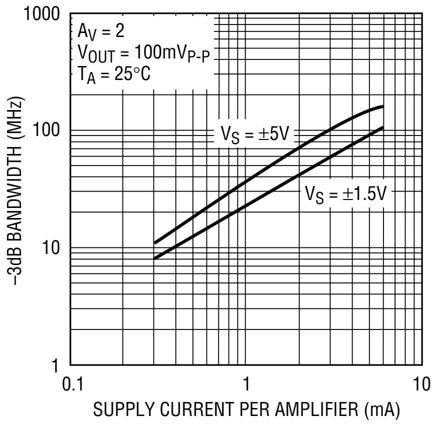
Maximum Capacitive Load vs Feedback Resistor



6210 G30

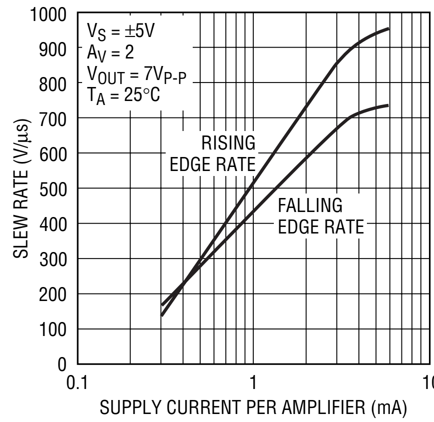
TYPICAL PERFORMANCE CHARACTERISTICS (Supply Current Is Measured Per Amplifier)

–3dB Small-Signal Bandwidth vs Supply Current



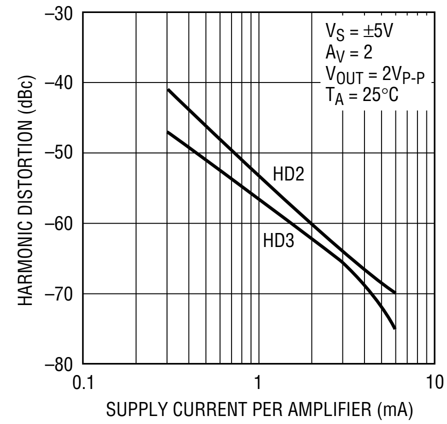
62101 G33

Slew Rate vs Supply Current



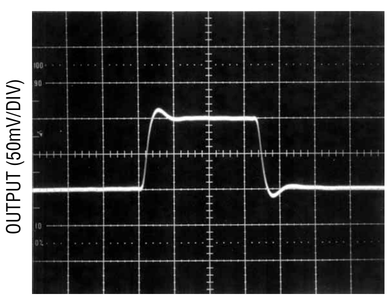
62101 G32

1MHz 2nd and 3rd Harmonic Distortion vs Supply Current



62101 G31

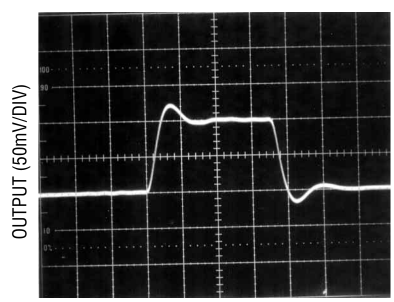
Small-Signal Transient Response (I_S = 6mA per Amplifier)



$V_S = ±5V$ TIME (10ns/DIV)
$V_{IN} = ±25mV$
$R_F = R_G = 887\Omega$
R_{SET} = 20k TO GND
$R_L = 150\Omega$

62101 G34

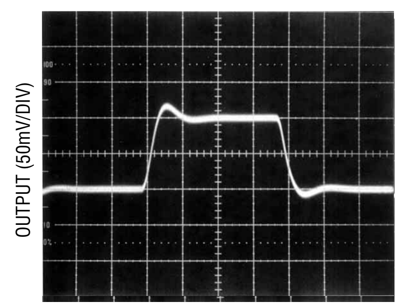
Small-Signal Transient Response (I_S = 3mA per Amplifier)



$V_S = ±5V$ TIME (10ns/DIV)
$V_{IN} = ±25mV$
$R_F = R_G = 1.1k$
R_{SET} = 56k TO GND
$R_L = 150\Omega$

62101 G35

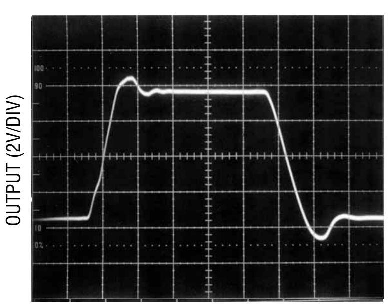
Small-Signal Transient Response (I_S = 300µA per Amplifier)



$V_S = ±5V$ TIME (100ns/DIV)
$V_{IN} = ±25mV$
$R_F = R_G = 11k$
R_{SET} = 1M TO GND
$R_L = 1k$

62101 G36

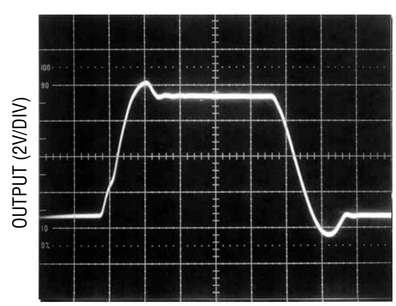
Large-Signal Transient Response (I_S = 6mA per Amplifier)



$V_S = ±5V$ TIME (10ns/DIV)
$V_{IN} = ±1.75V$
$R_F = R_G = 887\Omega$
R_{SET} = 20k TO GND
$R_L = 150\Omega$

62101 G37

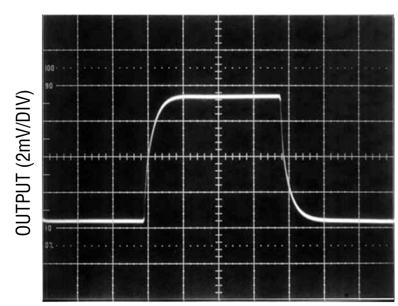
Large-Signal Transient Response (I_S = 3mA per Amplifier)



$V_S = ±5V$ TIME (10ns/DIV)
$V_{IN} = ±1.75V$
$R_F = R_G = 1.1k$
R_{SET} = 56k TO GND
$R_L = 150\Omega$

62101 G38

Large-Signal Transient Response (I_S = 300µA per Amplifier)



$V_S = ±5V$ TIME (100ns/DIV)
$V_{IN} = ±1.75V$
$R_F = R_G = 11k$
R_{SET} = 1M TO GND
$R_L = 1k$

62101 G39

APPLICATIONS INFORMATION

Setting the Quiescent Operating Current (I_{SET} Pin)

The quiescent bias point of the LT6210/LT6211 is set with either an external resistor from the I_{SET} pin to a lower potential or by drawing a current out of the I_{SET} pin. However, the I_{SET} pin is not designed to function as a shutdown. The LT6211 uses two entirely independent bias networks, so while each channel can be programmed for a different supply current, neither I_{SET} pin should be left unconnected. A simplified schematic of the internal biasing structure can be seen in Figure 1. Figure 2 illustrates the results of varying R_{SET} on 3V and ±5V supplies. Note that shorting the I_{SET} pin under 3V operation results in a quiescent bias of approximately 6mA. Attempting to bias the LT6210/LT6211 at a current level higher than 6mA by using a smaller resistor may result in instability and decreased performance. However, internal circuitry clamps the supply current of the part at a safe level of approximately 15mA in case of accidental connection of the I_{SET} pin directly to a negative potential.

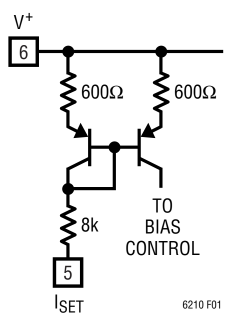


Figure 1. Internal Bias Setting Circuitry

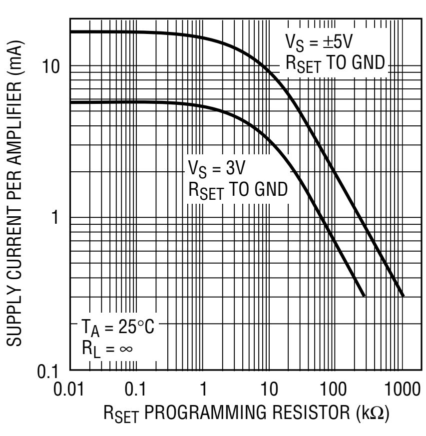


Figure 2. Setting R_{SET} to Control I_S

Input Considerations

The inputs of the LT6210/LT6211 are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than the absolute maximum ratings of ±10mA. In normal operation, the differential voltage between the inputs is small, so the ±1.4V limit is generally not an issue. ESD diodes protect both inputs, so although the part is not guaranteed to function outside the common mode range, input voltages that exceed a diode beyond either supply will also require current limiting to keep the input current below the absolute maximum of ±10mA.

Feedback Resistor Selection

The small-signal bandwidth of the LT6210/LT6211 is set by the external feedback resistors and the internal junction capacitances. As a result, the bandwidth is a function of the quiescent supply current, the supply voltage, the value of the feedback resistor, the closed-loop gain and the load resistor. Refer to the Typical AC Performance table for more information.

Layout and Passive Components

As with all high speed amplifiers, the LT6210/LT6211 require some attention to board layout. Low ESL/ESR bypass capacitors should be placed directly at the positive and negative supply (0.1μF ceramics are recommended). For best transient performance, additional 4.7μF tantalums should be added. A ground plane is recommended and trace lengths should be minimized, especially on the inverting input lead.

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Capacitance on the inverting input will cause peaking in the frequency response and overshoot in the transient response. Take care to minimize the stray capacitance at the inverting input to ground and between the output and the inverting input. If significant capacitance is unavoidable in a given application, an inverting gain configuration should be considered. When configured inverting, the amplifier inputs do not slew and the effect of parasitics is greatly reduced.

APPLICATIONS INFORMATION

Capacitive Loads

The LT6210/LT6211 are stable with any capacitive load. Although peaking and overshoot may result in the AC transient response, the amplifier's compensation decreases bandwidth with increasing output capacitive load to ensure stability. To maintain a response with minimal peaking, the feedback resistor can be increased at the cost of bandwidth as shown in the Typical Performance Characteristics. Alternatively, a small resistor (5Ω to 35Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present. The disadvantage of this technique is that the gain is a function of the load resistance.

Power Supplies

The LT6210/LT6211 will operate on single supplies from 3V to 12V and on split supplies from ±1.5V to ±6V. If split supplies of unequal absolute value are used, input offset voltage and inverting input current will shift from the values specified in the Electrical Characteristics table. Input offset voltage will shift 2mV and inverting input current will shift 0.5µA for each volt of supply mismatch.

Slew Rate

Unlike a traditional voltage feedback op amp, the slew rate of a current feedback amplifier is not independent of the amplifier gain configuration. In a current feedback amplifier, both the input stage and the output stage have slew rate limitations. In the inverting mode, and for gains of 2 or more in the noninverting mode, the signal amplitude between the input pins is small and the overall slew rate is that of the output stage. For gains less than 2 in the noninverting mode, the overall slew rate is limited by the input stage. The input slew rate of the LT6210/LT6211 on ±5V supplies with an R_{SET} resistor of 20k (I_S = 6mA) is approximately 600V/µs and is set by internal currents and capacitances. The output slew rate is additionally constrained by the value of the feedback resistor and internal capacitance. At a gain of 2 with 887Ω feedback and gain resistors, ±5V supplies and the same biasing as above, the output slew rate is typically 700V/µs. Larger feedback resistors, lower supply voltages and lower supply current levels will all reduce slew rate. Input slew rates significantly exceeding the output slew capability can actually decrease slew performance in a positive gain configuration; the cleanest transient response will be obtained from input signals with slew rates slower than 1000V/µs.

Output Swing and Drive

The output stage of the LT6210/LT6211 consists of a pair of class-AB biased common emitters that enable the output to swing rail-to-rail. Since the amplifiers can potentially deliver output currents well beyond the specified minimum short-circuit current, care should be taken not to short the output of the device indefinitely. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C if the output is used to drive low impedance loads. See Note 5 for details. Additionally, the output of the amplifier has reverse-biased ESD diodes connected to each supply. If the output is forced beyond either supply, large currents will flow through these diodes. If the current is limited to 80mA or less, no damage to the part will occur.

TYPICAL APPLICATION

3V Cable Driver with Active Termination

Driving back-terminated cables on single supplies usually results in very limited signal amplitude at the receiving end of the cable. However, positive feedback can be used to reduce the size of the series back termination resistor, thereby decreasing the attenuation between the series and shunt termination resistors while still maintaining controlled output impedance from the line-driving amplifier.

Figure 3 shows the LT6210 using this "active termination" scheme on a single 3V supply. The amplifier is AC-coupled and in an inverting gain configuration to maximize the input signal range. The gain from V_{IN} to the receiving end of the cable, V_{OUT}, is set to –1. The effective impedance looking into the amplifier circuit from the cable is 50Ω throughout the usable bandwidth.

TYPICAL APPLICATION

The response of the cable driver with a 1MHz sinusoid is shown in Figure 4. The circuit is capable of transmitting a $1.5V_{P-P}$ undistorted sinusoid to the 50Ω termination resistor and has a full signal $1V_{P-P}$ bandwidth of 50MHz. Small signal –3dB bandwidth extends from 1kHz to 56MHz with the selected coupling capacitors.

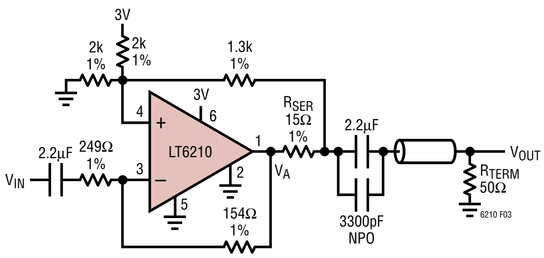


Figure 3. 3V Cable Driver with Active Termination

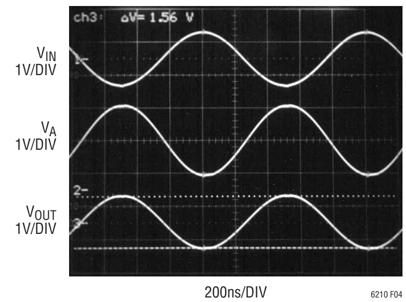
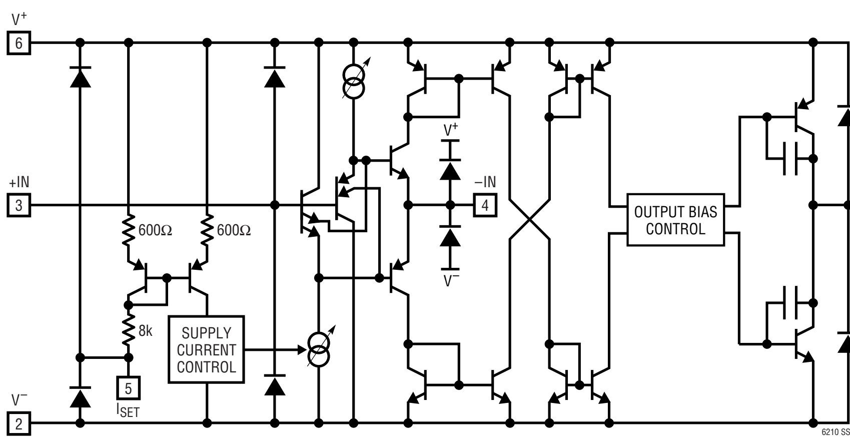


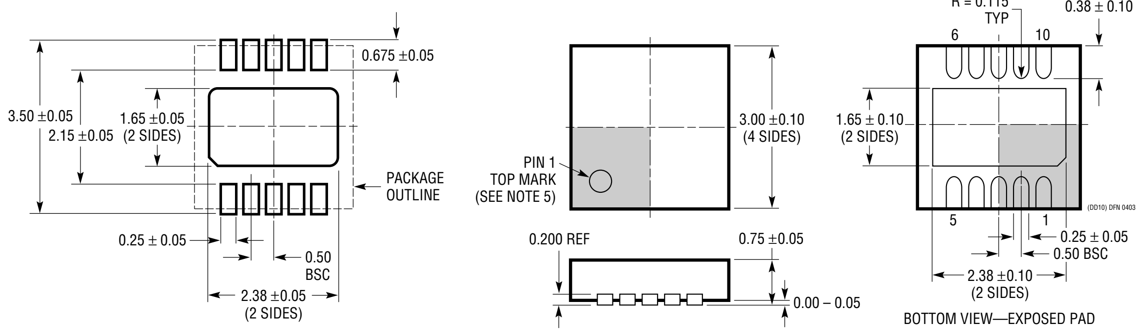
Figure 4. Response of Circuit at 1MHz

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)

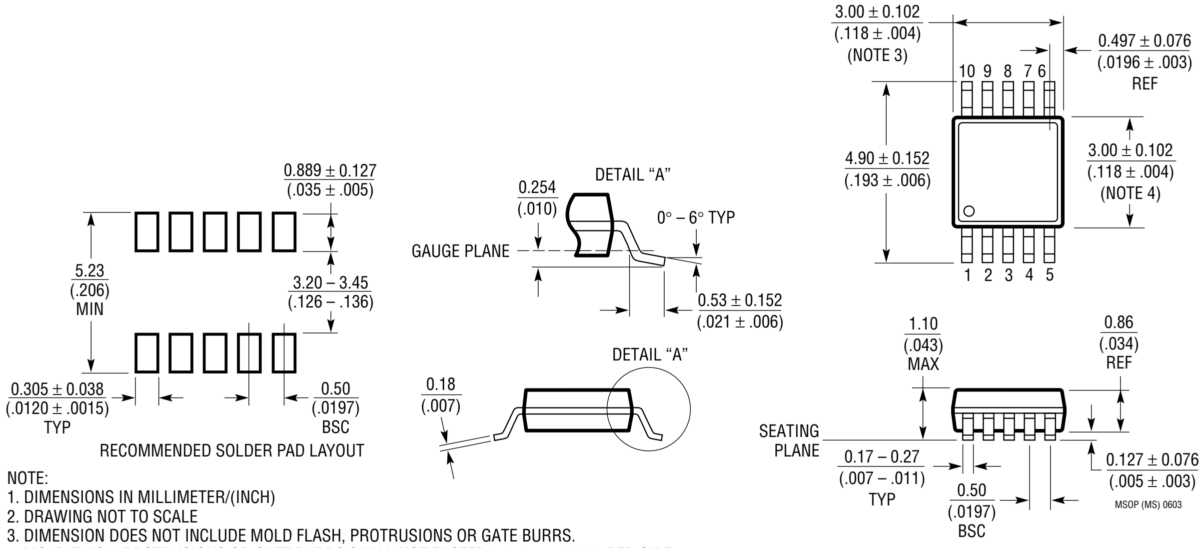


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

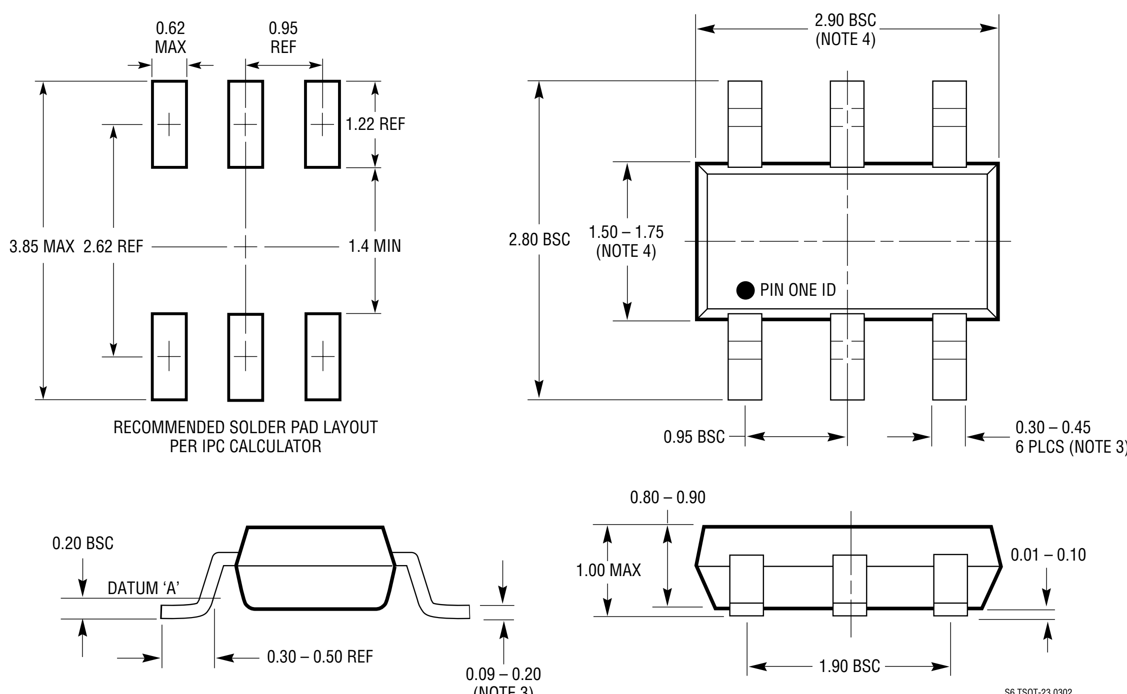
PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATIONS

Line Driver with Power Saving Mode

In applications where low distortion or high slew rate are desirable but not necessary at all times, it may be possible to decrease the LT6210 or LT6211's quiescent current when the higher power performance is not required. Figure 5 illustrates a method of setting quiescent current with a FET switch. In the 5V dual supply case pictured, shorting the I_{SET} pin through an effective 20k to ground sets the supply current to 6mA, while the 240k resistor at the I_{SET} pin with the FET turned off sets the supply current to approximately 1mA. The feedback resistor of 4.02k is selected to minimize peaking in low power mode. The bandwidth of the LT6210 in this circuit increases from about 40MHz in low power mode to over 200MHz in full speed mode, as illustrated in Figure 6. Other AC specs also improve significantly at the higher current setting. The following table shows harmonic distortion at 1MHz with a $2V_{P-P}$ sinusoid at the two selected current levels.

Harmonic Distortion

LOW POWER		FULL SPEED	
HD2	–53dBc	HD2	–68dBc
HD3	–46dBc	HD3	–77dBc

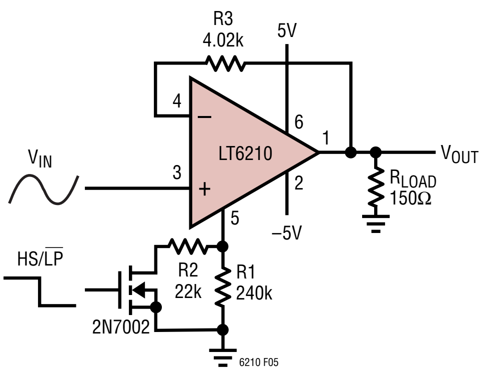


Figure 5. Line Driver with Low Power Mode

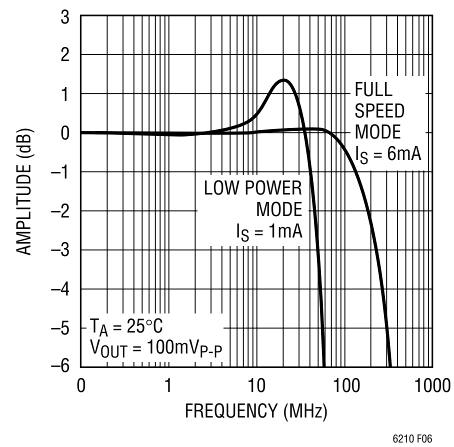


Figure 6. Frequency Response for Full Speed and Low Power Mode

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1252/LT1253/LT1254	100MHz Low Cost Video Amplifiers	Single, Dual and Quad Current Feedback Amplifiers
LT1395/LT1396/LT1397	400MHz, 800V/µs Amplifiers	Single, Dual and Quad Current Feedback Amplifiers
LT1398/LT1399	300MHz Amplifiers with Shutdown	Dual and Triple Current Feedback Amplifiers
LT1795	50MHz, 500mA Programmable I_S Amplifier	Dual Current Feedback Amplifier
LT1806/LT1807	325MHz, 140V/µs Rail-to-Rail I/O Amplifiers	Single and Dual Voltage Feedback Amplifiers
LT1815/LT1816/LT1817	220MHz, 1500V/µs Programmable I_S Operational Amplifier	Single, Dual and Quad Voltage Feedback Amplifiers

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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