Data Sheet No. PD94252

IRU3047

DUAL SYNCHRONOUS PWM CONTROLLER WITH CURRENT SHARING CIRCUITRY AND LDO CONTROLLER PRELIMINARY DATA SHEET

FEATURES

- Dual Synchronous Controller in 20-Pin Package with 180° out-of-phase operation
- LDO Controller with 40mA drive
- Can be configured as 2-Independent or 2-Phase **PWM Controller**
- Programmable Current Sharing in 2-Phase Configuration
- Flexible, Same or Separate Supply Operation
- Operation from 4V to 25V Input
- Internal 200KHz Oscillator per phase
- Soft-Start controls all outputs
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Short Circuit Protection for All Outputs
- Power Good Output

APPLICATIONS

- **Dual-Phase Power Supply**
- **DDR Memory Source Sink Vtt Application**
- Graphic Card

TYPICAL APPLICATION

DESCRIPTION

The IRU3047 IC combines a Dual synchronous Buck controller and a linear regulator controller, providing a cost-effective, high performance and flexible solution for multi-output applications. The Dual synchronous controller can be configured as 2-independent or 2-phase controller. In 2-phase configuration, the IRU3047 provides a programmable current sharing which is ideal when the output power exceeds any single input power budget. IRU3047 provides a separate adjustable output by driving a switch as a linear regulator. This device features an internal 200KHz oscillator, under-voltage lockout for all input supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

- Hard Disk Drive
- Power supplies requiring multiple outputs



Figure 1 - Typical application of IRU3047 configured as 2-phase converter.

PACKAGE ORDER INFORMATION

T _A (°C) DEVICE		PACKAGE		
0 To 70	IRU3047CW	20-Pin Plastic SOIC (W)		

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage	25V
VcH1, VcH2 and VcL Supply Voltage	30V (not i
Storage Temperature Range	-65°C To 1
Operating Junction Temperature Range	0°C To 12

PACKAGE INFORMATION



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, VcH1=VcH2=VcL=12V and Ta=0 to 70°C. Typical values refer to Ta=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage Section						
Fb Voltage	Vfb		1.225	1.250	1.275	V
Fb Voltage Line Regulation	Lreg	5 <vcc<12< td=""><td></td><td>0.2</td><td></td><td>%</td></vcc<12<>		0.2		%
UVLO Section						
UVLO Threshold - Vcc	UVLOVcc	Supply Ramping Up		4.2		V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - VccLDO	UVLOVccLDO	Supply Ramping Up		4.2		V
UVLO Hysteresis - VccLDO				0.25		V
UVLO Threshold - VcH1	UVLOVcH1	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH1				0.2		V
UVLO Threshold - VcH2	UVLOVcH2	Supply Ramping Up		3.5		V
UVLO Hysteresis - VcH2				0.2		V
UVLO Threshold - Fb	UVLOFb	Fb Ramping Down		0.6		V
UVLO Hysteresis - Fb				0.1		V
Supply Current Section						
Vcc Dynamic Supply Current	Dyn Icc	Freq=200KHz, C⊾=1500pF		5		mA
VcH1 Dynamic Supply Current	Dyn lcH1	Freq=200KHz, C⊾=1500pF		7		mA
VcH2 Dynamic Supply Current	Dyn lcH2	Freq=200KHz, C⊾=1500pF		7		mA
Vcc Static Supply Current	lccq	SS=0V		3.5		mA
VcH1 Static Supply Current	lcH1Q	SS=0V		2		mA
VcH2 Static Supply Current	lcH2Q	SS=0V		2		mA

25V
30V (not rated for inductive load)
-65°C To 150°C
0°C To 125°C

PARAMETER	SYM	TEST CONDITION	MIN	ТҮР	ΜΔΧ	UNITS
Soft-Start Section	01111			• • •	max	
Charge Current	89.m	SS-0V	15	25	30	^
Power Good Section		33-00	15	20	30	μΛ
Eh1 Lower Trip Point	PG	Eh1 Ramping Down				V
Eb1 Uppor Trip Point		Eb1 Ramping Up				V
Eb2 Lower Trip Point	PGrba	Eb2 Ramping Down				V
Eh2 Llonor Trip Point		Fb2 Ramping Up				V
Eb3 Lower Trip Point		Fb3 Ramping Down				V
Eh3 Lloper Trip Point		Fb3 Ramping Up				V
Power Good Voltage OK	VPC	5K resistor pulled up to 5V	45	1.1VREF	5	V
Frror Amp Section	VFG		7.0	4.0	0	v
Fb Voltage Input Bias Current	FB1	SS=3V		-0.1		μA
Fb Voltage Input Bias Current	FB2	SS=0V		-64		μA
Transconductance 1	G m1			400		μmho
Transconductance 2	g m2			600		μmho
Input Offset Voltage for PWM2	VOS(ERR)2	Fb2 to VP2	-2	0	+2	mV
Oscillator Section						
Frequency	Freq	Rt=Open	180	200	220	KHz
Ramp Amplitude	VRAMP			1.25		V
Output Drivers Section						
Rise Time	Tr	C∟=1500pF		35	100	ns
Fall Time	Tf	CL=1500pF		50	100	ns
Dead Band Time	Тов		50	150	250	ns
Max Duty Cycle	Τον	Fb=1V, Freq=200KHz	85	90		%
Min Duty Cycle	TOFF	Fb=1.5V	0	0		%
LDO Controller Section						
Drive Current	LDO		30	45		mA
Fb Voltage	VFBLDO		1.225	1.25	1.275	V
Input Bias Current	LDO(BIAS)			0.5	2	μA

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Vref	Reference Voltage.
2	Vp2	Non-inverting input to the second error amplifier, in the current sharing mode it is con-
		nected to the programming resistor. In independent two channel mode it is connected to
		the reference voltage (Pin1) when Fb2 is connected to the resistor divider to set the
		output voltage.
3,18	Fb2, Fb1	Inverting inputs to the error amplifiers, in current sharing mode Fb1 is connected to a
		resistor divider to set the output voltage and Fb2 is connected to programming resistor to
		achieve current sharing. In independent two channel mode, these pins work as feedback
		inputs for each channel.
4	Vcc	Supply voltage for the internal blocks of the IC.
5,6	Comp1, Comp2	Compensation pins for the error amplifiers.
7,14	VcH2, VcH1	Supply voltage for the high side output drivers. These are connected to voltages that
		must be at least 4V higher than their bus voltages (assuming 5V threshold MOSFET). A
		minimum of 1μ F high frequency capacitor must be connected from these pins to PGnd
		pin to provide peak drive current capability.
8,13	HDrv2, HDrv1	Output driver for high side power MOSFET. Connect a diode, such as BAT54 or 1N4148,
		from these pins to ground for the application when the inductor current goes negative
		(Source/Sink), soft-start at no load and for fast load transient from full load to no load.

PIN#	PIN SYMBOL	PIN DESCRIPTION
9,12	LDrv2, LDrv1	Output driver for the synchronous power MOSFET.
10	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to
		the system's ground plane.
11	Vcl	Supply voltage for the low side output drivers.
15	Vоитз	Driver signal for the LDO's external transistor.
16	Fb3	LDO's feedback pin, connected to a resistor divider to set the output voltage of LDO.
17	SS	Soft-Start pin. The converter can be shutdown by pulling this pin below 0.5V.
19	PGood	Power Good pin. This pin is a collector output that switches Low when any of the outputs
		are outside of the specified under voltage trip point.
20	Gnd	Ground pin.

BLOCK DIAGRAM





THEORY OF OPERATION

Introduction

The IRU3047 is designed for multi-outputs applications. It includes two synchronous buck controllers and a linear regulator controller. The two synchronous controller operates with fixed frequency voltage mode and can be configured as two independent controller or 2-phase controller with current sharing. The timing of the IC is provided through an internal oscillator circuit. These are two out of phase oscillators with 200KHz switching frequency.

Independent Mode

In this mode the IRU3047 provides two independent outputs with either common or different input voltages. The output voltage of the individual channel is set and controlled by the output of the error amplifier, this is the amplified error signal from the sensed output voltage and the reference voltage. This voltage is compared to the ramp signal and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

Current Sharing Mode

In the current sharing mode, the two converter's outputs tied together and provide one single output (see Figure 1). In this mode, one control loop acts as a master and sets the output voltage as a regular Voltage Mode buck controller and the other control loop acts as a slave and monitors the current information for current sharing. The current sharing is programmable and sets by using two external resistors in output currents' path. The slave's error amplifier, error amplifier 2 (see the block diagram) measures the voltage drops across the current sense resistors, the differential of these signals is amplified and compared with the ramp signal and generate the fixed frequency pulses of variable duty cycle to match the output currents.

Out of Phase Operation

The IRU3047 drives its two output stages 180° out of phase. In 2-phase configuration, the two inductor ripple currents cancel each other and result to a reduction of the output current ripple and contributes to a smaller output capacitors for the same ripple voltage requirement.

In application with single input voltage, the 2-phase configuration reduces the input ripple current. This results in much smaller RMS current in the input capacitor and reduction of input capacitor.

Soft-Start

The IRU3047 has a programmable soft start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vcc, VcH1 and VcH2 rise above their threshold and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.5V. This can be easily done by using an external small signal transistor. During shutdown the MOSFET drivers and the LDO controller turn off.

Power Good

The IRU3047 provides a power good signal. This is an open collector output and it is pulled low if the output voltages are not within the specified threshold. This pin can be left floating if not used.

Short-Circuit Protection

The outputs are protected against the short circuit. The IRU3047 protects the circuit for shorted output by sensing the output voltages. The IRU3047 shuts down the PWM signals and LDO controller, when the output voltages drops below the set values.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs and LDO controller remain in the off state whenever the supply voltages drop below set parameters. Normal operation resumes once the supply voltages rise above the set values.

APPLICATION INFORMATION

Design Example:

The following example is a typical application for IRU3047 in current sharing mode. The schematic is Figure 12 on page 16.

 $\begin{array}{l} \mathsf{V}_{\mathsf{IN1}(\mathsf{MASTER})} = 12\mathsf{V}\\ \mathsf{V}_{\mathsf{IN2}(\mathsf{SLAVE})} = 5\mathsf{V}\\ \mathsf{V}_{\mathsf{OUT1}} = 1.5\mathsf{V}\\ \mathsf{Iout} = 12\mathsf{A}\\ \Delta\mathsf{V}_{\mathsf{OUT}} = 75\mathsf{mV}\\ \mathsf{fs} = 200\mathsf{KHz} \end{array}$

PWM Section

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb1 pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the Fb1 pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT1} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

When an external resistor divider is connected to the output as shown in Figure 3.



Figure 3 - Typical application of the IRU3047 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_{6} = R_{5} \times \left(\frac{V_{OUT1}}{V_{REF}} - 1\right)$$

$$Will result to:$$

$$V_{OUT1} = 2.5V$$

$$V_{REF} = 1.25V$$

$$R_{5} = 1K$$

$$R_{6} = 1K$$

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

 $t_{\text{START}} = 75 \times Css$ (ms) ---(2) Where: Css is the soft-start capacitor (μ F)

For a start-up time of 75ms, the soft-start capacitor will be 1μ F. Choose a ceramic capacitor at 1μ F.

Boost Supply Vc

To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 1. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μ F to 1μ F is generally adequate for most applications.

Sense Resistor Selection

These resistors will determine the current sharing between two channels. The relationship between the Master and Slave output currents is expressed by:

RSEN1 × IMASTER = RSEN2 × ISLAVE ----(3)

For an equal current sharing, RSEN1=RSEN1 Choose RSEN1=RSEN2=5m Ω

Input Capacitor selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT} \sqrt{D \times (1-D)} ---(4)$$

Where:

D is the Duty Cycle, simply $D=V_{OUT}/V_{IN}$. IRMS is the RMS value of the input capacitor current. IOUT is the output current for each channel.

For VIN1=12V, lout1=6A and D1=0.208 Results to: IRMS1=2.43A

And for V_{IN2}=5V, lout_2=6A and D2=0.5 Results to: l_{RMS2} =3A

For higher efficiency, a low ESR capacitor is recommended.

For V_{IN1}=12V, choose two Poscap from Sanyo 16TPB47M (16V, 47μ F, $70m\Omega$, 1.4A)

For V_IN2=5V, choose two 6TPB330M (6.3V, 330 μ F, 40m $\Omega,$ 3A).

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$\mathsf{ESR} \leq \frac{\Delta \mathsf{Vo}}{\Delta \mathsf{lo}}$$
 ---(5)

Where: $\Delta V_0 = Output Voltage Ripple$ $\Delta I_0 = Output Current$ $\Delta V_0=100mV$ and $\Delta I_0=5A$, results to ESR=20m Ω

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPB470M 470 μ F, 6.3V has an ESR 40m Ω . Selecting two of these capacitors in parallel, results to an ESR of $\cong 20m\Omega$ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

The resulting output ripple current is smaller then each channel ripple current due to the 180° phase shift. These currents cancel each other. The cancellation is not the maximum because of the different duty cycle for each channel.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δ i); the optimum point is usually found between 20% and 50% ripple of the output current. For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} ; \Delta t = D \times \frac{1}{f_{S}} ; D = \frac{V_{OUT}}{V_{IN}}$$
$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_{S}} \qquad ---(6)$$

Where: $V_{IN} = Maximum Input Voltage$ $V_{OUT} = Output Voltage$ $\Delta i = Inductor Ripple Current$ $f_s = Switching Frequency$ $\Delta t = Turn On Time$ D = Duty Cycle

For $\Delta i_1=30\%$ of l_1 , we get $L_3=5.46\mu H$ For $\Delta i_2=30\%$ of l_2 , we get: $L_4=3.47\mu H$

The Coilcraft DO5022HC series provides a range of inductors in different values and low profile for large currents.

For L₃ choose DO5022P-602HC (6μ H, 7.5A) For L₄ choose DO5022P-472HC (4.7μ H, 8.4A)

Power MOSFET Selection

The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}) .

The gate drive requirement is almost the same for both MOSFETs. Caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

PCOND(Upper Switch) = $\hat{I}_{LOAD} \times R_{DS(ON)} \times D \times \vartheta$

 $P_{COND}(Lower Switch) = I_{LOAD} \times R_{DS(ON)} \times (1 - D) \times \vartheta$

 $\vartheta = R_{DS(ON)}$ Temperature Dependency

The total conduction loss is defined as:

 $P_{CON(TOTAL)}=P_{CON}(UpperSwitch)\vartheta+P_{CON}(LowerSwitch)\vartheta$

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7811A for control MOSFET and IRF7809A for synchronous MOSFET. These devices provide low on-resistance in a compact SOIC 8-Pin package.

The MOSFETs have the following data:

IRF7811A	IRF7809A				
VDSS = 28V	$V_{DSS} = 20V$				
l⊳ = 11.2A @ 90°C	l⊳ = 14.2A @ 90°C				
$R_{DS(ON)} = 12m\Omega$ @	$R_{DS(ON)} = 8.5 m\Omega$ @				
Vgs= 4.5V	$V_{GS} = 4.5V$				
For both: ϑ = 1.5 for 150°C					
(Junction	Temperature)				

The total conduction losses for the master channel is:

 $P_{CON(MASTER)} = 0.498W$

The total conduction losses for the slave channel is:

 $P_{CON(SLAVE)} = 0.5535W$

The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero-voltage condition, therefore the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$\mathsf{P}_{\mathsf{SW}} = \frac{\mathsf{V}_{\mathsf{DS}(\mathsf{OFF})}}{2} \times \frac{\mathsf{tr} + \mathsf{tf}}{\mathsf{T}} \times \mathsf{I}_{\mathsf{LOAD}} \qquad \qquad \text{---(7)}$$

Where:

 $V_{DS(OFF)}$ = Drain to Source Voltage at off time tr = Rise Time

tf = Fall Time

T = Switching Period

ILOAD = Load Current



Figure 4 - Switching time waveforms.

From IRF7811A data sheet we obtain:

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\frac{IRF7811A}{tr = 4ns}
tf = 8ns
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These values are taken under a certain condition test. For more detail please refer to the IRF7811A and IRF7809A data sheets.

By using equation (7), we can calculate the switching losses.

 $P_{SW(MASTER)} = 86.4mW$ $P_{SW(SLAVE)} = 36mW$

Feedback Compensation

The control scheme for master and slave channels is based on voltage mode control, but the compensation of these two feedback loops is slightly different.

The Master channel sets the output voltage and its feedback loop should take care of double pole introduced by the output filter as a regular voltage mode control loop. The goal is to provide a close loop transfer function with the highest 0dB crossing frequency and adequate phase margin. The slave feedback loop acts slightly different and its goal is using the current information for current sharing.

The master feedback loop sees the output filter. The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter expressed as follows:

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.



Figure 5 - Gain and phase of LC filter.

International

The master error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp1 pin to ground as shown in Figure 6.

The ESR zero of the LC filter expressed as follows:



Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / Vout) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad \text{---}(10)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(11)$$
$$F_z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(12)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

Fo1 > FESR and Fo1
$$\leq$$
 (1/5 ~ 1/10) \times fs

Use the following equation to calculate R4:

$$R_4 = \frac{V_{OSC}}{V_{IN(MASTER)}} \times \frac{F_{O1} \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \quad ---(13)$$

Where:

 $\begin{array}{l} \mathsf{V}_{\mathsf{IN}(\mathsf{MASTER})} = \mathsf{Maximum \ Input \ Voltage} \\ \mathsf{V}_{\mathsf{OSC}} = \mathsf{Oscillator \ Ramp \ Voltage} \\ \mathsf{F}_{\mathsf{O1}} = \mathsf{Crossover \ Frequency \ for \ the \ master \ E/A} \\ \mathsf{F}_{\mathsf{ESR}} = \mathsf{Zero \ Frequency \ of \ the \ Output \ Capacitor} \\ \mathsf{F}_{\mathsf{LC}(\mathsf{MASTER})} = \mathsf{Resonant \ Frequency \ of \ Output \ Filter} \\ \mathsf{g}_{\mathsf{m}} = \mathsf{Error \ Amplifier \ Transconductance} \\ \mathsf{R}_{\mathsf{5}} \ \mathsf{and} \ \mathsf{R}_{\mathsf{6}} = \mathsf{Resistor \ Dividers \ for \ Output \ Voltage} \\ \end{array}$

For:

 $V_{IN(MASTER)} = 12V$ $V_{OSC} = 1.25V$ $F_{O1} = 15KHz$ $F_{ESR} = 8.4KHz$ $F_{LC(MASTER)} = 2.1KHz$ $R_5 = R_6 = 1K\Omega$ $g_m = 600\mu mho$

This results to R₄=9.8K Ω . Choose R₄=10K Ω

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$\begin{split} & \text{Fz} \cong 75\%\text{Flc(master)} \\ & \text{Fz} \cong 0.75 \times \frac{1}{2\pi\sqrt{\text{ Lo} \times \text{ Co}}} \qquad \qquad \text{---(14)} \\ & \text{For:} \\ & \text{Lo} = 6\mu\text{H} \\ & \text{Co} = 940\mu\text{F} \\ & \text{Fz} = 1.57\text{KHz} \\ & \text{R}_4 = 10\text{K}\Omega \end{split}$$

Using equations (12) and (14) to calculate C_{θ} , we get:

One more capacitor is sometimes added in parallel with C_9 and R_4 . This introduces one more pole which is mainly used to supress the switching noise. The additional pole is given by:

$$F_{P} = \frac{1}{2\pi \times R_{4} \times \frac{C_{9} \times C_{POLE}}{C_{9} + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor $C_{\mbox{POLE}:}$

$$\begin{split} C_{\text{POLE}} = & \frac{1}{\pi \times R_4 \times f_{\text{S}} - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_{\text{S}}} \\ \text{For F}_{\text{P}} << & \frac{f_{\text{S}}}{2} \end{split}$$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.



Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

 $g_m Z_f >> 1$ and $g_m Z_{IN} >> 1$ ---(15)

By replacing Z_{IN} and Z_{i} according to figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12} + C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_{O1} = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad ---(16)$$

Where:

 V_{IN} = Maximum Input Voltage V_{OSC} = Oscillator Ramp Voltage Lo = Output Inductor Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (15) regarding transconductance error amplifier.

1) Select the crossover frequency:

Fo < Fesr and Fo \leq (1/10 ~ 1/6) \times fs

- 2) Select R₇, so that R₇ >> $\frac{2}{g_m}$
- 3) Place first zero before LC's resonant frequency pole.

$$F_{Z1} \cong 75\% \ F_{LC}$$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_{7}}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

C₁₂ > 50pF If not, change R₇ selection.

5) Place R₇ in equation (16) and calculate C₁₀:

$$C_{10} \leq \ \frac{2\pi \, \times \, Lo \, \times \, F_{0} \, \times \, Co}{R_{7}} \times \, \frac{V_{OSC}}{V_{IN}}$$

Place second pole at ESR zero.
 FP2 = FESR

$$R_8 = \frac{1}{2\pi \times C10 \times F_{P2}}$$

Check if R₈ > $\frac{1}{g_m}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency. $F_{Z2} = F_{LC}$

$$\mathsf{R}_6 = \frac{1}{2\pi \times \mathsf{C10} \times \mathsf{F}_{\mathsf{Z2}}} - \mathsf{R}_8$$

8) Use equation (1) to calculate R₅:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to - 12dB). The phase margin should be greater than 45° for overall stability.

The slave error amplifier is a differential-input transconductance amplifier as well, the main goal for the slave feed back loop is to control the inductor current to match the masters inductor current as well provides highest bandwidth and adequate phase margin for overall stability.

The transfer function of power stage is expressed by:

$$G(s) = \frac{I_{L2}(s)}{Ve(s)} = \frac{V_{IN} - V_{OUT}}{sL_2 \times V_{OSC}} ---(17)$$
Where:

$$V_{IN} = Input \text{ Voltage}$$

$$V_{OUT} = Output \text{ Voltage}$$

$$L_2 = Output \text{ Inductor}$$

$$V_{OSC} = Oscillator \text{ Peak Voltage}$$

As shown the transfer function is a function of inductor current.

The transfer function for the compensation network is given by equation (18), when using a series RC circuit as shown in Figure 8.

$$D(s) = \frac{Ve(s)}{R_{s2} \times I_{L2}(s)} = \left(g_m \times \frac{R_{s1}}{R_{s2}}\right) \times \left(\frac{1 + sC_2R_2}{sC_2}\right) \quad ---(18)$$



Figure 8 - The PI compensation network for slave channel.

The loop gain function is:

$$\begin{aligned} H(s) = [G(s) \times D(s) \times R_{S2}] \\ H(s) = R_{S2} \times \left(g_m \times \frac{R_{S1}}{R_{S2}}\right) \times \left(\frac{1 + sR_2C_2}{sC_2}\right) \times \left(\frac{V_{IN} - V_{OUT}}{sL_2 \times V_{OSC}}\right) \end{aligned}$$

Select a zero crossover frequency (F_{02}) one-tenth of the switching frequency:

$$F_{02} = \frac{f_{S}}{10}$$
$$F_{02} = 20 \text{KHz}$$

$$H(Fo) = g_m \times R_{S1} \times R_2 \times \frac{V_{IN} - V_{OUT}}{2\pi \times Fo \times L_2 \times V_{OSC}} = 1 \quad ---(19)$$

From (19), R₂ can be express as:

$$R_{2} = \frac{1}{g_{m} \times R_{S1}} \times \frac{2\pi \times F_{O2} \times L_{2} \times V_{OSC}}{V_{IN(SLAVE)} - V_{OUT}} \qquad ---(20)$$

Set the zero of compensator to be half of $F_{LC(SLAVE)}$, the compensator capacitor, C₂, can be calculated as:

$$F_{LC(SLAVE)} = \frac{1}{2\pi \sqrt{L_2 \times C_{OUT}}}$$

$$F_Z = \frac{F_{LC(SLAVE)}}{2}$$

$$C_2 = \frac{1}{2\pi \times R_2 \times F_Z} \qquad ---(21)$$

Using equations (20) and (21) we get the following values for R_2 and $\mathsf{C}_2.$

 $R_2 = 123K$; Choose $R_2 = 130K$

 $C_2 = 1023 pF$; Choose $C_2 = 1000 pF$

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL APPLICATION

Dual Input: 5V and 12V to 1.5V @ 16A 3.3V to 2.5V @ 2A



Figure 9 - Typical application of IRU3047, configured as a 2-phase converter in current sharing mode.

TYPICAL APPLICATION

12V to 1.8V @ 8A 5V to 2.5V @ 8A 3.3V to 2.5V @ 2A



Figure 10 - Typical application for IRU3047 configured as two independent controllers.

TYPICAL APPLICATION



Figure 11 - Typical application for IRU3047 configured for DDR memory application.

DEMO-BOARD APPLICATION

Dual Input: 5V and 12V to 1.5V @ 12A



Figure 12 - Typical application for IRU3047 configured as 2-phase converter in current sharing mode.

DEMO-BOARD APPLICATION

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1, Q3	MOSFET	20V, 8.5mΩ, 14A	2	IRF7809A	IR	irf.com
Q2, Q4	MOSFET	28V, 12mΩ, 11A	2	IRF7811A	IR	
U1	Controller	Synchronous PWM	1	IRU3047	IR	
D1, D2	Diode	Fast Switching	2	BAT54S	IR	
D100 *	Diode	Fast Switching	1	BAT54A	IR	
				or 1N4148	Any	
L1, L2	Inductor	1μH, 3A	2	DS1608C-102	Coilcraft	coilcraft.com
L3	Inductor	6μH, 7.5A	1	D05022P-602HC	Coilcraft	
L4	Inductor	4.7μH, 8.4A	1	D05022P-472HC	Coilcraft	
C2,C3	Cap, Ceramic	0.1μF, Y5V, 25V	2	ECJ-3YB1E105K	Panasonic	maco.panasonic.co.jp
C4,21,23,24,	Cap, Ceramic	1μF, Y5V, 16V	6	ECJ-2VF1C105Z	Panasonic	
103,104						
C7	Cap, Ceramic	0.22μF, Y5V, 25V	1	ECJ-3YB1E225K	Panasonic	
C101	Cap, Ceramic	1000pF, X7R, 50V	1	ECJ-2VB1H102K	Panasonic	
C9,C10	Cap, Poscap	47μF, 16V	2	16TPB47M	Sanyo	sanyo.com/industrial
C11,C12	Cap, Poscap	330μF, 6.3V	2	6TPB330M	Sanyo	
C13,C14	Cap, Poscap	470pF, X7R, 50V	2	ECJ-2VC1H471J	Panasonic	maco.panasonic.co.jp
C17,C18	Cap, Poscap	470 μ F, 6V, 40m Ω	2	6TPB470M	Sanyo	sanyo.com/industrial
C20,C22	Cap, Tantulum	33μF, 16V	2	EC-T1CD336R	Panasonic	maco.panasonic.co.jp
C100	Cap, Ceramic	10000pF	1			
R1,R12	Resistor	1K, 1%	2			
R2,3,4,8	Resistor	2.15Ω	4			
R13,R14	Resistor	5mΩ, 1W, 1%	2	ERJ-M1WSF5MOU		
R15,R16	Resistor	4.7Ω	2			
R103	Resistor	10K	1			
R105	Resistor	130K	1			

* Use this diode for (source/sink, no load) applications when the inductor current goes negative and for the fast load transient from full output load to no load.



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SYMBOL	20-PIN			
	MIN	MAX		
Α	12.598	12.979		
В	1.018	1.524		
С	0.66	REF		
D	0.33	0.508		
E	7.40	7.60		
F	2.032	2.64		
G	0.10	0.30		
	0.229	0.32		
J	10.008	10.654		
К	0°	8°		
L	0.406	1.270		
R	0.63 0.89			
Т	2.337 2.642			

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG	PACKAGE	PIN	PARTS	PARTS	T & R
DESIG	DESCRIPTION	COUNT	PER TUBE	PER REEL	Orientation
W	SOIC, Wide Body	20	38	1000	Fig A



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