National Semiconductor

CLC431/432
Dual Wideband Monolithic Op Amp with Disable

General Description

The CLC431 and CLC432 current-feedback amplifiers provide wide bandwidths and high slew rates for applications where board density and power are key considerations. These amplifiers provide DC-coupled small signal bandwidths exceeding 92MHz while consuming only 7mA per channel. Operating from ±15V supplies, the CLC431/432's enhanced slew rate circuitry delivers large-signal bandwidths with output voltage swings up to $28V_{pp}$. A wide range of bandwidth-insensitive gains are made possible by virtue of the CLC431 and CLC432's current-feedback topology.

The large common-mode input range and fast settling time (70ns to 0.05%) make these amplifiers well suited for CCD & data telecommunication applications. The disable of the CLC431 can accommodate ECL or TTL logic levels or a wide range of user definable inputs. With its fast enable/disable time (0.2µs/1µs) and high channel isolation of 70dB at 10MHz, the CLC431 can easily be configured as a 2:1 MUX. Many high performance video applications requiring signal gain and/or switching will be satisfied with the CLC431/432 due to their very low differential gain and phase errors (less than 0.1% and 0.1°; A_V = +2V/V at 4.43MHz into 150Ω load).

Quick 8ns rise and fall times on 10V pulses allow the CLC431/432 to drive either twisted pair or coaxial transmission lines over long distances.

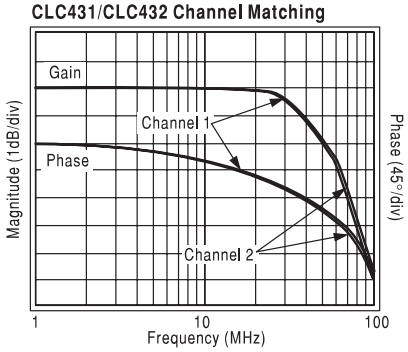
The CLC431/432's combination of low input voltage noise, wide common-mode input voltage range and large output voltage swings make them especially well suited for wide dynamic range signal processing applications.

Features

- Wide bandwidth: 92MHz (A_V=+1)
  62MHz (A_V=+2)
- Fast slew rate: 2000V/µs
- Fast disable: 1µs to high-Z output
- High channel isolation: 70dB at 10MHz
- Single or dual supplies: ±5V to ±16.5V

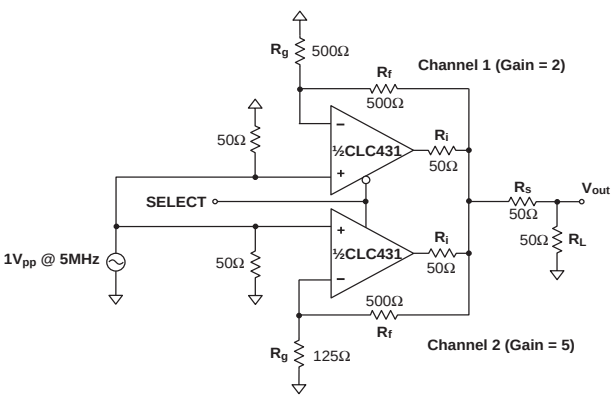
Applications

- Video signal multiplexing
- Twisted-pair differential driver
- CCD buffer & level shifting
- Discrete gain-select amplifier
- Transimpedance amplifier



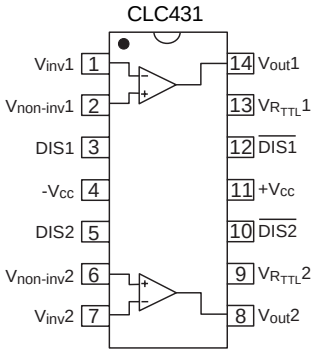
Typical Application

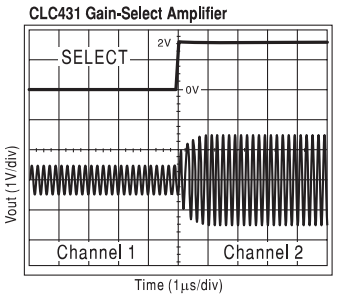
Discrete Gain Select Amplifier

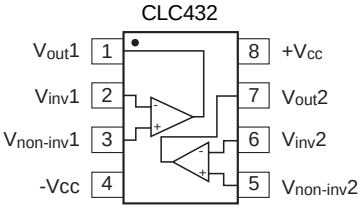


Pinout

PDIP & SOIC







CLC431/432 Electrical Characteristics (V_{CC} = ±15V; A_V = +2; R_f = R_g =750Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC431 & CLC432	+25	+25	0 to +70	-40 to +85	°C	1
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 4.0V_{pp}	62	42	37	36	MHz	
V_{CC} = ±5V	V_{out} < 4.0V_{pp}	62				MHz	
	V_{out} < 10V_{pp}	28	21	20	20	MHz	2
gain flatness	V_{out} < 4.0V_{pp}						
peaking	DC to 100MHz	0.05	0.5	0.7	0.7	dB	
rolloff	DC to 20MHz	0.0	0.8	0.8	0.8	dB	
linear phase deviation	DC to 30MHz	0.3	1.8	2.0	2.1	°	
differential gain	4.43MHz, R_L=150Ω	0.12	0.18	0.2	0.2	%	
differential phase	4.43MHz, R_L=150Ω	0.12	0.18	0.23	0.25	°	
TIME DOMAIN RESPONSE							
rise and fall time	10V step	8	12	13	13	ns	2
overshoot	2V step	5	10	12	12	%	
settling time	2V step to 0.05%	70	100	110	110	ns	
slew rate	V_{out} = ±10V	2000	1500	1450	1400	V/ms	2
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	- 65				dBc	6
3rd harmonic distortion	2V_{pp}, 1MHz	- 75				dBc	6
equivalent input noise							
voltage	>1MHz	3.3	4.2	4.4	4.5	nV/√Hz	
current, inverting	>1MHz	13	16	17	18	pA/√Hz	
current, non-inverting	>1MHz	2.0	2.5	2.6	2.8	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		3	6	7	7	mV	A
average drift		20	---	50	50	µV/°C	
bias current, non-inverting		2	8	10	16	µA	A
average drift		25	---	100	150	nA/°C	
bias current, inverting		2	6	6	8	µA	A
average drift		8	---	25	40	nA/°C	
power supply rejection ratio	DC	64	59	59	59	dB	
common-mode rejection ratio	DC	63	58	57	56	dB	
supply current	R_L= ∞, per channel	7.1	7.9	8.5	9.6	mA	A
CLC431 disabled	R_L= ∞, per channel	0.8	1.2	1.3	1.45	mA	A
MISCELLANEOUS PERFORMANCE							
input voltage range	common mode	± 12.2	± 12.0	± 11.8	± 11.6	V	
resistance	non-inverting	24	16	10	6	MΩ	
capacitance	non-inverting	0.5	1	1	1	pF	
output current		± 60	± 38	± 35	± 30	mA	
voltage range	R_L≥5kΩ	± 14.0	± 13.6	± 13.4	± 13.2	V	
	R_L=100Ω	± 6.0	± 3.7	± 3.7	± 2.9	V	
SWITCHING PERFORMANCE (CLC431)							
switching time	turn on	0.1	0.15	0.155	0.165	µs	
	turn off	0.7	1.0	1.2	1.2	µs	
DIS logic levels	single-ended mode						3
high input voltage (V_{IH})		> 2.0	> 2.0	> 2.0	> 2.0	V	
low input voltage (V_{IL})		< 0.8	< 0.8	< 0.8	< 0.8	V	
maximum current input	V_{IH} > DIS > V_{IL}	150	180	190	205	µA	
|DIS-$\overline{DIS}$|	differential mode						4
minimum differential voltage		0.3	0.4	0.4	0.4	V	
ISOLATION							
crosstalk, input referred	10MHz	70	64	64	64	dB	
off isolation	10MHz	64	60	60	60	dB	5

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

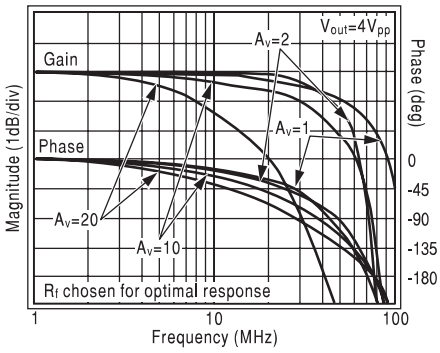
supply voltage	±16.5V
short circuit current	100mA
common-mode input voltage	±V_{cc}
differential input voltage	±10V
maximum junction temperature	+150°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C

Notes

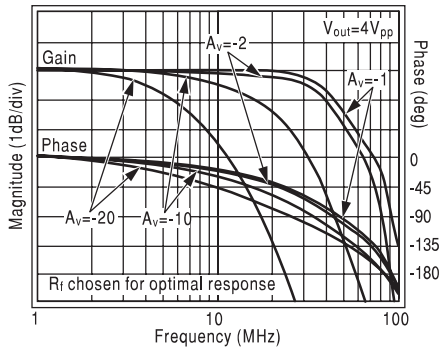
1) Tested and guaranteed with R_f = 866Ω. CLC432 tested and guaranteed with R_f = 750Ω.
2) Spec is guaranteed for R_L≥500Ω.
3) V_{RTTL} = 0, See text for single-ended mode of operation.
4) V_{RTTL} = NC, See text for differential mode of operation
5) Spec is guaranteed for AJE; AJP & AIB yield 7dB lower.
6) Spec is tested with 2V_{pp}, 10MHz and R_L = 100Ω.
A) J-level: spec is 100% tested at +25°C.

CLC431/432 Typical Performance Characteristics (T_A=+25°C, A_V=+2, V_{CC}=±15V, unless noted)

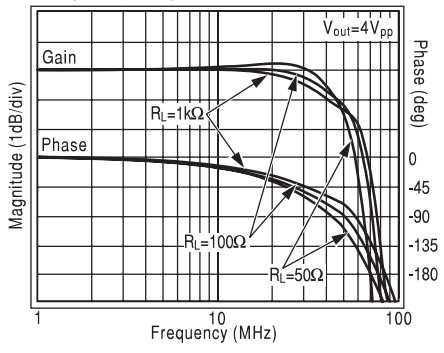
Non-Inverting Frequency Response



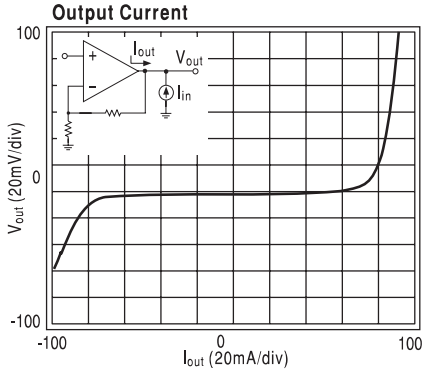
Inverting Frequency Response



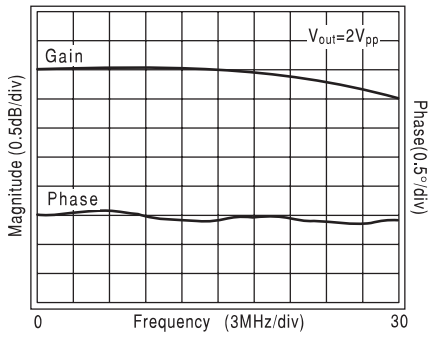
Frequency Response vs. Load Resistance



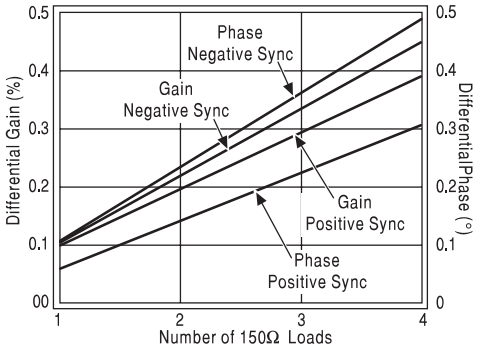
Output Current



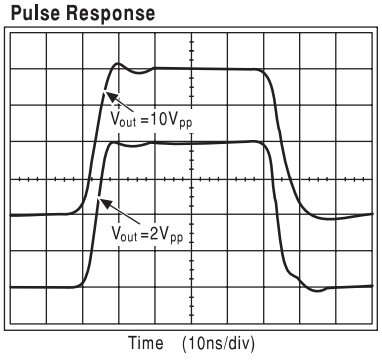
Gain Flatness & Linear Phase Deviation



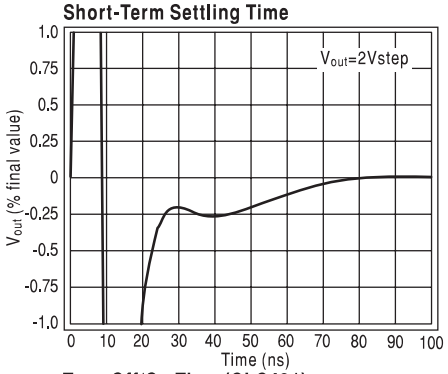
Differential Gain and Phase at 3.58MHz



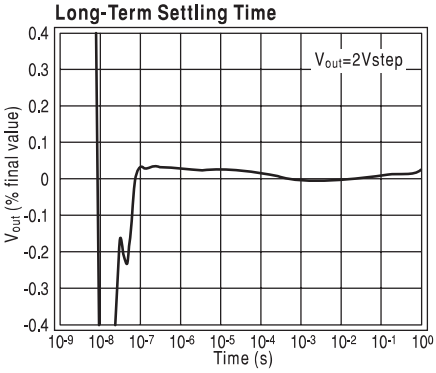
Pulse Response



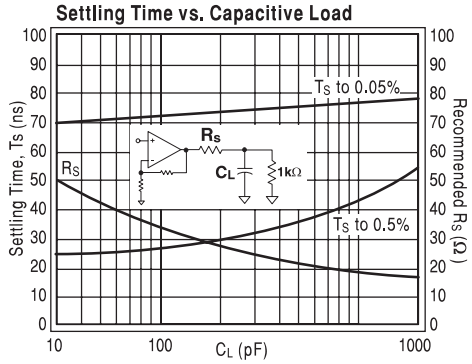
Short-Term Settling Time



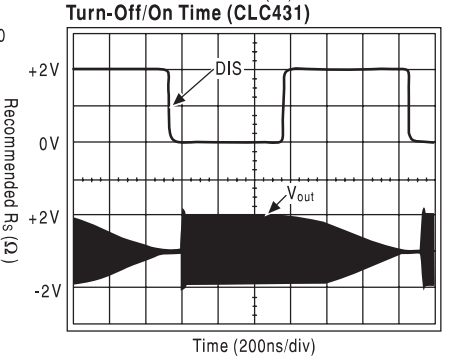
Long-Term Settling Time



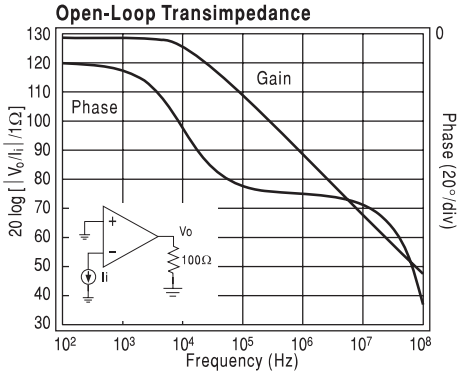
Settling Time vs. Capacitive Load



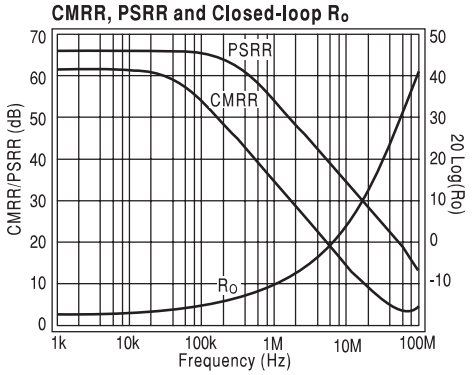
Turn-Off/On Time (CLC431)



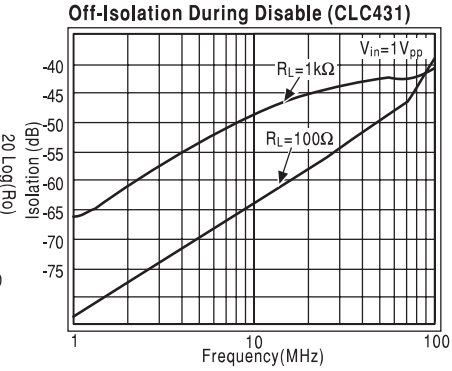
Open-Loop Transimpedance



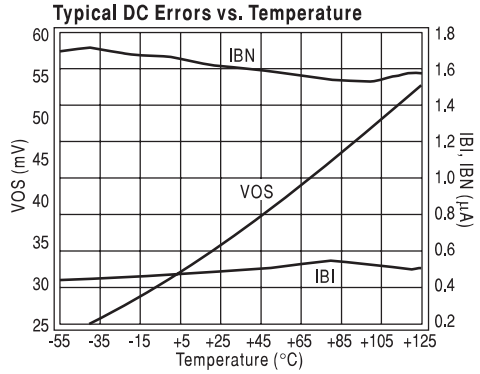
CMRR, PSRR and Closed-loop R_o



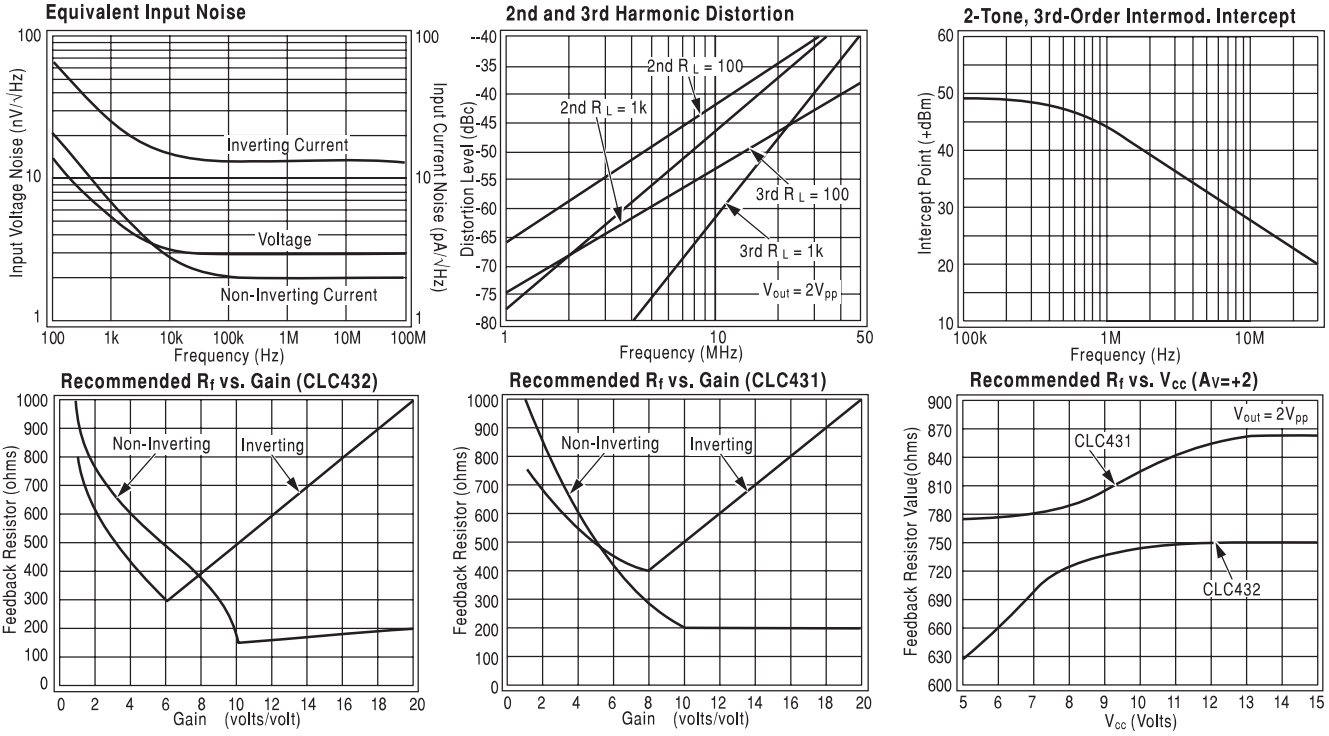
Off-Isolation During Disable (CLC431)



Typical DC Errors vs. Temperature



CLC431/432 Typical Performance Characteristics (T_A=+25°C, A_V=+2, V_{CC}=±15V, unless noted)



Application Discussion

Introduction

The CLC431 and the CLC432 are dual wideband current-feedback op amps that operate from single (+10V to +33V) or dual (±5V to ±16.5) power supplies. The CLC431 is equipped with a disable feature and is offered in 14-pin DIP and SOIC packages. The CLC432 is packaged in a standard 8-pin dual pinout and is offered in an 8-pin DIP and SOIC. Evaluation boards are available for each version of both devices. The evaluation boards can assist in the device and/or application evaluation and were used to generate the typical device performance plots on the preceding pages.

Each of the CLC431/CLC432's dual channels provide closely matched DC & AC electrical performance characteristics making them ideal choices for wideband signal processing. The CLC431, with its disable feature, can easily be configured as a 2:1 mux or several can be used to form a 10:1 mux without performance degradation. The two closely-matched channels of the CLC432 can be combined to form composite circuits for such applications as filter blocks, integrators, transimpedance amplifiers and differential line drivers and receivers.

Feedback Resistor Selection

The loop gain and frequency response for a current-feedback operational amplifier is determined largely by the feedback resistor (R_f). Package parasitics also influence ac response. Since the package parasitics of the CLC431 and the CLC432 are different, the optimum frequency and phase responses are obtained with different values of feedback resistor (for A_V=+2; CLC431: R_f=866Ω, CLC432: R_f=750Ω). The Electrical Characteristics and Typical Performance plots are valid for both devices under the specified conditions. Generally, lowering R_f from its recommended value will peak the frequency response and extend the bandwidth while increasing its value will roll off the response. Reducing the value of R_f too far below its recommended value will cause overshoot, ringing and eventually oscillation. For more information see Application Note OA-20 and OA-13.

In order to optimize the devices' frequency and phase response for gains other than +2V/V it is recommended to adjust the value of the feedback resistor. The two plots found in the Typical Performance section entitled "Recommended R_f vs. Gain" provide the means of selecting the feedback-resistor value that optimizes frequency and phase response over the CLC431/CLC432's gain range. Both plots show the value of R_f approaching a nonzero minimum at high non-inverting gains, which is characteristic of current-feedback op amps and yields best results. The linear portion of the two R_f vs. Inverting-gain curves results from the limitation placed on R_g (i.e. $R_g \geq 50\Omega$) in order to maintain an adequate input impedance for the inverting configuration. It should be noted that for stable operation a non-inverting gain of +1 requires an R_f equal to 1kΩ for both the CLC431 and the CLC432.

CLC431 Disable Feature

The CLC431 disable feature can be operated either single-endedly or differentially thereby accommodating a wide range of logic families. There are three pins associated with the disable feature of each of the CLC431's two amplifiers: DIS, $\overline{DIS}$ and V_{RTTL} (please see pinout on

front page). Also note that both amplifiers are guaranteed to be enabled if all three of these pins are unconnected.

Fig. 1 illustrates the single-ended mode of the CLC431's disable feature for logic families such as TTL and CMOS. In order to operate properly, V_{RTTL} must be grounded, thereby biasing $\overline{DIS}$ to approximately +1.4V through the two internal series diodes. For single-ended operation, $\overline{DIS}$ should be left floating. Applying a TTL or CMOS logic "high" (i.e. >2.0Volts) to DIS will switch the tail current of the differential pair to Q1 and "shut down" Q2 which results in the *disabling* of that channel of the CLC431. Alternatively, applying a logic "low" (i.e. <0.8Volts) to DIS will switch the tail current from Q1 to Q2 effectively *enabling* that channel. If DIS is left floating under single-ended operation, then the associated amplifier is guaranteed to be *disabled*.

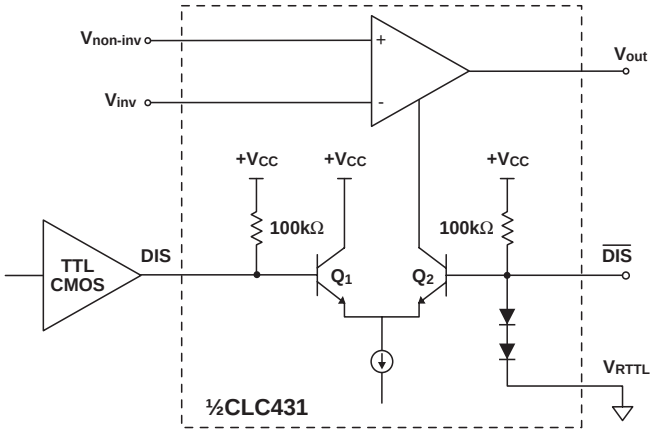


Fig. 1

The disable feature of the CLC431 is such that DIS and $\overline{DIS}$ have common-mode input voltage ranges of ($+V_{CC}$) to ($-V_{CC}$+3V) and are so guaranteed over the commercial temperature range. Internal clamps (not shown) protect the DIS input from excessive input voltages that could otherwise cause damage to the device. This condition occurs when enough source current flows into the node so as to allow DIS to rise to V_{CC}. This clamp is activated once DIS exceeds $\overline{DIS}$ by 1.5Volts and guarantees that V_{DIS} (ground referenced) does not exceed 4.7Volts.

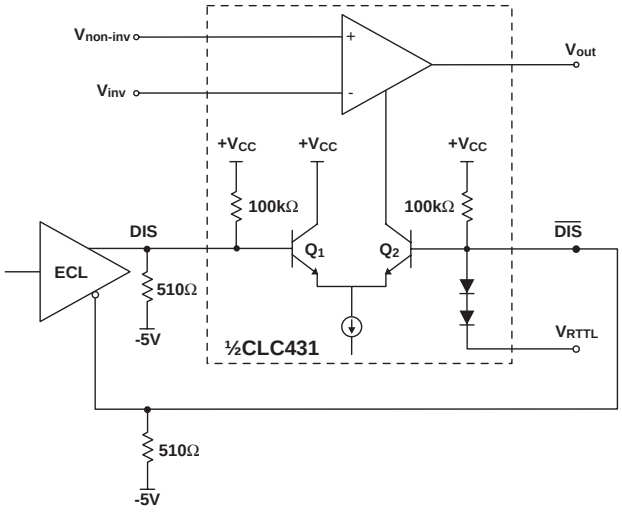


Fig. 2

Fig. 2 illustrates the differential mode of the CLC431's disable feature for ECL-type logic. In order for this mode to operate properly, V_{RTTL} must be left floating while DIS and $\overline{DIS}$ are to be connected directly to the ECL gate as illustrated. Applying a differential logic "high" (DIS - $\overline{DIS}$ ≥ 0.4Volts) switches the tail current of the differential pair from Q2 to Q1 and results in the *disabling* of that CLC431 channel. Alternatively, applying a differential logic "low" (DIS - $\overline{DIS}$ ≤ -0.4Volts) switches the tail current of the differential pair from Q1 to Q2 and results in the *enabling* of that same channel. The internal clamp, mentioned above, also protects against excessive differential voltages up to 30Volts while limiting input currents to <3mA.

DC Performance

A current-feedback amplifier's input stage does not have equal nor correlated bias currents, therefore they cannot be cancelled and each contributes to the total DC offset voltage at the output by the following equation:

$$V_{offset} = \pm \left(I_{bn} * R_s \left(1 + \frac{R_f}{R_g} \right) + V_{io} \left(1 + \frac{R_f}{R_g} \right) + I_{bi} * R_f \right)$$

The input resistor R_s is that resistance seen when looking from the non-inverting input back towards the source. For inverting DC-offset calculations, the source resistance seen by the input resistor R_g must be included in the output offset calculation as a part of the non-inverting gain equation. Application note OA-7 gives several circuits for DC offset correction.

Layout Considerations

It is recommended that the decoupling capacitors (0.1µF ceramic and 6.8µF electrolytic) should be placed as close as possible to the power supply pins to insure a proper high-frequency low impedance bypass. Careful attention to circuit board layout is also necessary for best performance. Of particular importance is the control of parasitic capacitances (to ground) at the output and invering input pins. See CLC431/432 Evaluation Board literature for more information.

Applications Circuits

2:1 Video Mux (CLC431)

Fig. 3 illustrates the connections necessary to configure the CLC431 as a 2:1 multiplexer in a 75Ω system. Each of the two CLC431's amplifiers is configured with a non-inverting gain of +2V/V using 634Ω feedback (R_f) and gain-setting (R_g) resistors. The feedback resistor value is lower than that recommended in order to compensate for the reduction of loop-gain that results from the inclusion of the 50Ω resistor (R_i) in the feedback loop. This 50Ω resistor serves to isolate the output of the active channel from the impedance of the inactive channel yet does not affect the low output impedance of the active channel. Notice that for proper operation V_{RTTL} 1 (pin 13) is grounded and V_{RTTL} 2 (pin 9) is unconnected. The pins associated with the disable feature are to be connected as follows: DIS1 and $\overline{DIS}$2 (pins 3 & 10) are connected together as well as DIS2 and $\overline{DIS}$1 (pins 5 & 12). Channel 1 is selected with the application of a logic "low" to SELECT while a logic "high" selects Channel 2.

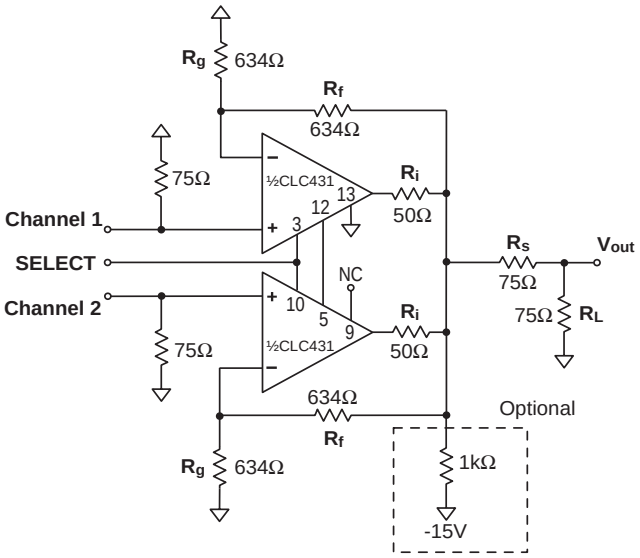


Fig. 3

The optional 1kΩ pull-down resistor connected from the output of the 2:1 mux to the negative power supply ($-V_{CC}$) results in improved differential gain and phase performance (0.02% and 0.01°) at PAL video levels.

Switched Gain Amplifier (CLC431)

As seen from the front page, the CLC431 can also be configured as a switched-gain amplifier that is similar to the 2:1 mux. Configuring each of the two CLC431's amplifiers with different non-inverting gains and tying the two inputs together (eliminating one of the input-terminating resistors) allows the CLC431 to switch an input signal between two different gains.

Inactive Channel Impedances (CLC431)

The impedance that is seen when looking into the output of a disabled CLC431 is typically represented as 1MΩ||16pF. The inverting input impedance becomes very high, essentially open. Therefore, the impedance presented by a disabled channel is $(R_f+R_g)||(R_i+(1M\Omega||16pF))$ as illustrated in Fig. 4. It should also be noted that any trace capacitance that is associated with the common output connection will add in parallel to that presented by the CLC431's inactive channel.

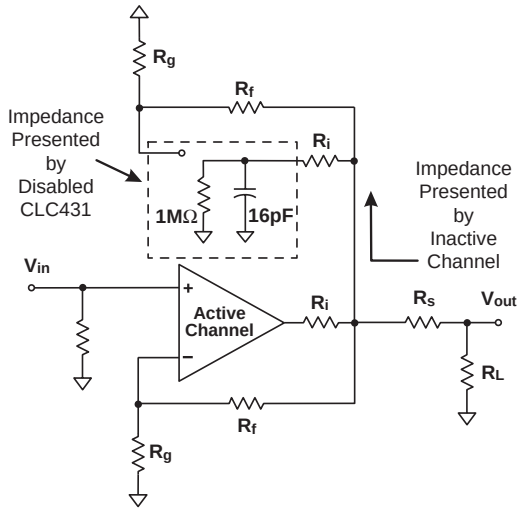


Fig. 4

Twisted-Pair Driver.

Twisted-pair cables are used in many applications such as telephony, video and data communications. The CLC432's two matched channels make it well suited for such applications and is illustrated in Fig. 5.

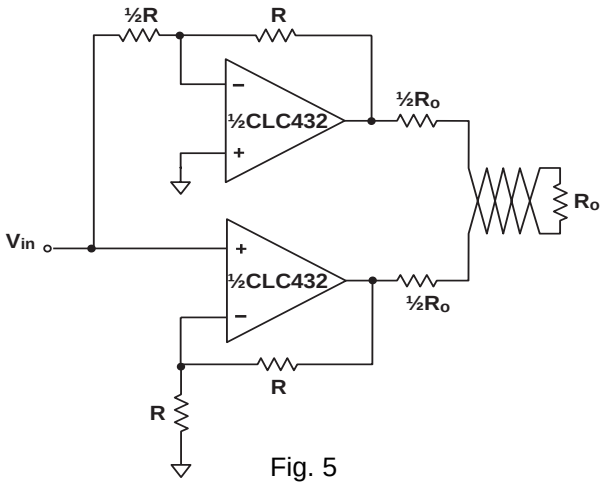
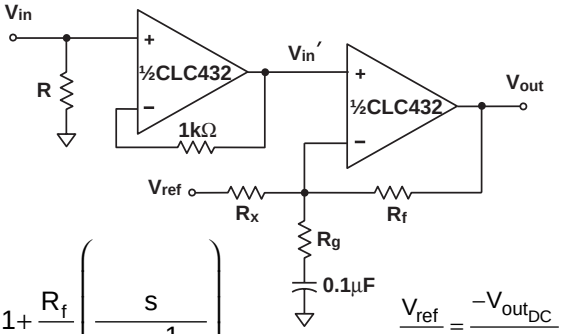


Fig. 5

CCD Amplifier.

The CLC432 can easily be configured as 10MSPS CCD amplifier with DC level shifting as illustrated in Fig 6. Notice that one of the CLC432's channels buffers the CCD output while the other channel is configured with both an inverting DC gain and an AC gain in order to achieve the overall transfer function shown in Fig. 6.



$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_g}\left(\frac{s}{s + \frac{1}{R_g C_g}}\right)$$

$$\frac{V_{ref}}{R_x} = \frac{-V_{out_{DC}}}{R_f}$$

$$R_x >> \frac{1}{2\pi f_{in} C_g}$$

for $R_x >> R_g$

Fig. 6

Ordering Information

Model	Temperature Range	Description
CLC431AJP	-40°C to +85°C	14-pin PDIP
CLC431AJE	-40°C to +85°C	14-pin SOIC
CLC431ALC	-40°C to +85°C	dice
CLC431A8B	-55°C to +125°C	14-pin CerDIP, MIL-STD-883
CLC431AMC	-55°C to +125°C	dice, MIL-STD-883
CLC432AJP	-40°C to +85°C	8-pin PDIP
CLC432AJE	-40°C to +85°C	8-pin SOIC
CLC432ALC	-40°C to +85°C	dice
CLC432A8B	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC432AMC	-55°C to +125°C	dice, MIL-STD-883

DESC SMD numbers: 5962-94725.

Reliability Information

Transistor count	37

Package Thermal Resistance

CLC431 Package	θ_{JC}	θ_{JA}
AJP	55°C	100°C
AJE	35°C	105°C
CERDIP	25°C	80°C
CLC432 Package		
AJP	55°C	110°C
AJE	40°C	115°C
CERDIP	25°C	115°C

Customer Design Applications Support

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1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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