



PRELIMINARY

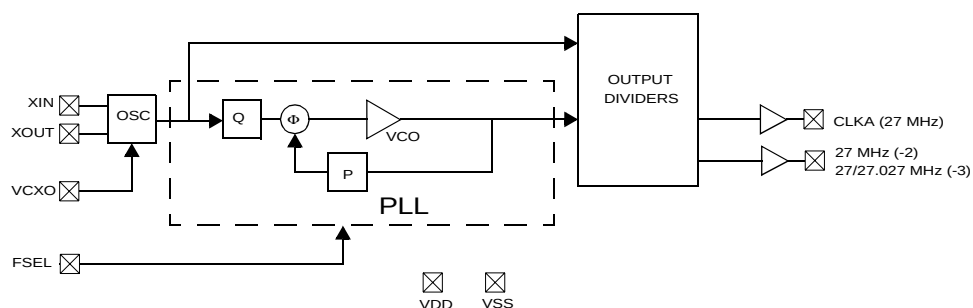
CY24212

MediaClock™ MPEG Clock Generator with VCXO

Features	Benefits
• Integrated phase-locked loop (PLL)	Highest-performance PLL tailored for multimedia applications
• Low jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• VCXO with analog adjust	Large ± 150 -ppm range, better linearity
• 3.3V operation	Enables application compatibility

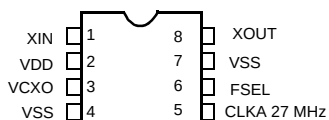
Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24212-1	1	13.5 MHz/27 MHz (selectable)	27 MHz
CY24212-2	2	13.5 MHz/27 MHz (selectable)	Two copies of 27 MHz
CY24212-3	2	27 MHz	27 MHz/27.027 MHz (-1 ppm)
CY24212-5	2	27 MHz	27 MHz/27.027 MHz (0 ppm)

Logic Block Diagram

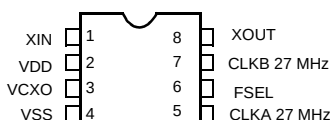


Pin Configurations

**CY24212-1
8-pin SOIC**



**CY24212-2
8-pin SOIC**



**CY24212-3,-5
8-pin SOIC**

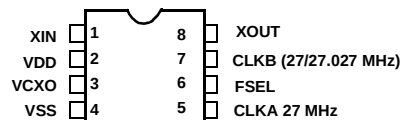


Table 1. CY24212 (-1, -2) Frequency Select Option

FSEL	Reference	CLKA/CLKB
0	13.5 MHz	27 MHz
1	27 MHz	27 MHz

Table 2. CY24212 (-3, -5) Frequency Select Option

FSEL	Reference	CLKA	CLKB
0	27 MHz	27 MHz	27 MHz
1	27 MHz	27 MHz	27.027 MHz

Pin Description

Name	Pin Number	Description
XIN	1	Reference Input.
VDD	2	Voltage Supply.
VCXO	3	Input Analog Control for VCXO.
VSS	4	Ground.
CLKA	5	27-MHz Clock Output.
FSEL (-1,-2)	6	Input Frequency Select, Weak Internal Pull-up. FSEL = 0, XIN = 13.5 MHz FSEL = 1, XIN = 27 MHz
FSEL (-3,-5)	6	Output Frequency Select, Weak Internal Pull-up. FSEL = 0, CLKA = 27 MHz, CLKB = 27 MHz FSEL = 1, CLKA = 27 MHz, CLKB = 27.027 MHz
VSS (-1)	7	Ground.
CLKB (-2)	7	27 MHz.
CLKB (-3,-5)	7	27 MHz/27.027 MHz.
XOUT ^[1]	8	Reference Output.

Pullable Crystal Specifications

Parameter	Name	Min	Typ	Max	Unit
CR _{load}	Crystal Load Capacitance		14		pF
C0/C1				240	
ESR	Equivalent Series Resistance		35	50	Ω
T ₀	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT _s	Stability over Temperature and Aging			± 50	ppm

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
T _S	Storage Temperature ^[2]	-65	125	°C
T _J	Junction Temperature		125	°C
	Digital Inputs	V _{SS} - 0.3	V _{DD} + 0.3	V
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0		70	°C
C _{LOAD}	Max. Load Capacitance			15	pF
f _{REF}	Reference Frequency	13.5		27	MHz

Notes:

1. Float XOUT if XIN is externally driven.
2. Rated for ten years.

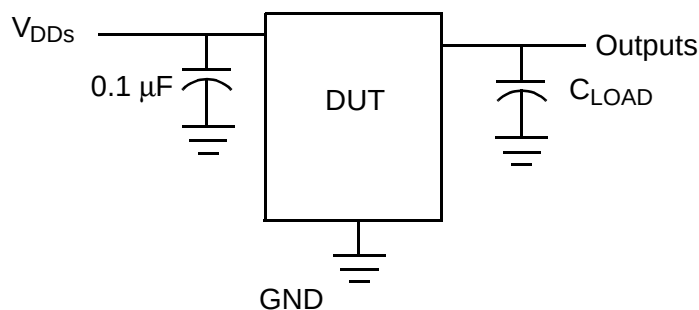
DC Electrical Specifications

Parameter	Name	Description	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD} = 3.3V$ (source)	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$ (sink)	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	–	5	10	μA
I_{IL}	Input Low Current	$V_{IL} = 0V$	–	–	50	μA
$f_{\Delta XO}$	VCXO Pullability Range		± 150			ppm
V_{VCXO}	VCXO Input Range		0		V_{DD}	V
I_{DD}	Supply Current	Sum of Core and Output Current			35	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	V_{DD}
R_{UP}	Pull-up resistor on inputs	$V_{DD} = 3.14$ to $3.47V$, measured $V_{IN} = 0V$		100	150	k Ω

AC Electrical Specifications ($V_{DD} = 3.3V$)

Parameter ^[3]	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 1</i> , 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15$ pF. See <i>Figure 2</i> .	0.8	1.4		V/ns
t_9	Clock Jitter	Peak-to-peak period jitter		300		ps
t_{10}	PLL Lock Time				3	ms

Test and Measurement Set-up



Note:

3. Not 100% tested.

Voltage and Timing Definitions

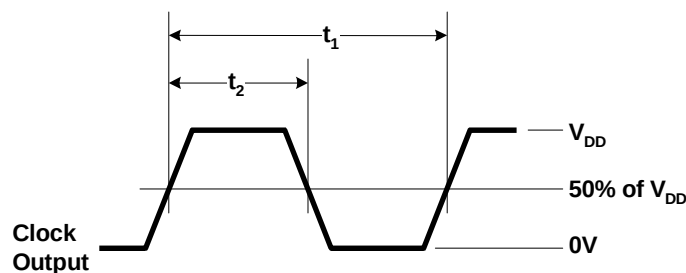


Figure 1. Duty Cycle Definition

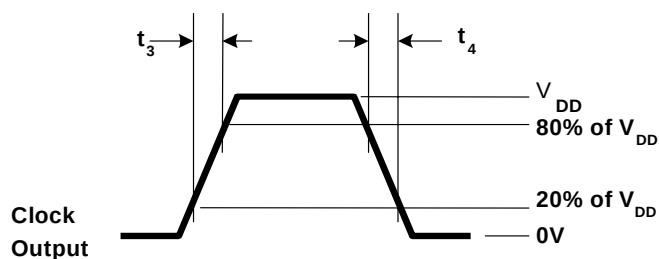
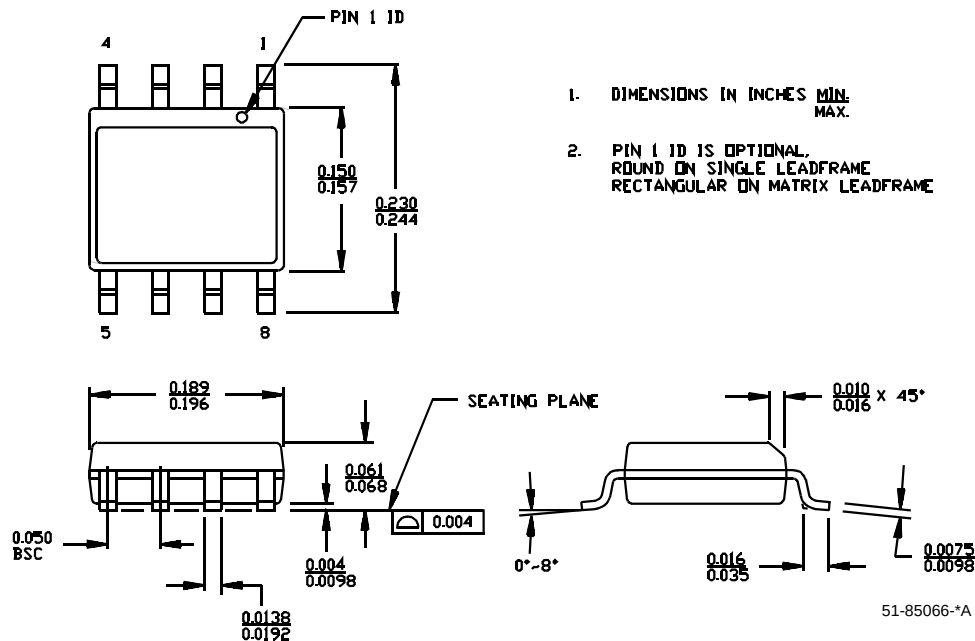


Figure 2. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24212SC-1	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-1T	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-2	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-2T	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-3	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-3T	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-5	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-5T	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V

Package Drawing and Dimensions
8-Lead (150-Mil) SOIC S8


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Document History Page

Document Title: CY24212 MediaClock™ MPEG Clock Generator with VCXO Document Number: 38-07402				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117089	09/09/02	CKN	New Data Sheet
*A	120888	12/06/02	CKN	Added -3
*B	123064	02/19/03	CKN	Added -5