NCP5316

Four/Five/Six-Phase Buck CPU Controller

The NCP5316 provides full−featured and flexible control for the latest high−performance CPUs. The IC can be programmed as a four−, five− or six−phase buck controller, and the per−phase switching frequency can be as high as 1.0 MHz. Combined with external gate drivers and power components, the controller implements a compact, highly integrated multi−phase buck converter.

Enhanced V^{2}™ control inherently compensates for variations in both line and load, and achieves current sharing between phases. This control scheme provides fast transient response, reducing the need for large banks of output capacitors and higher switching frequency.

The controller meets VR(M)10.x specifications with all the required functions and protection features.

Features

- Switching Regulator Controller
  - Programmable 4/5/6 Phase Operation
  - Lossless Current Sensing
  - Programmable Up to 1.0 MHz Switching Frequency Per Phase
  - 0 to 100% Adjustment of Duty Cycle
  - Programmable Adaptive Voltage Positioning Reduces Output Capacitor Requirements
  - Programmable Soft Start
- Current Sharing
  - Differential Current Sense Pins for Each Phase
  - Current Sharing Within 10% Between Phases
- Protection Features
  - Programmable Pulse−by−Pulse Current Limit for Each Phase
  - “111110” and “111111” DAC Code Fault
  - Latching Off Overvoltage Protection
  - Programmable Latch Overcurrent Protection
  - Undervoltage Lockout
  - Reference Undervoltage Lockout
  - MOSFET Driver Control through Driver−On Signal
- System Power Management
  - 6−Bit DAC with 0.5% Tolerance
  - Programmable Lower Power Good Threshold
  - Power Good Output
  - External Enable Control
  - 3.3 V Reference Voltage Output

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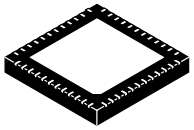
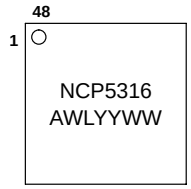
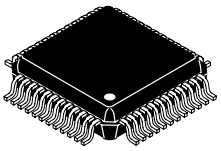
MARKING DIAGRAMS

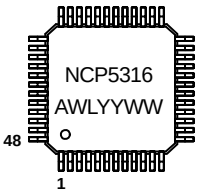


48−PIN QFN, 7 × 7
MN SUFFIX
CASE 485K
(Bottom View)





LQFP−48
FT SUFFIX
CASE 932



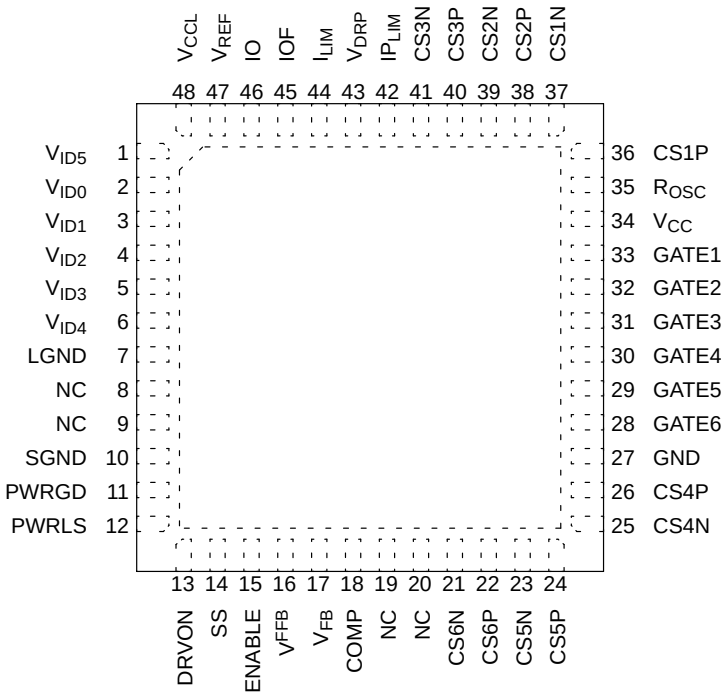
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

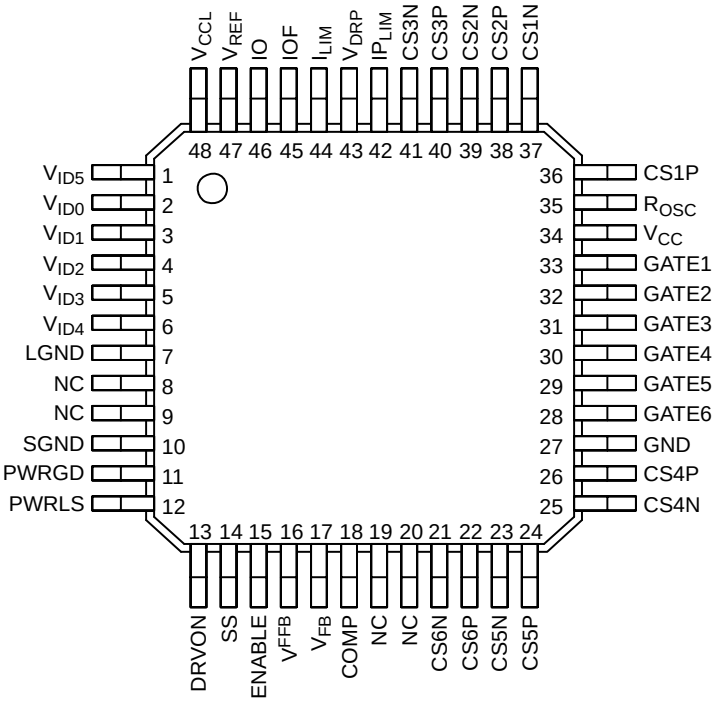
Device	Package	Shipping†
NCP5316MNR2	48−Pin QFN*	2000 Tape & Reel
NCP5316FTR2	LQFP−48*	2000 Tape & Reel

*7 × 7 mm

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



48−Pin QFN, Top View



LQFP−48

Figure 1. Pin Connections

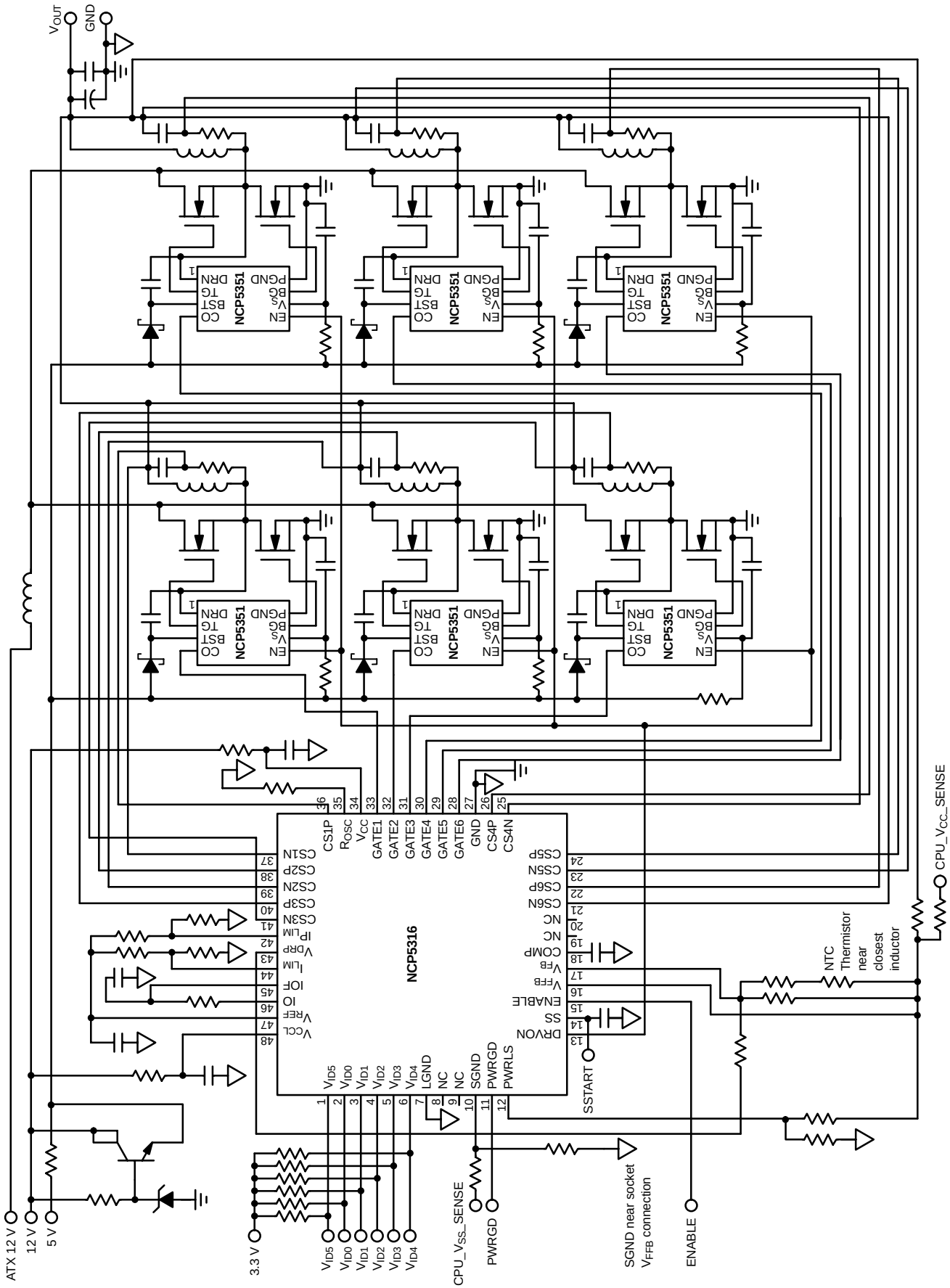


Figure 2. Application Diagram, 12 V to 0.8375 − 1.600 V Six−Phase Converter

MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature	150	°C
Lead Temperature Soldering, Reflow (Note 1)	230 peak	°C
Storage Temperature Range	−65 to 150	°C
ESD Susceptibility: Human Body Model (HBM)	2.0	kV
Moisture Sensitivity Level (MSL), LQFP	1	−
MSL, QFN	2	−
θ_{JA}, LQFP	52	°C/W
θ_{JA}, QFN, Pad Soldered to PCB	34	°C/W

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Number	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
15	ENABLE	18 V	−0.3 V	1.0 mA	1.0 mA
1−6	V_{ID0}−V_{ID5}	18 V	−0.3 V	1.0 mA	1.0 mA
7	LGND	−	−	50 mA	−
8	NC	NA	NA	NA	NA
9	NC	NA	NA	NA	NA
10	SGND	1.0 V	−1.0 V	1.0 mA	−
11	PWRGD	18 V	−0.3 V	1.0 mA	20 mA
12	PWRLS	7.0 V	−0.3 V	1.0 mA	1.0 mA
13	DRVON	7.0 V	−0.3 V	1.0 mA	1.0 mA
14	SS	7.0 V	−0.3 V	1.0 mA	1.0 mA
16	V_{FFB}	7.0 V	−0.3 V	1.0 mA	1.0 mA
17	V_{FB}	7.0 V	−0.3 V	1.0 mA	1.0 mA
18	COMP	7.0 V	−0.3 V	1.0 mA	1.0 mA
19	NC	NA	NA	NA	NA
20	NC	NA	NA	NA	NA
21	CS6N	18 V	−0.3 V	1.0 mA	1.0 mA
22	CS6P	18 V	−0.3 V	1.0 mA	1.0 mA
23	CS5N	18 V	−0.3 V	1.0 mA	1.0 mA
24	CS5P	18 V	−0.3 V	1.0 mA	1.0 mA
25	CS4N	18 V	−0.3 V	1.0 mA	1.0 mA
26	CS4P	18 V	−0.3 V	1.0 mA	1.0 mA
27	GND	−	−	0.4 A, 1.0 μs, 100 mA DC	−
28−33	GATE6−GATE1	18 V	−0.3 V	0.1 A, 1.0 μs, 25 mA DC	0.1 A, 1.0 μs, 25 mA DC
34	V_{CC}	18 V	−0.3 V	−	0.4 A, 1.0 μs, 100 mA DC
35	R_{OSC}	7.0 V	−0.3 V	1.0 mA	1.0 mA
36	CS1P	18 V	−0.3 V	1.0 mA	1.0 mA
37	CS1N	18 V	−0.3 V	1.0 mA	1.0 mA
38	CS2P	18 V	−0.3 V	1.0 mA	1.0 mA
39	CS2N	18 V	−0.3 V	1.0 mA	1.0 mA
40	CS3P	18 V	−0.3 V	1.0 mA	1.0 mA

MAXIMUM RATINGS (continued)

Pin Number	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
41	CS3N	18 V	−0.3 V	1.0 mA	1.0 mA
42	IP_{LIM}	7.0 V	−0.3 V	1.0 mA	1.0 mA
43	V_{DRP}	7.0 V	−0.3 V	1.0 mA	1.0 mA
44	I_{LIM}	7.0 V	−0.3 V	1.0 mA	1.0 mA
45	IOF	7.0 V	−0.3 V	1.0 mA	1.0 mA
46	IO	7.0 V	−0.3 V	5.0 mA	1.0 mA
47	V_{REF}	7.0 V	−0.3 V	5.0 mA	1.0 mA
48	V_{CCL}	18 V	−0.3 V	−	50 mA

VOLTAGE IDENTIFICATION (VID)

VID Pins (0 = low, 1 = high)						VID Code*(V)	−0.5%	V_{OUT} No Load† (V)	+0.5%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	V_{ID5}				
0	1	0	1	0	0	0.8375	0.8134	0.8175	0.8216
0	1	0	0	1	1	0.8500	0.8259	0.8300	0.8342
0	1	0	0	1	0	0.8625	0.8383	0.8425	0.8467
0	1	0	0	0	1	0.8750	0.8507	0.8550	0.8593
0	1	0	0	0	0	0.8875	0.8632	0.8675	0.8718
0	0	1	1	1	1	0.9000	0.8756	0.8800	0.8844
0	0	1	1	1	0	0.9125	0.8880	0.8925	0.8970
0	0	1	1	0	1	0.9250	0.9005	0.9050	0.9095
0	0	1	1	0	0	0.9375	0.9129	0.9175	0.9221
0	0	1	0	1	1	0.9500	0.9254	0.9300	0.9347
0	0	1	0	1	0	0.9625	0.9378	0.9425	0.9472
0	0	1	0	0	1	0.9750	0.9502	0.9550	0.9598
0	0	1	0	0	0	0.9875	0.9627	0.9675	0.9723
0	0	0	1	1	1	1.0000	0.9751	0.9800	0.9849
0	0	0	1	1	0	1.0125	0.9875	0.9925	0.9975
0	0	0	1	0	1	1.0250	1.0000	1.0050	1.0100
0	0	0	1	0	0	1.0375	1.0124	1.0175	1.0226
0	0	0	0	1	1	1.0500	1.0249	1.0300	1.0352
0	0	0	0	1	0	1.0625	1.0373	1.0425	1.0477
0	0	0	0	0	1	1.0750	1.0497	1.0550	1.0603
0	0	0	0	0	0	1.0875	1.0622	1.0675	1.0728
1	1	1	1	1	1	OFF			
1	1	1	1	1	0	OFF			
1	1	1	1	0	1	1.1000	1.0746	1.0800	1.0854
1	1	1	1	0	0	1.1125	1.0870	1.0925	1.0980
1	1	1	0	1	1	1.1250	1.0995	1.1050	1.1105
1	1	1	0	1	0	1.1375	1.1119	1.1175	1.1231
1	1	1	0	0	1	1.1500	1.1244	1.1300	1.1357

*VID Code is for reference only.
†V_{OUT} No Load is the input to the error amplifier.

VOLTAGE IDENTIFICATION (VID) (continued)

VID Pins (0 = low, 1 = high)						VID Code*(V)	−0.5%	V_{OUT} No Load† (V)	+0.5%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	V_{ID5}				
1	1	1	0	0	0	1.1625	1.1368	1.1425	1.1482
1	1	0	1	1	1	1.1750	1.1492	1.1550	1.1608
1	1	0	1	1	0	1.1875	1.1617	1.1675	1.1733
1	1	0	1	0	1	1.2000	1.1741	1.1800	1.1859
1	1	0	1	0	0	1.2125	1.1865	1.1925	1.1985
1	1	0	0	1	1	1.2250	1.1990	1.2050	1.2110
1	1	0	0	1	0	1.2375	1.2114	1.2175	1.2236
1	1	0	0	0	1	1.2500	1.2239	1.2300	1.2362
1	1	0	0	0	0	1.2625	1.2363	1.2425	1.2487
1	0	1	1	1	1	1.2750	1.2487	1.2550	1.2613
1	0	1	1	1	0	1.2875	1.2612	1.2675	1.2738
1	0	1	1	0	1	1.3000	1.2736	1.2800	1.2864
1	0	1	1	0	0	1.3125	1.2860	1.2925	1.2990
1	0	1	0	1	1	1.3250	1.2985	1.3050	1.3115
1	0	1	0	1	0	1.3375	1.3109	1.3175	1.3241
1	0	1	0	0	1	1.3500	1.3234	1.3300	1.3367
1	0	1	0	0	0	1.3625	1.3358	1.3425	1.3492
1	0	0	1	1	1	1.3750	1.3482	1.3550	1.3618
1	0	0	1	1	0	1.3875	1.3607	1.3675	1.3743
1	0	0	1	0	1	1.4000	1.3731	1.3800	1.3869
1	0	0	1	0	0	1.4125	1.3855	1.3925	1.3995
1	0	0	0	1	1	1.4250	1.3980	1.4050	1.4120
1	0	0	0	1	0	1.4375	1.4104	1.4175	1.4246
1	0	0	0	0	1	1.4500	1.4229	1.4300	1.4372
1	0	0	0	0	0	1.4625	1.4353	1.4425	1.4497
0	1	1	1	1	1	1.4750	1.4477	1.4550	1.4623
0	1	1	1	1	0	1.4875	1.4602	1.4675	1.4748
0	1	1	1	0	1	1.5000	1.4726	1.4800	1.4874
0	1	1	1	0	0	1.5125	1.4850	1.4925	1.5000
0	1	1	0	1	1	1.5250	1.4975	1.5050	1.5125
0	1	1	0	1	0	1.5375	1.5099	1.5175	1.5251
0	1	1	0	0	1	1.5500	1.5224	1.5300	1.5377
0	1	1	0	0	0	1.5625	1.5348	1.5425	1.5502
0	1	0	1	1	1	1.5750	1.5472	1.5550	1.5628
0	1	0	1	1	0	1.5875	1.5597	1.5675	1.5753
0	1	0	1	0	1	1.6000	1.5721	1.5800	1.5879

*VID Code is for reference only.
†V_{OUT} No Load is the input to the error amplifier.

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $V_{CCL} = V_{CC} = 12$ V; $C_{GATEx} = 100$ pF, $C_{COMP} = 0.01$ μF, $C_{SS} = 0.1$ μF, $C_{VCC} = 0.1$ μF, $R_{ROSC} = 32.4$ kΩ, $V(I_{LIM}) = 3.3$ V, $V(IP_{LIM}) = 3.3$ V, unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
VID Inputs					
Input Threshold	V_{ID5}, V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	400	–	800	mV
VID Pin Current	V_{ID5}, V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0} = 0 V	–	–	1.0	μA
SGND Bias Current	SGND < 300 mV, All DAC Codes	10	20	40	μA
SGND Voltage Compliance Range	–	−200	–	300	mV
Power Good					
Upper Threshold Offset from V_{OUT} No Load	–	85	100	115	mV
Lower Threshold Constant	PWRLS/V_{OUT} No Load	0.475	0.500	0.525	V/V
Output Low Voltage	I_{PWRGD} = 4.0 mA	–	0.15	0.40	V
Delay	V_{FFB} low to PWRGD low	50	250	600	μs
Overvoltage Protection VID					
OVP Threshold above VID	–	190	200	250	mV
Enable Input					
Start Threshold	Gates switching, SS high	0.8	–	–	V
Stop Threshold	Gates not switching, SS low	–	–	0.4	V
Input Pull−Up Voltage	1.0 MΩ to GND	2.7	2.8	3.3	V
Input Pull−Up Resistance	–	7.0	10	20	kΩ
Voltage Feedback Error Amplifier					
V_{FB} Bias Current	–	–	0.1	1.0	μA
COMP Source Current	COMP = 0.5 V to 2.0 V	40	70	100	μA
COMP Sink Current	–	40	70	100	μA
Transconductance	Note 2	1.1	1.3	1.5	mmho
Open Loop DC Gain	Note 2	72	80	–	dB
Unity Gain Bandwidth	C_{COMP} = 30 pF	–	4.0	–	MHz
PSRR @ 1.0 kHz	–	–	60	–	dB
COMP Max Voltage	V_{FB} = 0 V	2.9	3	–	V
COMP Min Voltage	V_{FB} = 1.6 V	–	50	150	mV
PWM Comparators					
Minimum Pulse Width	Measured from CSxP to GATEx, V_{FB} = CSxN = 0.5, COMP = 0.5 V, 60 mV step between CSxP and CSxN; Measure at GATEx = 1.0 V	–	40	100	ns
Transient Response Time	Measured from CSxN to GATEx, COMP = 2.1 V, CSxP = CSxN = 0.5 V, CSxN stepped from 1.2 V to 2.0 V	–	40	60	ns
Channel Start−Up Offset	CSxP = CSxN = V_{FFB} = 0, Measure Vcomp when GATEx switch high	0.35	0.6	0.75	V
Artificial Ramp Amplitude	50% duty cycle	–	100	–	mV
MOSFET Driver Enable (DRVON)					
Output High	DRVON floating	2.3	–	–	V
Output Low	–	–	–	0.2	V
Pull−Down Resistance	DRVON = 1.5 V, ENABLE = 0 V, R = 1.5 V/I(DRVON)	35	70	140	kΩ
Source Current	DRVON = 1.5 V	1	4	6.5	mA
V_{REF}					
Output Voltage	0 mA < I(V_{REF}) < 1.0 mA	3.25	3.3	3.35	V
GATES					
High Voltage	Measure GATEx, I_{GATEx} = 1.0 mA	2.25	2.70	3.00	V

2. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $V_{CCL} = V_{CC} = 12$ V; $C_{GATEx} = 100$ pF, $C_{COMP} = 0.01$ μF, $C_{SS} = 0.1$ μF, $C_{VCC} = 0.1$ μF, $R_{ROSC} = 32.4$ kΩ, $V(I_{LIM}) = 3.3$ V, $V(IP_{LIM}) = 3.3$ V, unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
GATES					
Low Voltage	Measure GATEx, $I_{GATEx} = 1.0$ mA	−	0.1	0.7	V
Rise Time GATE	0.8 V < GATEx < 2.0 V, $V_{CC} = 10$ V	−	2.5	10	ns
Fall Time GATE	2.0 V > GATEx > 0.8 V, $V_{CC} = 10$ V	−	5.0	10	ns
Oscillator					
Switching Frequency	$R_{OSC} = 32.4$ k, 4−Phase mode $R_{OSC} = 32.4$ k, 5−Phase mode $R_{OSC} = 32.4$ k, 6−Phase mode	450 520 550	525 620 650	600 720 750	kHz kHz kHz
R_{OSC} Voltage	−	0.95	1.0	1.05	V
Phase Delay, 6 Phases	−	−	60	−	deg
Phase Delay, 5 Phases	CS6P = CS6N = V_{CC}	−	72	−	deg
Phase Delay, 4 Phases	CS3P = CS3N = CS6P = CS6N = V_{CC}	−	90	−	deg
Phase Disable Threshold	V_{CC} − (CSxP = CSxN)	500	−	−	mV
Adaptive Voltage Positioning					
V_{DRP} Output Voltage to DAC_{OUT} Offset	CSxP = CSxN, V_{FB} = COMP, Measure V_{DRP} − COMP	−15	−	15	mV
Current Sense Amplifier to V_{DRP} Gain	CSxP − CSxN = 80 mV, V_{FB} = COMP, Measure V_{DRP} − COMP, $V_{DRP} = 1.0$ V	2.3	2.55	2.75	V/V
V_{DRP} Source Current	CSxP − CSxN = 0 mV, V_{FB} = COMP, $V_{DRP} = 2.0$ V	1.0	1.5	14	mA
V_{DRP} Sink Current	CSxP − CSxN = 80 mV, V_{FB} = COMP, $V_{DRP} = 0.5$ V	0.2	0.4	0.6	mA
Soft Start					
Charge Current	$V_{CCL} = 10$ V	30	40	50	μA
Discharge Current	$V_{CCL} = 7.0$ V	90	120	150	μA
COMP Pull−Down Current	$V_{CCL} = 10$ V	0.2	0.9	2.1	mA
Current Sensing and Overcurrent Protection					
CSxP Input Bias Current	CSxN = CSxP = 0 V	−	0.1	1.0	μA
CSxN Input Bias Current	CSxN = CSxP = 0 V	−	0.1	1.0	μA
Current Sense Amp to PWM Gain	CSxN = 0 V, CSxP = 80 mV, Measure V(COMP) when GATEx switches high	−	3.0	−	V/V
Current Sense Amp to PWM Bandwidth	−	−	7.0	−	MHz
Current Sense Amp to IO Gain	IO/(CSxP − CSxN), $I_{LIM} = 0.6$ V, GATEx not switching	3.85	4.2	4.4	V/V
Current Sense Amp to IO Bandwidth	−	−	1.0	−	MHz
IO Source Current	−	4.0	10	−	mA
IO Sink Current	−	0.5	0.9	1.5	mA
I_{LIM} Input Bias Current	$I_{LIM} = 0$ V	−	0.1	1.0	μA
IOF Input Bias Current	IOF = 0 V	−	0.1	1.0	μA
IP_{LIM} Input Bias Current	$IP_{LIM} = 0$ V	−	0.1	1.0	μA
Current Sense Amp to Pulse−by−Pulse Current Limit Comparator Gain	−	8.0	9.5	11	V/V
Current Sense Common Mode Input Range	Note 2	0	−	2.0	V
General Electrical Specifications					
V_{CC} Operating Current	COMP = 0.3 V (no switching)	−	36	40	mA
UVLO Start Threshold	SS charging, GATEx switching	8.5	9.0	9.5	V
UVLO Stop Threshold	GATEx not switching, SS & COMP discharging	7.5	8.0	8.5	V
UVLO Hysteresis	Start − Stop	0.8	1.0	1.2	V

2. Guaranteed by design, not tested in production.

PIN DESCRIPTION

Pin No.	Pin Symbol	Pin Name	Description
1−6	V_{ID0}−V_{ID5}	DAC VID Inputs	VID−compatible logic input used to program the converter output voltage. All high on V_{ID0}−V_{ID4} generates fault.
7	LGND	Logic Ground	IC analog ground; connected to IC substrate.
8, 9, 19, 20	NC	No Connect	For factory test only. Let these pins float.
10	SGND	Remote Sense Ground	Ground connection for DAC and error amplifier. Provides remote sensing of load ground.
11	PWRGD	Power Good Output	Open collector output goes high when the converter output is in regulation.
12	PWRLS	Power Good Sense	Voltage sensing pin for Power Good lower threshold.
13	DRVON	Drive Enable	Logic high output enables MOSFET drivers, and logic low turns all MOSFETs off through MOSFET drivers. Pulled to ground through internal 70 kΩ resistor.
14	SS	Soft Start	A capacitor between this pin and ground programs the soft start time.
15	ENABLE	Enable	A voltage less than the threshold puts the IC in Fault Mode, discharging SS. Connect to system VID_{PWRGD} signal to control power-up sequencing. Hysteresis is provided to prevent chatter.
16	V_{FFB}	Fast Voltage Feedback	Input of PWM comparator for fast voltage feedback, and also the inputs of Power Good sense and overvoltage protection comparators
17	V_{FB}	Voltage Feedback	Error amplifier inverting input.
18	COMP	Error Amp Output	Provides loop compensation and is clamped by SS during soft start and fault conditions. It is also the inverting input of PWM comparators.
21	CS6N	Current Sense Reference	Inverting input to current sense amplifier #6, and Phase 6 disable pin.
22	CS6P	Current Sense Input	Non−inverting input to current sense amplifier #6, and Phase 6 disable pin.
23	CS5N	Current Sense Reference	Inverting input to current sense amplifier #5.
24	CS5P	Current Sense Input	Non−inverting input to current sense amplifier #5.
25	CS4N	Current Sense Reference	Inverting input to current sense amplifier #4.
26	CS4P	Current Sense Input	Non−inverting input to current sense amplifier #4.
27	GND	Ground	Power supply return of Gate circuits.
28−33	GATE6−GATE1	Channel Outputs	PWM outputs to drive MOSFET driver ICs.
34	V_{CC}	Gate Power Supply	Power Supply Input for Gate circuits. Must be tied to V_{CCL}.
35	R_{OSC}	Oscillator Frequency Adjust	Resistor to ground programs the oscillator frequency, as shown in Figure 5.
36	CS1P	Current Sense Input	Non−inverting input to current sense amplifier #1.
37	CS1N	Current Sense Reference	Inverting input to current sense amplifier #1.
38	CS2P	Current Sense Input	Non−inverting input to current sense amplifier #2.
39	CS2N	Current Sense Reference	Inverting input to current sense amplifier #2.
40	CS3P	Current Sense Input	Non−inverting input to current sense amplifier #3, and Phase 3 disable pin.
41	CS3N	Current Sense Reference	Inverting input to current sense amplifier #3, and Phase 3 disable pin.
42	IP_{LIM}	Pulse−by−Pulse Limit	Resistor divider from V_{REF} to ground programs the threshold of pulse−by−pulse limit of each phase.
43	V_{DRP}	Output of Current Sense Amplifiers for Adaptive Voltage Positioning: “Droop” Pin	The offset above DAC voltage is proportional to the sum of inductor current. A resistor from this pin to V_{FB} programs the amount of Adaptive Voltage Positioning. Leave this pin open for no Adaptive Voltage Positioning.

PIN DESCRIPTION (continued)

Pin No.	Pin Symbol	Pin Name	Description
44	I_{LIM}	Total Current Limit	Resistor divider between V_{REF} and ground programs the average current limit.
45	IOF	Average Inductor Current Input	Connect a low pass filter from the 10 pin to the 10F pin to provide average inductor current information.
46	IO	Inductor Current Output	Output of the sum of inductor current.
47	V_{REF}	Reference	3.3 V reference voltage output.
48	V_{CCL}	Logic Power Supply	Power supply input for IC logic. Must be tied to V_{CC}.

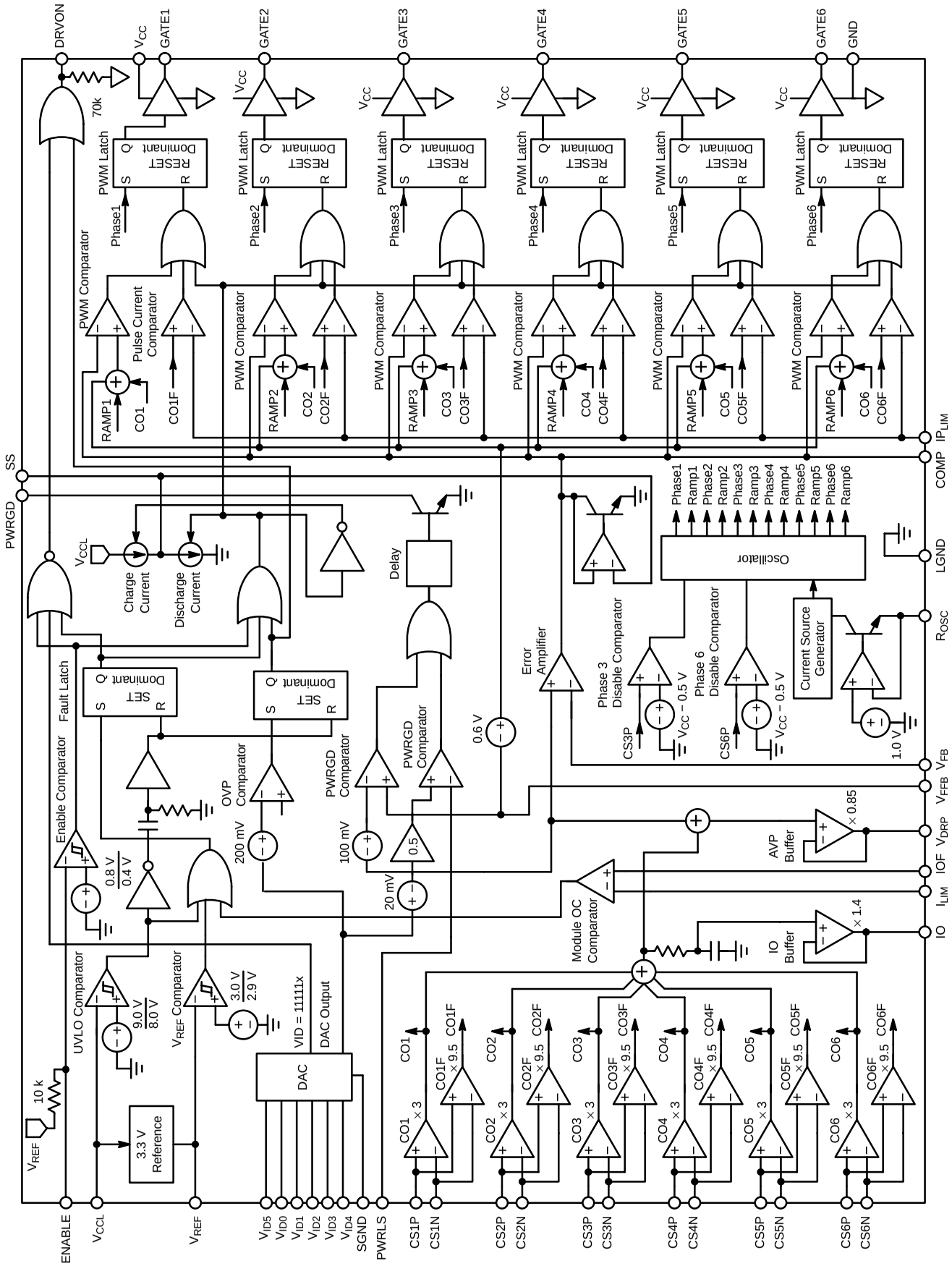


Figure 3. Block Diagram

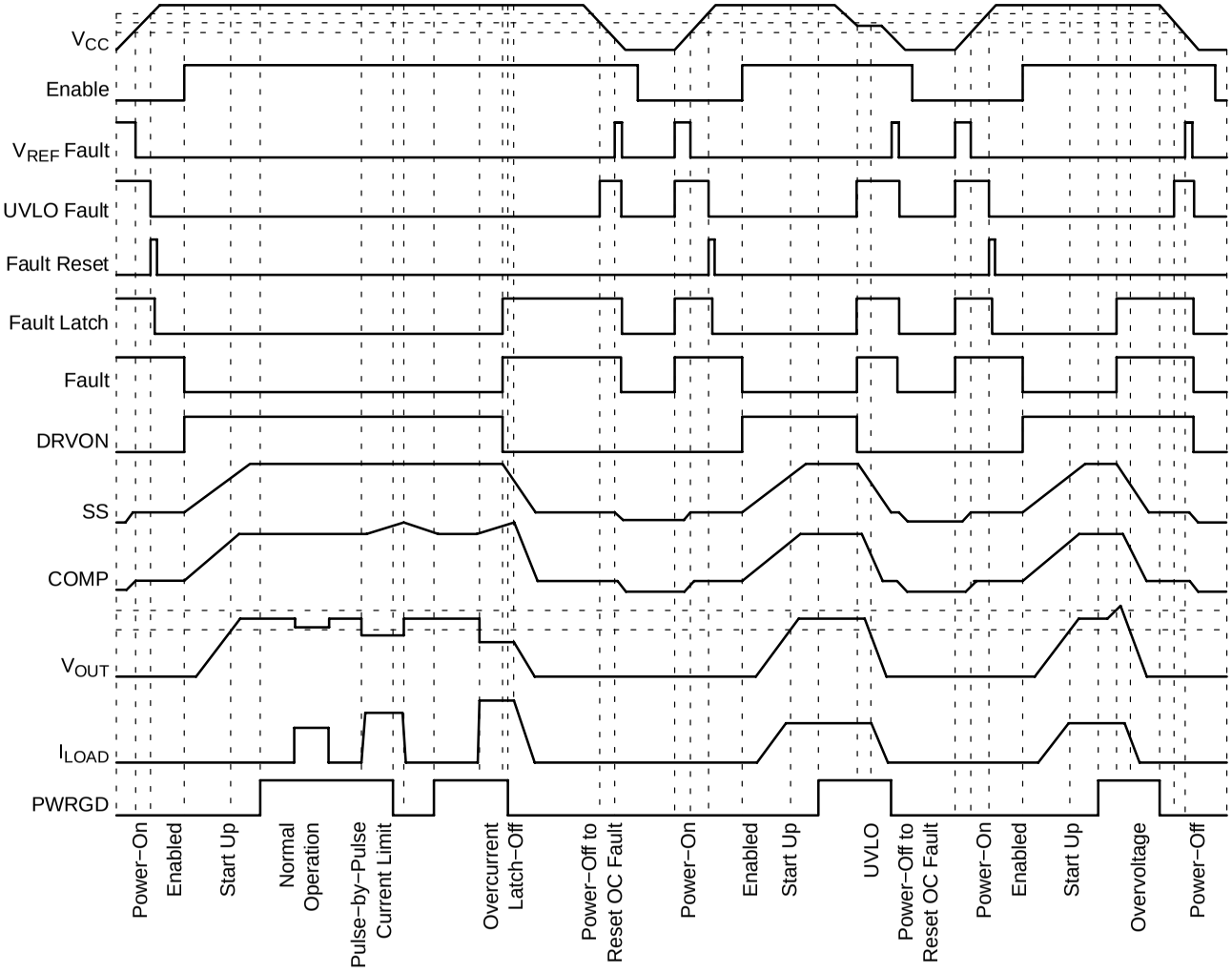


Figure 4. Operating Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

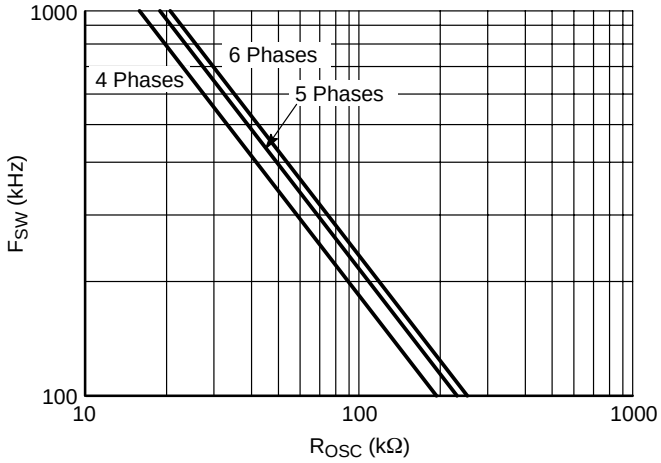


Figure 5. R_{OSC} (kΩ) vs. f_{SW} (kHz)

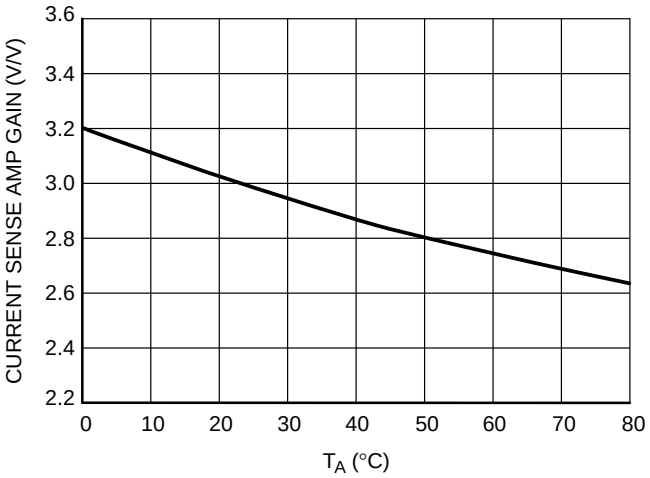


Figure 6. Current Sense Amplifier to PWM Gain vs. T_A

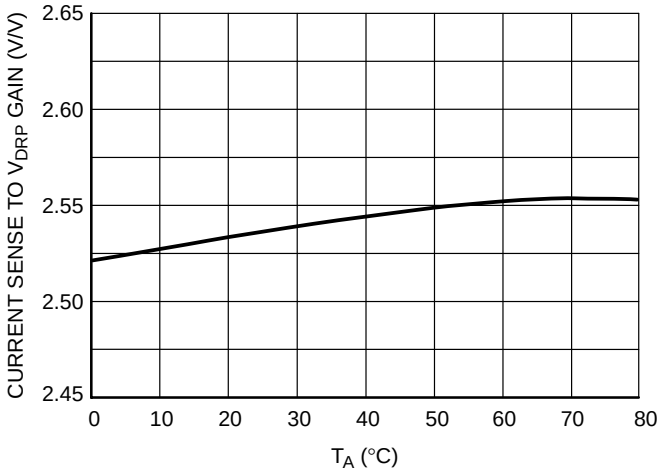


Figure 7. Current Sense to V_{DRP} Gain vs. T_A

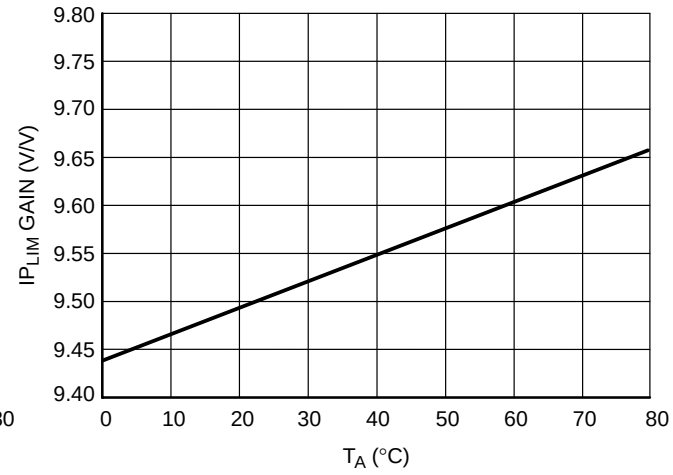


Figure 8. IP_{LIM} Gain vs. T_A

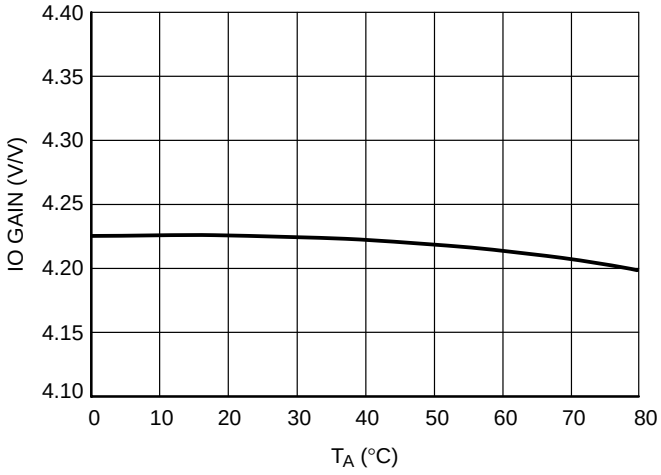


Figure 9. IO Gain vs. T_A

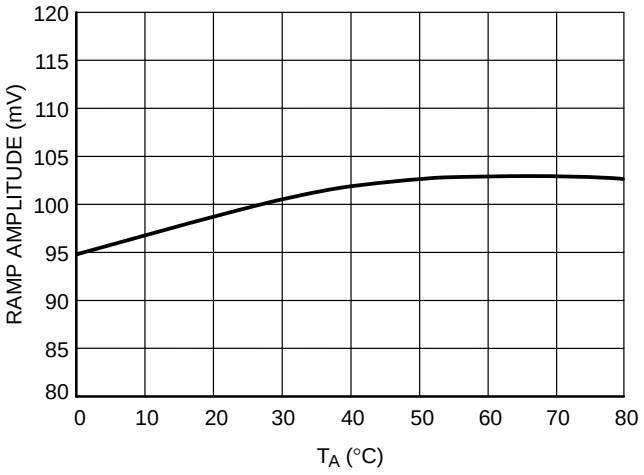


Figure 10. Artificial Ramp Amplitude at 50% Duty Cycle vs. T_A

TYPICAL PERFORMANCE CHARACTERISTICS

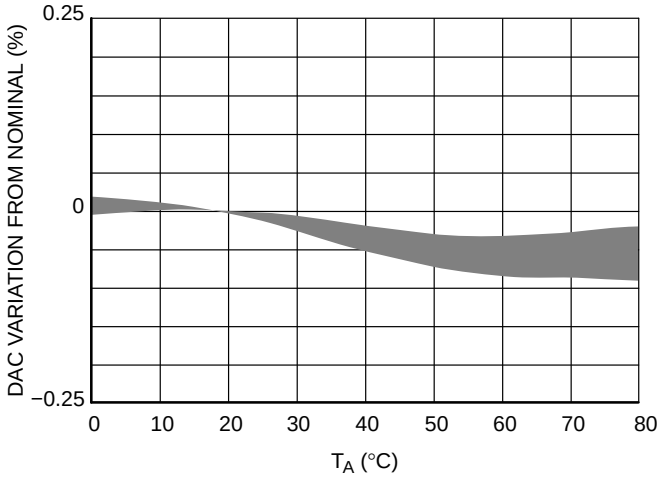


Figure 11. DAC Output vs. T_A

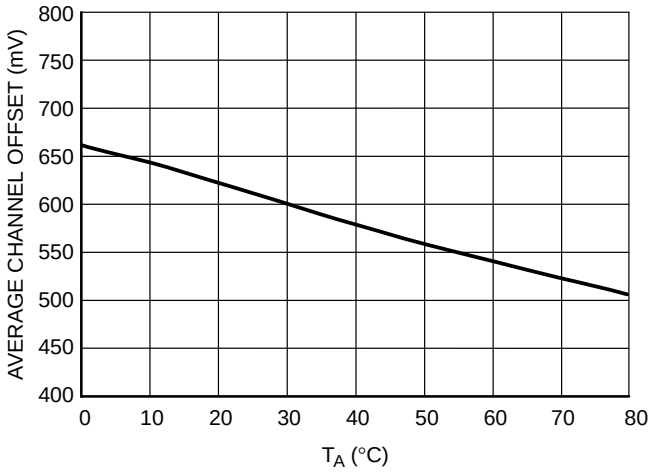


Figure 12. Average Channel Offset vs. T_A

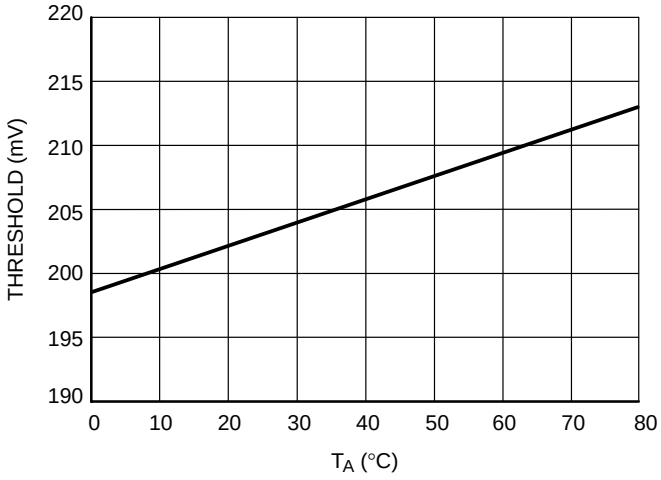


Figure 13. OVP Latch Threshold vs. T_A

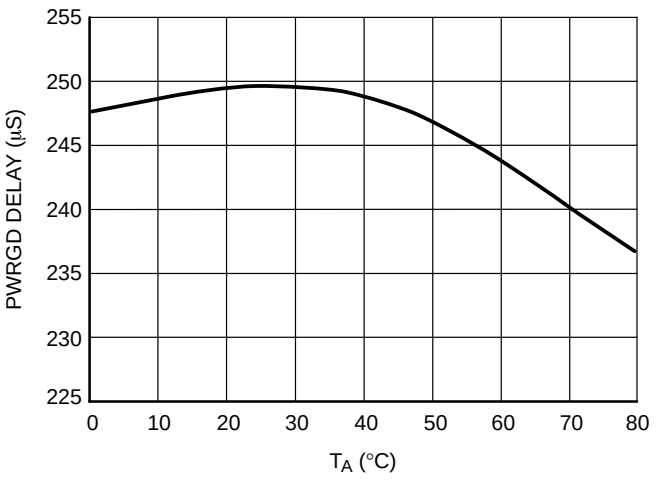


Figure 14. PWRGD Delay vs. T_A

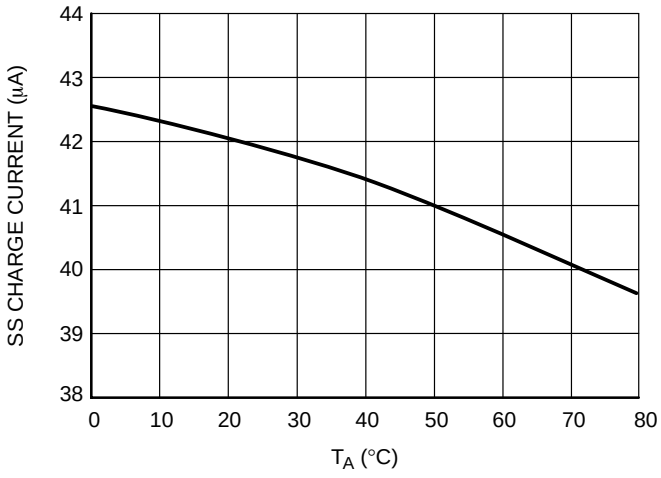


Figure 15. SS Charge Current vs. T_A

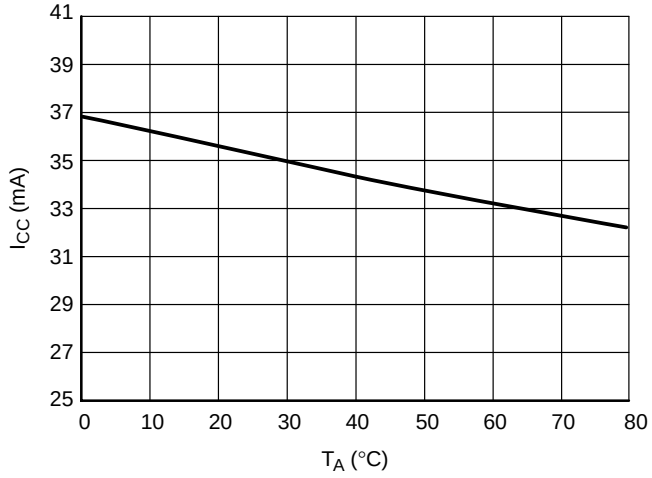


Figure 16. I_{CC} vs. T_A

APPLICATIONS INFORMATION

Overview

The NCP5316 DC/DC controller from ON Semiconductor was developed using the Enhanced V^2 topology. Enhanced V^2 combines the original V^2 topology with peak current−mode control for fast transient response and current sensing capability. The addition of an internal PWM ramp and implementation of fast−feedback directly from Vcore has improved transient response and simplified design. This controller can be adjusted to operate as a four−, five− or six−phase controller, and can also be used in a one−, two− or three−phase system. Differential current sensing provides improved current sharing and easier layout. The NCP5316 includes Power Good (PWRGD), providing a highly integrated solution to simplify design, minimize circuit board area, and reduce overall system cost.

Two advantages of a multi−phase converter over a single−phase converter are current sharing and increased effective output frequency. Current sharing allows the designer to use less inductance in each phase than would be required in a single−phase converter. The smaller inductor will produce larger ripple currents but the total per−phase power dissipation is reduced because the RMS current is lower. Transient response is improved because the control loop will measure and adjust the current faster in a smaller output inductor. Increased apparent output frequency is desirable because the off− time and the ripple voltage of the multi−phase converter will be less than that of a single−phase converter.

Fixed Frequency Multi−Phase Control

In a multi−phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The NCP5316 controller uses six−phase, fixed−frequency, Enhanced V^2 architecture to measure and control currents in individual phases. In six−phase mode, each phase is delayed 60° from the previous phase. Normally, GATEx transitions to a high voltage at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring GATEx low. Once GATEx goes low, it will remain low until the beginning of the next oscillator cycle. While GATEx is high, the Enhanced V^2 loop will respond to line and load variations. On the other hand, once GATEx is low, the loop cannot respond until the beginning of the next PWM cycle. Therefore, constant frequency Enhanced V^2 will typically respond to disturbances within the off−time of the converter.

The Enhanced V^2 architecture measures and adjusts the output current in each phase. An additional differential input (CSxN and CSxP) for inductor current information has been added to the V^2 loop for each phase as shown in Figure 17. The triangular inductor current is measured differentially across RS, amplified by CSA and summed with the channel startup offset, the internal ramp and the output voltage at the non−inverting input of the PWM comparator. The purpose of the internal ramp is to compensate for propagation delays in the NCP5316. This provides greater design flexibility by allowing smaller external ramps, lower minimum pulse widths, higher frequency operation and PWM duty cycles above 50% without external slope compensation. As the sum of the inductor current and the internal ramp increase, the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts a cycle with higher current, the PWM cycle will terminate earlier providing negative feedback. The NCP5316 provides a differential current sense input (CSxN and CSxP) for each phase. Current sharing is accomplished by referencing all phases to the same COMP pin, so that a phase with a larger current signal will turn off earlier than a phase with a smaller current signal.

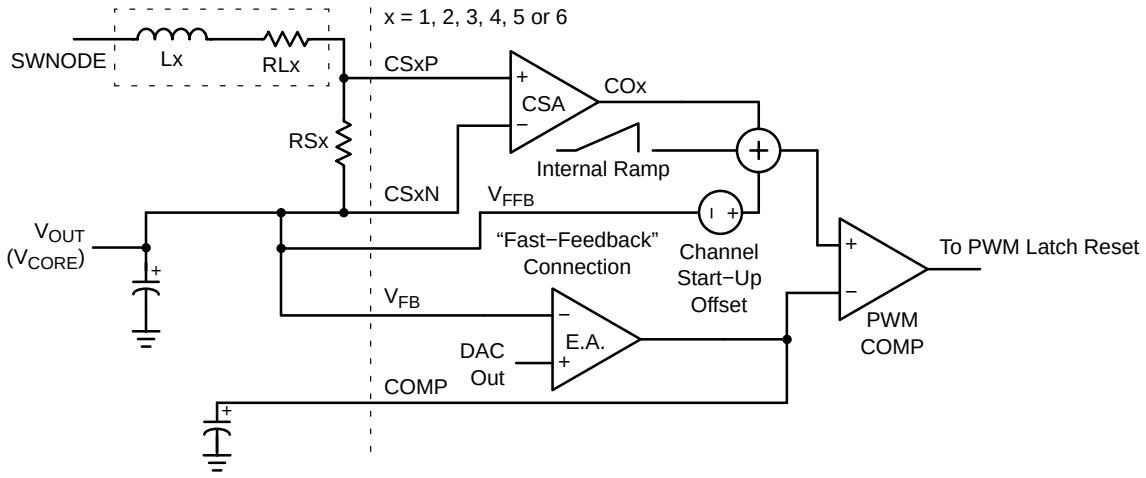


Figure 17. Enhanced V^2 Control Employing Resistive Current Sensing and Internal Ramp

Enhanced V^2 responds to disturbances in V_{CORE} by employing both “slow” and “fast” voltage regulation. The internal error amplifier performs the slow regulation. Depending on the gain and frequency compensation set by the amplifier’s external components, the error amplifier will typically begin to ramp its output to react to changes in the output voltage in one or two PWM cycles. Fast voltage feedback is implemented by a direct connection from Vcore to the non−inverting pin of the PWM comparator via the summation with the inductor current, internal ramp and offset. A rapid increase in output current will produce a negative offset at Vcore and at the output of the summer. This will cause the PWM duty cycle to increase almost instantly. Fast feedback will typically adjust the PWM duty cycle in one PWM cycle.

As shown in Figure 17, an internal ramp (100 mV at a 50% duty cycle) is added to the inductor current ramp at the positive terminal of the PWM comparator. This additional ramp compensates for propagation time delays from the current sense amplifier (CSA), the PWM comparator and the MOSFET gate drivers. As a result, the minimum ON time of the controller is reduced and lower duty−cycles may be achieved at higher frequencies. Also, the additional ramp reduces the reliance on the inductor current ramp and allows greater flexibility when choosing the output inductor and the $R_{CSx}C_{CSx}$ time constant of the feedback components from V_{CORE} to the CSx pin.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be:

$$V_{COMP} = V_{OUT} @ 0\ A + Channel\_Startup\_Offset + Int\_Ramp + G_{CSA} \cdot Ext\_Ramp/2$$

Int_Ramp is the “partial” internal ramp value at the corresponding duty cycle, Ext_Ramp is the peak−to−peak external steady−state ramp at 0 A, G_{CSA} is the current sense amplifier gain (3.0 V/V) and the channel startup offset is 0.60 V. The magnitude of the Ext_Ramp can be calculated from:

$$Ext\_Ramp = D \cdot (V_{IN} - V_{OUT})/(R_{CSx} \cdot C_{CSx} \cdot f_{SW})$$

For example, if V_{OUT} at 0 A is set to 1.480 V with AVP and the input voltage is 12.0 V, the duty cycle (D) will be 1.480/12.0 or 12.3%. Int_Ramp will be 100 mV/50% · 12.3% = 25 mV. Realistic values for R_{CSx}, C_{CSx} and f_{SW} are 10 kΩ, 0.015 μF and 650 kHz. Using these and the previously mentioned formula, Ext_Ramp will be 15.0 mV.

$$V_{COMP} = 1.480\ V + 0.60\ V + 25\ mV + 2.65\ V/V \cdot 15.0\ mV/2 = 2.125\ Vdc.$$

If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage, or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as:

$$\Delta V = R_S \cdot G_{CSA} \cdot \Delta I_{OUT}$$

The single−phase power stage output impedance is:

$$Single\ Stage\ Impedance = \Delta V_{OUT}/\Delta I_{OUT} = R_S \cdot G_{CSA}$$

The total output impedance will be the single stage impedance divided by the number of phases in operation.

The output impedance of the power stage determines how the converter will respond during the first few microseconds of a transient before the feedback loop has repositioned the COMP pin.

The peak output current can be calculated from:

$$I_{OUT,PEAK} = (V_{COMP} - V_{OUT} - Offset)/(R_S \cdot G_{CSA})$$

Figure 18 shows the step response of the COMP pin at a fixed level. Before T1, the converter is in normal steady−state operation. The inductor current provides a portion of the PWM ramp through the current sense amplifier. The PWM cycle ends when the sum of the current ramp, the “partial” internal ramp voltage signal and offset exceed the level of the COMP pin. At T1, the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the V_{FB} pin and the cycle ends at T2. After T2, the output voltage remains lower than at light load and the average current signal level (CSx output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system, the COMP pin would move higher to restore the output voltage to the original level.

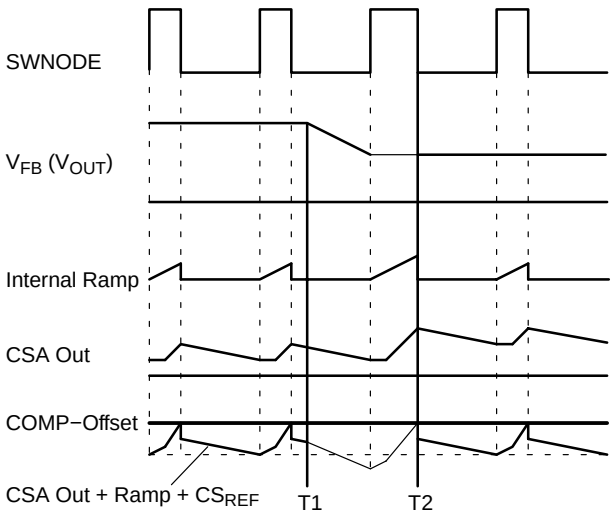


Figure 18. Open Loop Operation

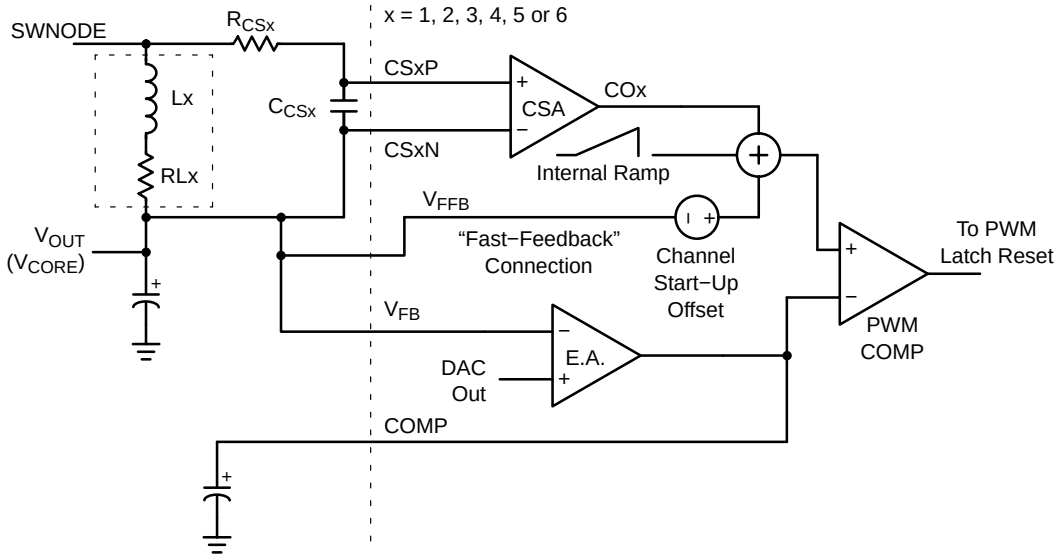


Figure 19. Enhanced V^2 Control Employing Lossless Inductive Current Sensing and Internal Ramp

Inductive Current Sensing

For lossless sensing, current can be measured across the inductor as shown in Figure 19. In the diagram, L is the output inductance and R_L is the inherent inductor resistance. To compensate the current sense signal, the values of R_{CSx} and C_{CSx} are chosen so that $L/R_L = R_{CSx} \cdot C_{CSx}$. If this criteria is met, the current sense signal should be the same shape as the inductor current and the voltage signal at CSx will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value R_L was used.

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of 0.39% per °C. The increase in winding resistance at higher temperatures should be considered when setting the threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 17.

Current Sharing Accuracy

Printed circuit board (PCB) traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at relatively the same points for each phase. In some cases, especially with inductive sensing, resistance of the PCB can be useful for increasing the current sense resistance. The total current sense resistance used for calculations must include any PCB trace resistance that carries inductor current between the CSxP input and the CSxN input.

Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case CSA input mismatch is ±10 mV and will typically be within 4.0 mV. The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance, a 3.0 mV mismatch with a 2.0 mΩ sense resistance will produce a 1.5 A difference in current between phases.

External Ramp Size and Current Sensing

The internal ramp allows flexibility in setting the current sense time constant. Typically, the current sense $R_{CSx} \cdot C_{CSx}$ time constant should be equal to or slightly slower than the inductor's time constant. If RC is chosen to be smaller (faster) than L/R_L, the AC or transient portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady−state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $R_{CSx} \cdot C_{CSx}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $R_{CSx} \cdot C_{CSx}$. If this error is excessive, it will affect transient response, adaptive positioning and current limit. During a positive current transient, the COMP pin will be required to undershoot in response to the current signal in order to maintain the output voltage. Similarly, the V_{DRP} signal will overshoot which will produce too much transient droop in the output voltage. The single−phase pulse−by−pulse overcurrent protection will trip earlier than it would if compensated correctly and hiccup−mode current limit will have a lower threshold for fast rising step loads than for slowly rising output currents.

Transient Response and Adaptive Voltage Positioning

For applications with fast transient currents, the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. Adaptive voltage positioning can reduce peak−peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is applied. Similarly, the output voltage can be set lower than nominal during heavy loads to reduce overshoot when the load current is removed. For low current applications, a droop resistor can provide fast, accurate adaptive positioning. However, at high currents, the loss in a droop resistor becomes excessive. For example, a 50 A converter with a 1 mΩ resistor would provide a 50 mV change in output voltage between no load and full load and would dissipate 2.5 W.

Lossless adaptive voltage positioning (AVP) is an alternative to using a droop resistor, but it must respond to changes in load current. Figure 20 shows how AVP works. The waveform labeled “normal” shows a converter without AVP. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) AVP, the peak−to−peak excursions are cut in half. In the slow AVP waveform, the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.

The controller can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram in Figure 2). The no−load positioning is now set internally to VID − 20 mV, reducing the potential error due to resistor and bias current mismatches.

In order to realize the AVP function, a resistor divider network is connected between V_{FB}, V_{DRP} and V_{OUT}. During no−load conditions, the V_{DRP} pin is at the same voltage as the V_{FB} pin. As the output current increases, the V_{DRP} pin voltage increases proportionally. This drives the V_{FB} voltage higher, causing V_{OUT} to “droop” according to a loadline set by the resistor divider network.

The response during the first few microseconds of a load transient is controlled primarily by power stage output impedance, and by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow, there will be a long transition to the final voltage after a transient. This will be most apparent with low capacitance output filters.

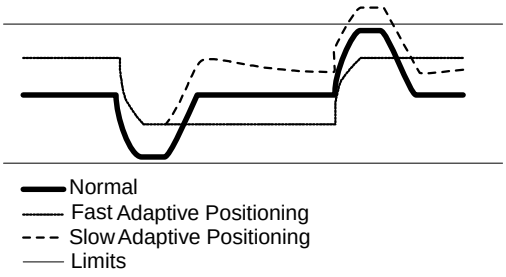


Figure 20. Adaptive Voltage Positioning

Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced V^2 control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 40 ns, causing the GATEx output to shut off. The (external) MOSFET driver should react normally to turn off the top MOSFET and turn on the bottom MOSFET. This results in a “crowbar” action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the fault latch is reset by cycling power at the V_{CC} pin.

If the voltage at the V_{FFB} pin exceeds 200 mV above the VID voltage, the converter will latch off.

Power Good

According to the latest specifications, the Power Good (PWRGD) signal must be asserted when the output voltage is within a window defined by the VID code, as shown in Figure 21.

The PWRLS pin is provided to allow the PWRGD comparators to accurately sense the output voltage. The effect of the PWRGD lower threshold can be modified using a resistor divider from the output to PWRLS to ground, as shown in Figure 22.

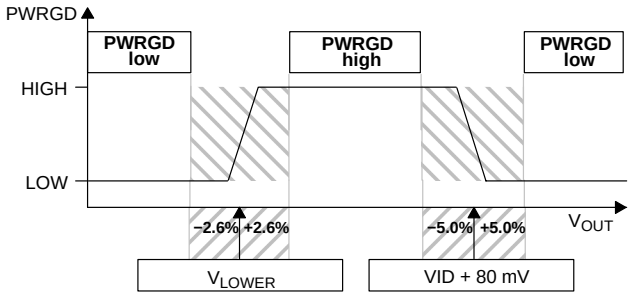


Figure 21. PWRGD Assertion Window

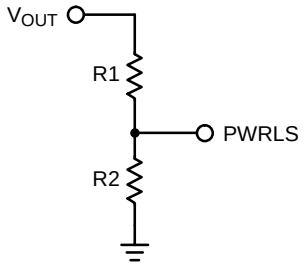


Figure 22. Adjusting the PWRGD Threshold

Since the internally−set thresholds for PWRLS are V_{OUT} No Load /2 for the lower threshold and V_{OUT} No Load + 100 mV for the upper threshold, a simple equation can be provided to assist the designer in selecting a resistor divider to provide the desired PWRGD performance.

$$V_{LOWER} = \frac{V_{OUT}\ NoLoad}{2} \cdot \frac{R_1 + R_2}{R_1}$$

$$V_{UPPER} = V_{OUT}\ NoLoad + 100\ mV$$

The logic circuitry inside the chip sets PWRGD low only after a delay period has been passed. A “power bad” event does not cause PWRGD to go low unless it is sustained through the delay time of 250 μs. If the anomaly disappears before the end of the delay, the PWRGD output will never be set low.

In order to use the PWRGD pin as specified, the user is advised to connect external resistors as necessary to limit the current into this pin to 4 mA or less.

Undervoltage Lockout

The NCP5316 includes an undervoltage lockout circuit. This circuit keeps the IC’s output drivers low until V_{CC} applied to the IC reaches 9 V. The GATE outputs are disabled when V_{CC} drops below 8 V.

Soft Start

At initial power−up, both SS and COMP voltages are zero. The total SS capacitance will begin to charge with a current of 40 μA. The error amplifier directly charges the COMP capacitance. An internal clamp ensures that the COMP pin voltage will always be less than the voltage at the SS pin, ensuring proper start−up behavior. All GATE outputs are held low until the COMP voltage reaches 0.6 V. Once this threshold is reached, the GATE outputs are released to operate normally.

Current Limit

Two levels of over−current protection are provided. First, if the absolute value of the voltage between the Current Sense pins (CSxN and CSxP) exceeds the voltage at the IP_{LIM} pin (Single Pulse Current Limit), the PWM comparator is turned off. This provides fast peak current protection for individual phases. Second, the individual phase currents are summed and externally low−pass filtered to compare an averaged current signal to a user adjustable voltage on the I_{LIM} pin. If the I_{LIM} voltage is exceeded, the fault latch trips and the converter is latched off. V_{CC} must be recycled to reset the latch.

Fault Protection Logic

The NCP5316 includes fault protection circuitry to prevent harmful modes of operation from occurring. The fault logic is described in Table 1.

Gate Outputs

The NCP5316 is designed to operate with external gate drivers. Accordingly, the gate outputs are capable of driving a 100 pF load with typical rise and fall times of 5 ns.

Digital to Analog Converter (DAC)

The output voltage of the NCP5316 is set by means of a 6−bit, 0.5% DAC. The VID pins must be pulled high externally. A 1 kΩ pullup to a maximum of 3.3 V is recommended to meet Intel specifications. To ensure valid logic signals, the designer should ensure at least 800 mV will be present at the IC for a logic high.

The output of the DAC is described in the Electrical Characteristics section of the data sheet. These outputs are consistent with VR 10.x and processor specifications. The DAC output is equal to the VID code specification minus 20 mV.

The latest VR and processor specifications require a power supply to turn its output off in the event of a 11111X VID code. When the DAC sees such a code, the GATE pins stop switching and go low. This condition is described in Table 1.

Table 1. Description of Fault Logic

Faults	Results				
	Stop Switching	PWRGD Level	Driver Enable	SS Characteristics	Reset Method
Overvoltage Lockout	Yes		High	−0.3 mA	Power On
Enable Low	Yes	Depends on output voltage level	Low	−0.3 mA	Not Affected
Module Overcurrent Limit	Yes	Depends on output voltage level	Low	−0.3 mA	Power On
DAC Code = 11111x	Yes	Depends on output voltage level	Low	−0.3 mA	Change VID Code
V_{REF} Undervoltage Lockout	Yes	Depends on output voltage level	Low	−0.3 mA	Power On
Phase Negative Overcurrent Limit	Yes	Depends on output voltage level	Low	−0.3 mA	Power On
Phase Overcurrent Limit	Terminate Pulse	Depends on output voltage level	High	Not Affected	Not Affected
PWRLS Out of Range	No	Low	High	Not Affected	Not Affected

Adjusting the Number of Phases

The NCP5316 was designed with a selectable−phase architecture. Designers may choose any number of phases up to six. The phase delay is automatically adjusted to match the number of phases that will be used. This feature allows the designer to select the number of phases required for a particular application.

Six−phase operation is standard. All phases switch with a 60 degree delay between pulses. No special connections are required.

Five−phase operation is achieved by disabling either phase 3 or phase 6. Tie together CS3N and CS3P or CS6N and CS6P, and then pull both pins to V_{CC}. The remaining phases will continue to switch, but now there will be a 72 degree delay between pulses. The phase firing order will become 1−2−3−4−5 or 1−2−4−5−6, depending on which phase was disabled.

Four−phase operation is achieved by tying together CS3N, CS3P, CS6N and CS6P, and pulling all of these pins to V_{CC}. This will result in a 90 degree phase delay, and a firing order of 1−2−4−5.

Three−phase operation may be realized as well. First, the designer must choose the proper phases. For example, for three−phase operation, phases 2, 4 and 6 must be selected.

Second, the current sense inputs should be pulled to a defined voltage ground. Simply tie all the current sense inputs of the unused phases together and connect them to ground.

Design Procedure

1. Setting the Switching Frequency

The per−phase switching frequency is set by placing a resistor from ROSC to GND. Choose the resistor according to Figure 6.

2. Output Capacitor Selection

The output capacitors filter the current from the output inductor and provide a low impedance for transient load current changes. Typically, microprocessor applications require both bulk (electrolytic, tantalum) and low impedance, high frequency (ceramic) types of capacitors. The bulk capacitors provide “hold up” during transient loading. The low impedance capacitors reduce steady−state ripple and bypass the bulk capacitance when the output current changes very quickly. The microprocessor manufacturers usually specify a minimum number of ceramic capacitors. The designer must determine the number of bulk capacitors.

Choose the number of bulk output capacitors to meet the peak transient requirements. The formula below can be used to provide a starting point for the minimum number of bulk capacitors ($N_{OUT,MIN}$):

$$N_{OUT,MIN} = \text{ESR per capacitor} \cdot \frac{\Delta I_{O,MAX}}{\Delta V_{O,MAX}} \quad (1)$$

In reality, both the ESR and ESL of the bulk capacitors determine the voltage change during a load transient according to:

$$\Delta V_{O,MAX} = (\Delta I_{O,MAX}/\Delta t) \cdot ESL + \Delta I_{O,MAX} \cdot ESR \quad (2)$$

Unfortunately, capacitor manufacturers do not specify the ESL of their components and the inductance added by the PCB traces is highly dependent on the layout and routing. Therefore, it is necessary to start a design with slightly more than the minimum number of bulk capacitors and perform transient testing or careful modeling/simulation to determine the final number of bulk capacitors.

The latest Intel processor specifications discuss “dynamic VID” (DVID), in which the VID codes are stepped up or down to a new desired output voltage. Due to the timing requirements at which the output must be in regulation, the output capacitor selection becomes more complicated. The ideal output capacitor selection has low ESR and low capacitance. Too much output capacitance will make it difficult to meet DVID timing specifications; too much ESR will complicate the transient solution. The Sanyo 4SEPC560 and Panasonic EEU−FL provide a good balance of capacitance vs. ESR.

3. Output Inductor Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady−state and transient performance of the converter. When selecting an inductor, the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size and cost (usually the primary concern).

In general, the output inductance value should be electrically and physically as small as possible to provide the best transient response at minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc.) resulting in increased dissipation and lower converter efficiency. Increased ripple currents force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors, adversely affecting converter cost.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. Equation 3 may be used to calculate the minimum inductor value to produce a given maximum ripple current (α) per phase. The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the selected maximum ripple current.

$$Lo_{MIN} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{(\alpha \cdot I_{O,MAX} \cdot V_{IN} \cdot f_{SW})} \quad (3)$$

α is the ripple current as a percentage of the maximum output current *per phase* (α = 0.15 for ±15%, α= 0.25 for ±25%, etc.). If the minimum inductor value is used, the inductor current will swing ± α% about its value at the center. Therefore, for a four−phase converter, the inductor must be designed or selected such that it will not saturate with a peak current of $(1 + \alpha) \cdot I_{O,MAX}/4$.

The maximum inductor value is limited by the transient response of the converter. If the converter is to have a fast transient response, the inductor should be made as small as possible. If the inductor is too large its current will change too slowly, the output voltage will droop excessively, more bulk capacitors will be required and the converter cost will be increased. For a given inductor value, it is useful to determine the times required to increase or decrease the current.

For increasing current:

$$\Delta t_{INC} = Lo \cdot \Delta I_O/(V_{IN} - V_{OUT}) \quad (3.1)$$

For decreasing current:

$$\Delta t_{DEC} = Lo \cdot \Delta I_O/(V_{OUT}) \quad (3.2)$$

For typical processor applications with output voltages less than half the input voltage, the current will be increased much more quickly than it can be decreased. Thus, it may be more difficult for the converter to stay within the regulation limits when the load is removed than when it is applied and excessive overshoot may result.

The output voltage ripple can be calculated using the output inductor value derived in this Section (Lo_{MIN}), the number of output capacitors ($N_{OUT,MIN}$) and the per capacitor ESR determined in the previous Section:

$$V_{OUT,P-P} = (\text{ESR per cap} / N_{OUT,MIN}) \cdot \{(V_{IN} - \#\text{Phases} \cdot V_{OUT}) \cdot D / (Lo_{MIN} \cdot f_{SW})\} \quad (4)$$

This formula assumes steady−state conditions with no more than one phase on at any time. The second term in Equation 4 is the total ripple current seen by the output capacitors. The total output ripple current is the “time summation” of the four individual phase currents that are 90 degrees out−of−phase. As the inductor current in one phase ramps upward, current in the other phase ramps downward and provides a canceling of currents during part of the switching cycle. Therefore, the total output ripple current and voltage are reduced in a multi−phase converter.

4. Input Capacitor Selection

The choice and number of input capacitors is primarily determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with adequate margin. To calculate the number of input capacitors, one must first determine the total RMS input ripple current. To this end, begin by calculating the average input current to the converter:

$$I_{IN,AVG} = I_{O,MAX} \cdot D/\eta \quad (5)$$

where:

D is the duty cycle of the converter, $D = V_{OUT}/V_{IN}$;

η is the specified minimum efficiency;

$I_{O,MAX}$ is the maximum converter output current.

The input capacitors will discharge when the control FET is ON and charge when the control FET is OFF as shown in Figure 23.

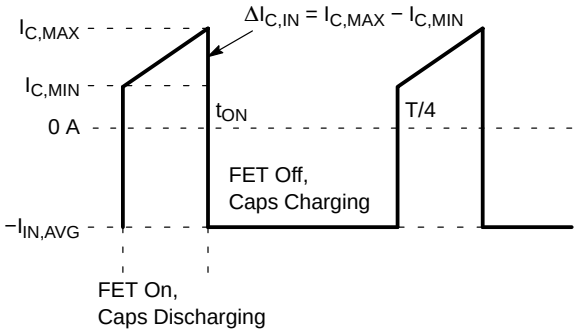


Figure 23. Input Capacitor Current for a Four−Phase Converter

The following equations will determine the maximum and minimum currents delivered by the input capacitors:

$$I_{C,MAX} = I_{Lo,MAX}/\eta - I_{IN,AVG} \quad (6)$$

$$I_{C,MIN} = I_{Lo,MIN}/\eta - I_{IN,AVG} \quad (7)$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/\phi + \Delta I_{Lo}/2 \quad (8)$$

where ϕ is the number of phases in operation.

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/\phi - \Delta I_{Lo}/2 \quad (9)$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value Lo:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW}) \quad (10)$$

For the four−phase converter, the input capacitor(s) RMS current is then:

$$I_{CIN,RMS} = [4D \cdot (I_{C,MIN}^2 + I_{C,MIN} \cdot \Delta I_{C,IN} + \Delta I_{C,IN}^2/3) + I_{IN,AVG}^2 \cdot (1 - 4D)]^{1/2} \quad (11)$$

Select the number of input capacitors (N_{IN}) to provide the RMS input current ($I_{CIN,RMS}$) based on the RMS ripple current rating per capacitor ($I_{RMS,RATED}$):

$$N_{IN} = I_{CIN,RMS}/I_{RMS,RATED} \quad (12)$$

For a four−phase converter with perfect efficiency ($\eta = 1$), the worst case input ripple−current will occur when the converter is operating at a 12.5% duty cycle. At this operating point, the parallel combination of input capacitors must support an RMS ripple current equal to 12.5% of the converter's DC output current. At other duty cycles, the ripple−current will be less. For example, at a duty cycle of either 6% or 19%, the four−phase input ripple−current will be approximately 10% of the converter's DC output current.

In general, capacitor manufacturers require derating to the specified ripple−current based on the ambient temperature. More capacitors will be required because of the current derating. The designer should know the ESR of the input capacitors. The input capacitor power loss can be calculated from:

$$P_{CIN} = I_{CIN,RMS}^2 \cdot ESR\_per\_capacitor/N_{IN} \quad (13)$$

Low ESR capacitors are recommended to minimize losses and reduce capacitor heating. The life of an electrolytic capacitor is reduced 50% for every 10°C rise in the capacitor's temperature.

5. Input Inductor Selection

The use of an inductor between the input capacitors and the power source will accomplish two objectives. First, it will isolate the voltage source and the system from the noise generated in the switching supply. Second, it will limit the inrush current into the input capacitors at power up. Large inrush currents reduce the expected life of the input capacitors. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients.

The worst case input current slew rate will occur during the first few PWM cycles immediately after a step−load change is applied as shown in Figure 24. When the load is applied, the output voltage is pulled down very quickly. Current through the output inductors will not change instantaneously, so the initial transient load current must be conducted by the output capacitors. The output voltage will step downward depending on the magnitude of the output current ($I_{O,MAX}$), the per capacitor ESR of the output capacitors (ESR_{OUT}) and the number of the output capacitors (N_{OUT}) as shown in Figure 24. Assuming the load current is shared equally between all phases, the output voltage at full transient load will be:

$$V_{OUT,FULL-LOAD} = V_{OUT,NO-LOAD} - (I_{O,MAX}/\phi) \cdot ESR_{OUT}/N_{OUT} \quad (14)$$

When the control MOSFET (Q1 in Figure 24) turns ON, the input voltage will be applied to the opposite terminal of the output inductor (the SWNODE). At that instant, the voltage across the output inductor can be calculated as:

$$\Delta V_{Lo} = V_{IN} - V_{OUT,FULL-LOAD} = V_{IN} - V_{OUT,NO-LOAD} + (I_{O,MAX}/\phi) \cdot ESR_{OUT}/N_{OUT} \quad (15)$$

The differential voltage across the output inductor will cause its current to increase linearly with time. The slew rate of this current can be calculated from:

$$dI_{Lo}/dt = \Delta V_{Lo}/Lo \quad (16)$$

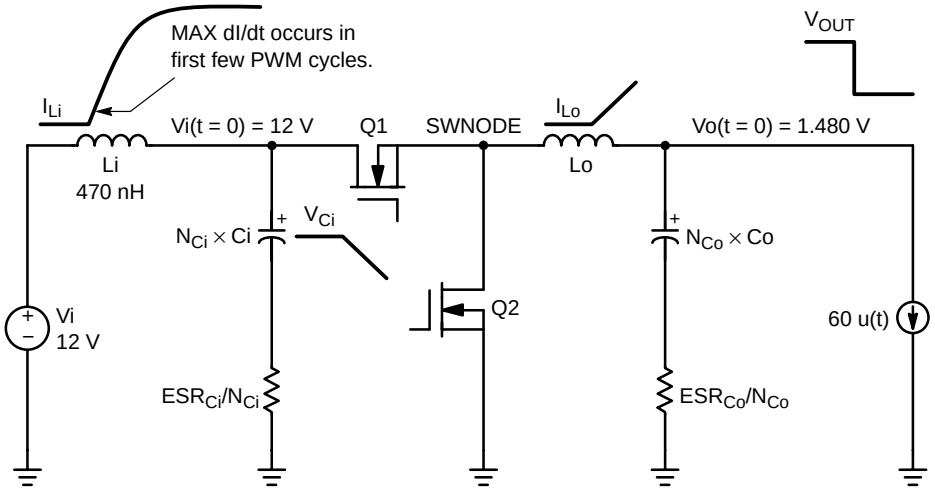


Figure 24. Calculating the Input Inductance

Current changes slowly in the input inductor so the input capacitors must initially deliver the vast majority of the input current. The amount of voltage drop across the input capacitors (ΔV_{Ci}) is determined by the number of input capacitors (N_{IN}), their per capacitor ESR (ESR_{IN}) and the current in the output inductor according to:

$$\Delta V_{Ci} = ESR_{IN}/N_{IN}\, dI \cdot Lo/dt \cdot D/f_{SW} \quad (17)$$

Before the load is applied, the voltage across the input inductor (V_{Li}) is very small and the input capacitors charge to the input voltage V_{IN}. After the load is applied, the voltage drop across the input capacitors, ΔV_{Ci}, appears across the input inductor as well. Knowing this, the minimum value of the input inductor can be calculated from:

$$Li_{MIN} = V_{Li} / dI_{IN}/dt_{MAX} = \Delta V_{Ci} / dI_{IN}/dt_{MAX} \quad (18)$$

dI_{IN}/dt_{MAX} is the maximum allowable input current slew rate.

The input inductance value calculated from Equation 18 is relatively conservative. It assumes the supply voltage is very “stiff” and does not account for any parasitic elements that will limit dI/dt such as stray inductance. Also, the ESR values of the capacitors specified by the manufacturer’s data sheets are worst case high limits. In reality, input voltage “sag,” lower capacitor ESRs and stray inductance will help reduce the slew rate of the input current.

As with the output inductor, the input inductor must support the maximum current without saturating the inductor. Also, for an inexpensive iron powder core, such as the −26 or −52 from Micrometals, the inductance “swing” with DC bias must be taken into account and inductance will decrease as the DC input current increases. At the maximum input current, the inductance must not decrease below the minimum value or the dI/dt will be higher than expected.

6. MOSFET & Heatsink Selection

Power dissipation, package size and thermal requirements drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non−overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$P_{D,CONTROL} = (I_{RMS,CNTL}^2 \cdot R_{DS(on)}) + (I_{Lo,MAX} \cdot Q_{switch}/I_g \cdot V_{IN} \cdot f_{SW}) + (Q_{oss}/2 \cdot V_{IN} \cdot f_{SW}) + (V_{IN} \cdot Q_{RR} \cdot f_{SW}) \quad (19)$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the loss associated with the control and synchronous MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the synchronous MOSFET. The first two terms are usually adequate to predict the majority of the losses.

$I_{RMS,CNTL}$ is the RMS value of the trapezoidal current in the control MOSFET:

$$I_{RMS,CNTL} = \sqrt{D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (20)$$

$I_{Lo,MAX}$ is the maximum output inductor current:

$$I_{Lo,MAX} = I_{O,MAX}/\phi + \Delta I_{Lo}/2 \quad (21)$$

$I_{Lo,MIN}$ is the minimum output inductor current:

$$I_{Lo,MIN} = I_{O,MAX}/\phi - \Delta I_{Lo}/2 \quad (22)$$

$I_{O,MAX}$ is the maximum converter output current.
D is the duty cycle of the converter:

$$D = V_{OUT}/V_{IN} \quad (23)$$

ΔI_{Lo} is the peak−to−peak ripple current in the output inductor of value L_o:

$$\Delta I_{Lo} = (V_{IN} - V_{OUT}) \cdot D/(Lo \cdot f_{SW}) \quad (24)$$

$R_{DS(on)}$ is the ON resistance of the MOSFET at the applied gate drive voltage.

Q_{switch} is the post gate threshold portion of the gate−to−source charge plus the gate−to−drain charge. This may be specified in the data sheet or approximated from the gate−charge curve as shown in the Figure 25.

$$Q_{switch} = Q_{gs2} + Q_{gd} \quad (25)$$

I_g is the output current from the gate driver IC.
V_{IN} is the input voltage to the converter.
f_{sw} is the switching frequency of the converter.
Q_G is the MOSFET total gate charge to obtain $R_{DS(on)}$; commonly specified in the data sheet.
V_g is the gate drive voltage.
Q_{RR} is the reverse recovery charge of the *lower* MOSFET.
Q_{oss} is the MOSFET output charge specified in the data sheet.

For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$P_{D,SYNCH} = (I_{RMS,SYNCH}^2 \cdot R_{DS(on)}) + (Vf_{diode} \cdot I_{O,MAX}/2 \cdot t\_nonoverlap \cdot f_{SW}) \quad (26)$$

where:

Vf_{diode} is the forward voltage of the MOSFET's intrinsic diode at the converter output current.
t_nonoverlap is the non−overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non−overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$I_{RMS,SYNCH} = \sqrt{1 - D} \cdot [(I_{Lo,MAX}^2 + I_{Lo,MAX} \cdot I_{Lo,MIN} + I_{Lo,MIN}^2)/3]^{1/2} \quad (27)$$

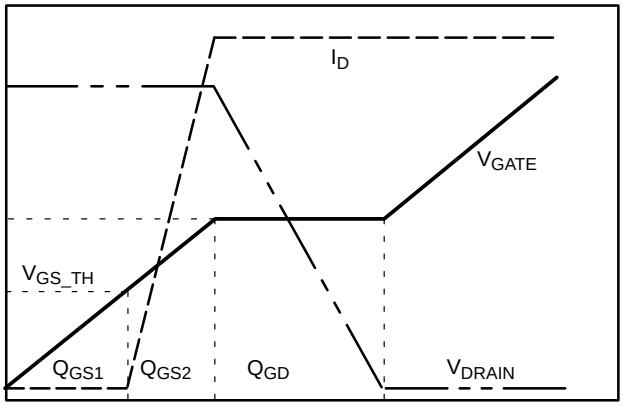


Figure 25. MOSFET Switching Characteristics

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature.

$$\theta_T < (T_J - T_A)/P_D \quad (28)$$

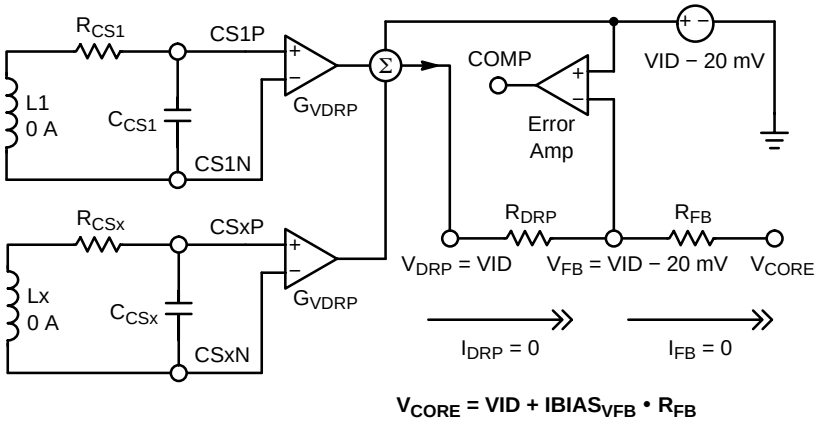
where:

θ_T is the total thermal impedance ($\theta_{JC} + \theta_{SA}$);
θ_{JC} is the junction−to−case thermal impedance of the MOSFET;
θ_{SA} is the sink−to−ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal "pad" is used);
T_J is the specified maximum allowed junction temperature;
T_A is the worst case ambient operating temperature.

For TO−220 and TO−263 packages, standard FR−4 copper clad circuit boards will have approximate thermal resistances (θ_{SA}) as shown below:

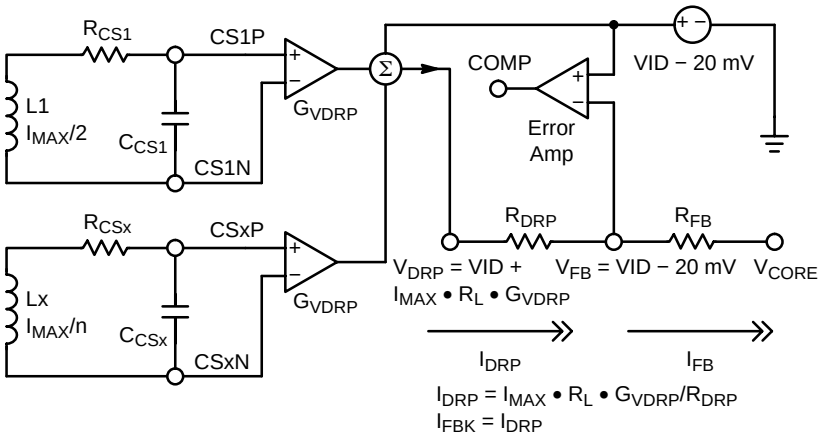
Pad Size (in^2/mm^2)	Single−Sided 1 oz. Copper
0.50/323	60−65°C/W
0.75/484	55−60°C/W
1.00/645	50−55°C/W
1.50/968	45−50°C/W

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading and component variations (i.e., worst case MOSFET $R_{DS(on)}$). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, it is advisable to have as much heatsink area as possible. All too often, new designs are found to be too hot and require re−design to add heatsinking.



$$V_{CORE} = VID + IBIAS_{VFB} \bullet R_{FB}$$

Figure 26. AVP Circuitry at No−Load



$$V_{CORE} = VID - I_{DRP} \bullet R_{FB}$$
$$= VID - I_{MAX} \bullet R_L \bullet G_{VDRP} \bullet R_{FB}/R_{DRP}$$

Figure 27. AVP Circuitry at Full−Load

7. Adaptive Voltage Positioning

Two resistors program the Adaptive Voltage Positioning (AVP): R_{FB} and R_{DRP}. These components form a resistor divider, shown in Figures 26 and 27, between V_{DRP}, V_{FB}, and V_{OUT}.

Resistor R_{FB} is connected between V_{OUT} and the V_{FB} pin of the controller. At no load, this resistor will conduct the very small internal bias current of the V_{FB} pin. Therefore V_{FB} should be kept below 10 kΩ to avoid output voltage error due to the input bias current. If the R_{FB} resistor is kept small, the V_{FB} bias current can be ignored.

Resistor R_{DRP} is connected between the V_{DRP} and V_{FB} pins of the controller. At no load, these pins should be at an equal potential, and no current should flow through R_{DRP}. In reality, the bias current coming out of the V_{DRP} pin is likely to have a small positive voltage with respect to V_{FB}. This current produces a small decrease in output voltage at no load, which can be minimized by keeping the R_{DRP} resistor below 30 kΩ. As load current increases, the voltage at the V_{DRP} pin rises. The ratio of the R_{DRP} and R_{FB} resistors causes the voltage at the V_{FB} pin to rise, reducing the output voltage. Figure 28 shows the DC effect of AVP, given an appropriate resistor ratio.

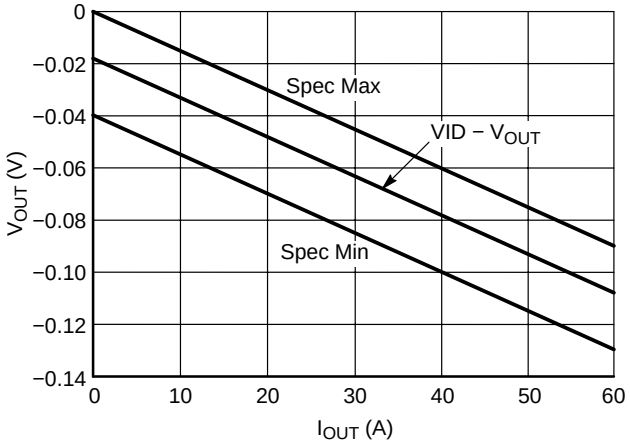


Figure 28. The DC Effects of AVP vs. Load

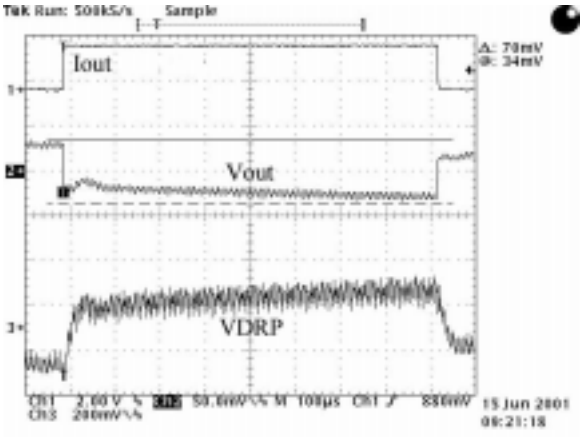


Figure 29. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Long (Slow): V_{DRP} and V_{OUT} Respond Too Slowly.

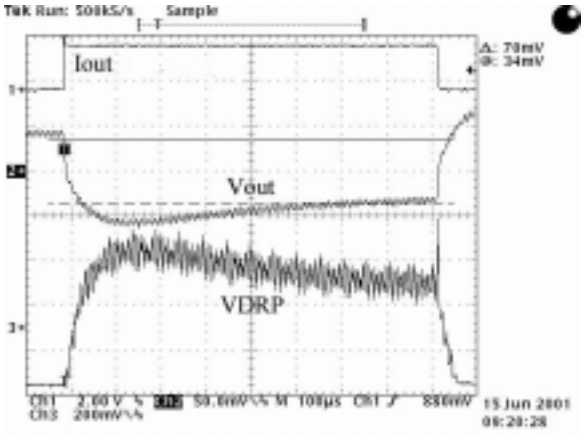


Figure 30. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Short (Fast): V_{DRP} and V_{OUT} Both Overshoot.

To choose components, recall that the two resistors R_{FB} and R_{DRP} form a voltage divider. Select the appropriate resistor ratio to achieve the desired loadline. At no load, the output voltage is positioned 20 mV below the DAC output setting. The output voltage droop will follow the equation:

$$R_{DRP} = g \cdot \frac{R_L R_{FB}}{R_{LL}} \quad (29)$$

where:

g = gain of the current sense amplifiers (V/V);

R_{SENSE} = resistance of the sense element (mΩ);

R_{LL} = load line resistance (mΩ).

It is easiest to select a value for R_{FB} and then evaluate the equation to find R_{DRP}. R_{LL} is simply the desired output voltage droop divided by the output current. If a sense resistor is used to detect inductor current, then R_{SENSE} will be the value of the sense resistor. If inductor sensing is used, R_{SENSE} will be the resistance of the inductor, assuming that the current sense network equation (eq. 30) is valid. Refer to the discussion on Current Sensing for further information.

8. Current Sensing

Current sensing is used to balance current between different phases, to limit the maximum phase current and to limit the maximum system current. Since the current information, sensed across the inductor, is a part of the control loop, better stability is achieved if the current information is accurate and noise−free. The NCP5316 introduces a novel feature to achieve the best possible performance: differential current sense amplifiers.

Two sense lines are routed for each phase, as shown in Figure 27.

For inductive current sensing, choose the current sense network (R_{CSx}, C_{CSx}, x = 1, 2, 3, 4, 5 or 6) to satisfy

$$R_{CSx} \cdot C_{CSx} = Lo/(R_L + R_{PCB}) \quad (30)$$

For resistive current sensing, choose the current sense network (R_{CSx}, C_{CSx}, x = 1, 2, 3, 4, 5 or 6) to satisfy

$$R_{CSx} \cdot C_{CSx} = Lo/(R_{sense}) \quad (31)$$

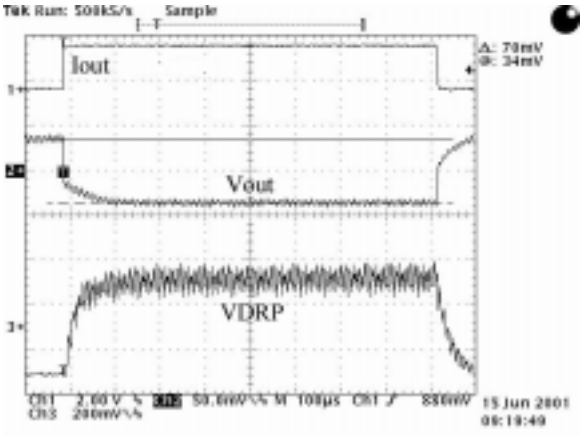


Figure 31. V_{DRP} Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Optimal: V_{DRP} and V_{OUT} Respond to the Load Current Quickly Without Overshooting.

This will provide an adequate starting point for R_{CSx} and C_{CSx}. After the converter is constructed, the value of R_{CSx} (and/or C_{CSx}) should be fine−tuned in the lab by observing the V_{DRP} signal during a step change in load current. Tune the $R_{CSx} \cdot C_{CSx}$ network by varying R_{CSx} to provide a "square−wave" at the V_{DRP} output pin with maximum rise time and minimal overshoot as shown in Figure 31.

9. Error Amplifier Tuning

After the steady−state (static) AVP has been set and the current sense network has been optimized, the Error Amplifier must be tuned. The gain of the Error Amplifier should be adjusted to provide an acceptable transient response by increasing or decreasing the Error Amplifier's feedback capacitor (C_{AMP}). The bandwidth of the control loop will vary directly with the gain of the error amplifier.

If C_{AMP} is too large, the loop gain/bandwidth will be low, the COMP pin will slew too slowly and the output voltage will overshoot as shown in Figure 32. On the other hand, if C_{AMP} is too small, the loop gain/bandwidth will be high, the COMP pin will slew very quickly and overshoot will occur. Integrator “wind up” is the cause of the overshoot. In this case, the output voltage will transition more slowly because COMP spikes upward as shown in Figure 33. Too much loop gain/bandwidth increases the risk of instability. In general, one should use the lowest loop gain/bandwidth possible to achieve acceptable transient response. This will insure good stability. If C_{AMP} is optimal, the COMP pin will slew quickly but not overshoot and the output voltage will monotonically settle as shown in Figure 35.

After the control loop is tuned to provide an acceptable transient response, the steady−state voltage ripple on the COMP pin should be examined. When the converter is operating at full steady−state load, the peak−to−peak voltage ripple (V_{PP}) on the COMP pin should be less than 20 mV_{PP} as shown in Figure 34. Less than 10 mV_{PP} is ideal. Excessive ripple on the COMP pin will contribute to jitter.

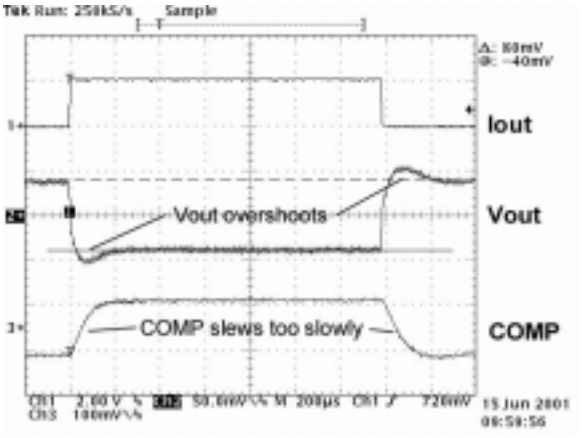


Figure 32. The Value of C_{AMP} Is Too High and the Loop Gain/Bandwidth Too Low. COMP Slews Too Slowly Which Results in Overshoot in V_{OUT}.

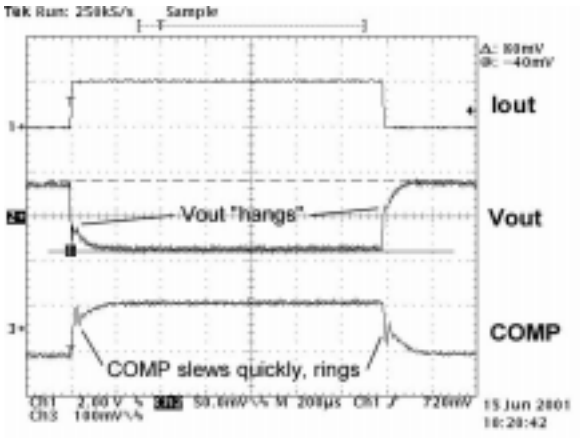


Figure 33. The Value of C_{AMP} Is Too Low and the Loop Gain/Bandwidth Too High. COMP Moves Too Quickly, Which Is Evident from the Small Spike in Its Voltage When the Load Is Applied or Removed. The Output Voltage Transitions More Slowly Because of the COMP Spike.

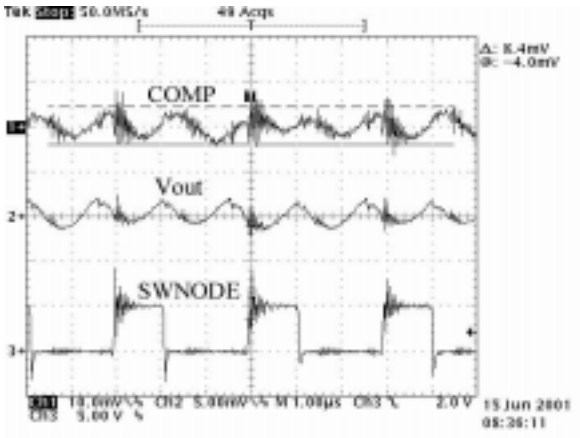


Figure 34. At Full−Load the Peak−to−Peak Voltage Ripple on the COMP Pin Should Be Less than 20 mV for a Well−Tuned/Stable Controller. Higher COMP Voltage Ripple Will Contribute to Output Voltage Jitter.

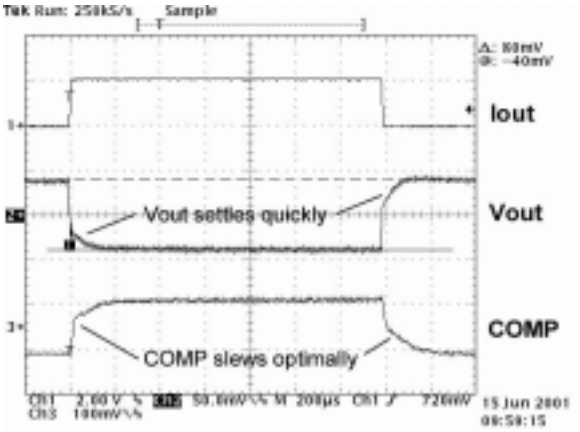


Figure 35. The Value of C_{AMP} Is Optimal. COMP Slews Quickly Without Spiking or Ringing. V_{OUT} Does Not Overshoot and Monotonically Settles to Its Final Value.

10. Current Limit Setting

When the output of the current sense amplifier (COx in the block diagram) exceeds the voltage on the I_{LIM} pin, the part will latch off. For inductive sensing, the I_{LIM} pin voltage should be set based on the inductor's maximum resistance (R_{LMAX}). The design must consider the inductor's resistance increase due to current heating and ambient temperature rise. Also, depending on the current sense points, the circuit board may add additional resistance. In general, the temperature coefficient of copper is +0.39% per °C. If using a current sense resistor (R_{SENSE}), the I_{LIM} pin voltage should be set based on the maximum value of the sense resistor.

Since under transient conditions, a single phase may see a very high positive or negative current for mere microseconds at a time, the user may set a limit to the maximum phase current. The phase current limit prevents an individual phase from conducting too much current in either the positive or negative direction. The IP_{LIM} pin is used to set this threshold.

The IO pin provides an output signal proportional to inductor current, which can be used for system validation purposes as well as for current limiting. This signal is fed back into the IC through a low−pass filter between IO and IOF, as shown in Figure 36, so designers may customize the response time of the current limit functions.

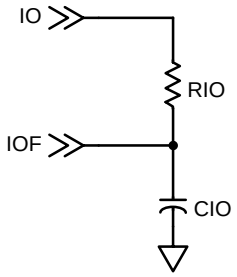


Figure 36. Filtering the IO Signal

The designer should select these values empirically. A 0.01 μF capacitor and a 20 kΩ resistor will prevent inadvertent current limit triggering in many cases.

V_{IO} can be calculated as

$$V_{IO} = n_{\Phi} \cdot I_L \cdot R_L \cdot g \cdot 3.3$$

where:

n_{Φ} = the number of phases;
I_L = inductor current (A);
R_L = sense element resistance (Ω);
g = current sense to IO pin gain.

The user may easily set the phase and module current limits at this point. This limit is programmed by a resistor divider from V_{REF}, as shown in Figure 37.

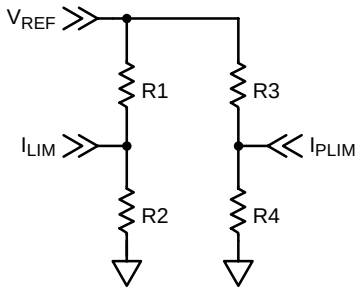


Figure 37. Programming the Current Limits

When the NCP5316 is powered up, V_{REF} will be 3.3 V. This allows the user to set the module and phase current limits with the resistor divider shown above.

$$\text{Module Current Limit} = \frac{V_{REF}}{R_L \cdot g \cdot n_{\Phi}} \cdot \frac{R1}{R1 + R2}$$

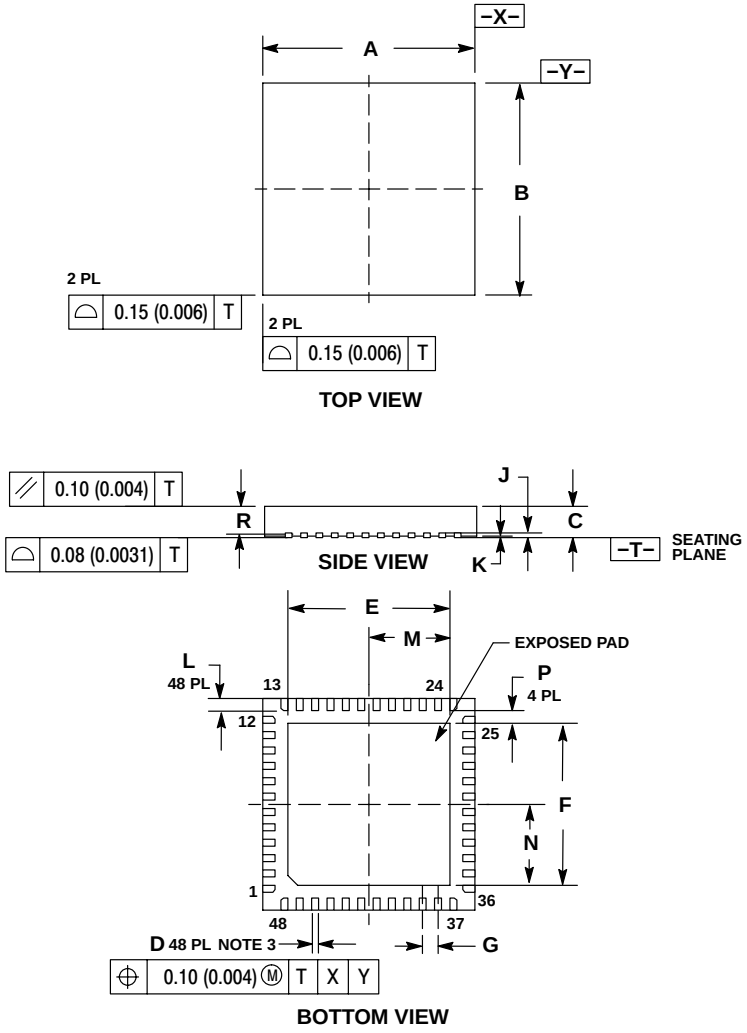
$$\text{Phase Current Limit} = \frac{V_{REF}}{9.5 \cdot R_L} \cdot \frac{R3}{R3 + R4}$$

For convenience in component selection, as well as to keep the V_{REF} pin current below 1 mA, the designer is recommended to set R2 and R4 equal to 10 kΩ.

For the overcurrent protection to work properly, the current sense time constant (RC) should be slightly larger than the R_L time constant. If the RC time constant is too fast, a step load change will cause the sensed current waveform to appear larger than the actual inductor current and will trip the current limit at a lower level than expected.

PACKAGE DIMENSIONS

48−PIN QFN, 7 × 7
MN SUFFIX
CASE 485K−02
ISSUE B

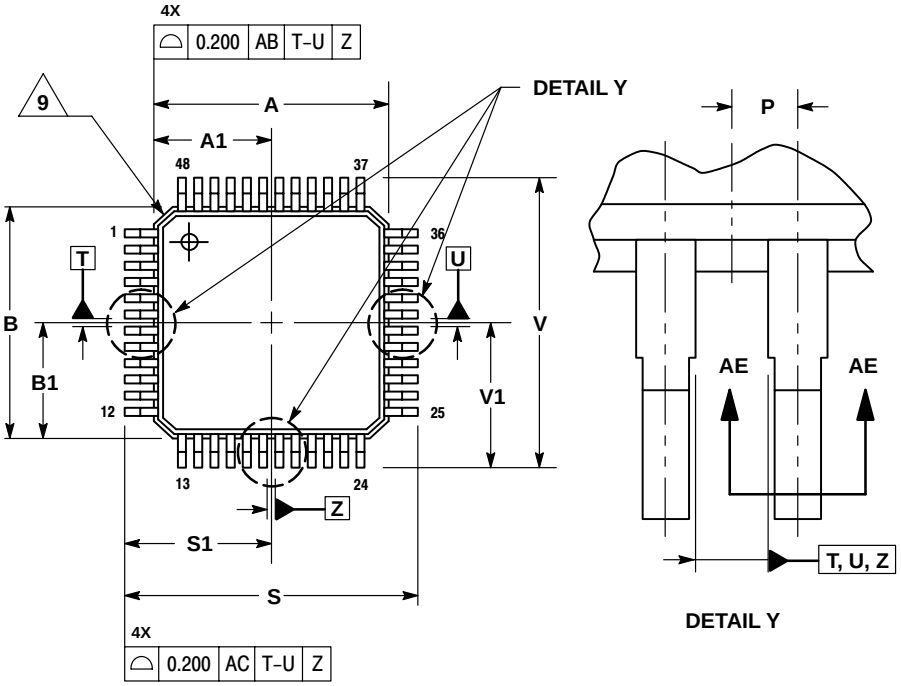


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.30 AND 0.35 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. 485K−01 OBSOLETE, NEW STANDARD IS 485K−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.00 BSC		0.276 BSC	
B	7.00 BSC		0.276 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	5.26	5.46	0.207	0.215
F	5.26	5.46	0.207	0.215
G	0.50 BSC		0.020 BSC	
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	2.85	2.95	0.112	0.116
N	2.85	2.95	0.112	0.116
R	0.60	0.80	0.024	0.031
P	0.42 REF		0.165 REF	

PACKAGE DIMENSIONS

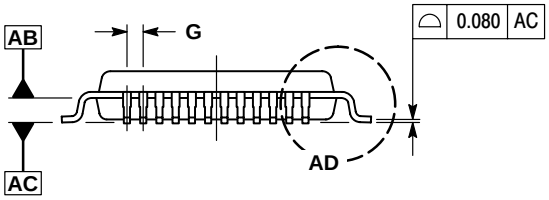
LQFP−48
FTB SUFFIX
CASE 932−02
ISSUE E

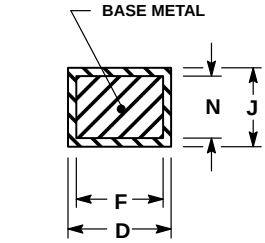


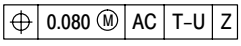
DETAIL Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

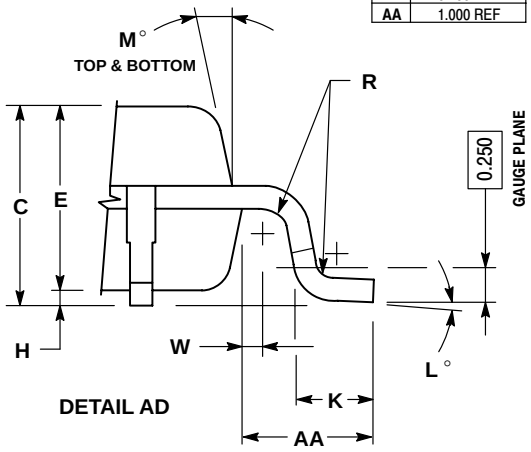
	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	1°	5°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	







SECTION AE−AE



DETAIL AD

Notes

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